Nanosheet Width Investigation for Gate-All-Around Devices Targeting SRAM Application

Ashish Pal, El Mehdi Bazizi, Benjamin Colombeau, Blessy Alexander and Buvna Ayyagari-Sangamalli

Applied Materials, Santa Clara, USA; Email: ashish_pal@amat.com

***Abstract*— Gate-all-around (GAA) transistor architecture offers more design flexibility in choosing a nanosheet width tailored for a given application. This is a unique advantage of GAA over FinFET, where the channel perimeter (Weff) is quantized, mostly determined by number of fins and fin height per device (Weff = Fin number x (2 x fin height + fin thickness)). In this paper we discuss the GAA NMOS and PMOS nanosheet width optimization to achieve the best SRAM performance. By using 3D process, device and circuit modeling, we investigate the impact of NMOS and PMOS nanosheet widths on different SRAM performance metrics. Finally, we show that implementation of different NMOS and PMOS nanosheet widths can lead to better GAA SRAM performance, significantly higher than their FinFET SRAM counterpart.**

Keywords*— *Gate-all-around, FinFET, SRAM, nanosheet width

I. Introduction

As the next generation logic transistor architecture, Gate-all-around (GAA) devices need to be optimized for both logic, SRAM and I/O applications. Other than conventional performance FEOL tuning knobs as in FinFET, such as gate length, doping profiles and process thermal budgets, the nanosheet width (NSW) is an additional optimization parameter for GAA. Unlike in FinFET, where the channel perimeter (Weff) is quantized because of integer fin numbers, NSW and hence the Weff in GAA can be varied continuously and can be optimized separately based on the targeted application. In this paper, we show such NSW optimization schemes for conventional 6-transistor SRAM application. We evaluate the SRAM performance metrics for different GAA NMOS and PMOS NSW combinations and attempt to match or exceed FinFET SRAM performance.

II. Description of Approach

Fig. 1 shows the SRAM characterization modeling workflow, which combines the FEOL transistor characteristics and MOL/BEOL parasitics and finally generates different cell and array level SRAM performance metrics. First FinFET and GAA transistor process modeling were performed assuming typical 3nm dimensions (Fig. 2), similar thermal budgets and process flow, generating 3D device structures with doping profile (Fig. 3), used further for device-level performance evaluation (Fig. 4). For this purpose, we calibrated our drift-diffusion based modeling framework to the semi-classical sub-band Boltzmann transport equation (BTE) one, solved consistently with Poisson and Schrodinger equations [1]. The fin width in FinFET and the nanosheet thickness in GAA are both assumed to be 5nm, leading to similar electrostatics (subthreshold swing and DIBL) in FinFET and GAA. For silicon, the electron mobility is higher at (100) surface compared to the (110) one, which results in 23% higher current in GAA than FinFET for same Weff. In contrary, the (100) surface shows lower hole mobility compared to the (110) surface. This results in 14% lower current in GAA PMOS compared to FinFET NMOS for same Weff.

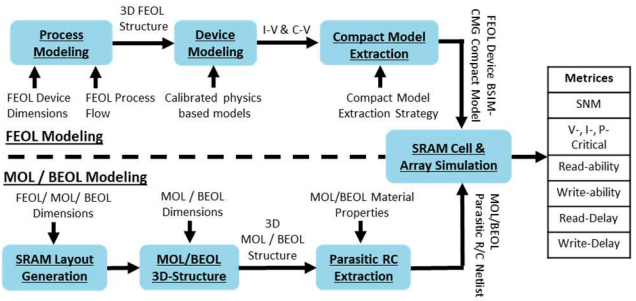

Figure 1. FinFET and gate-all-around (GAA) SRAM characterization workflow connecting FEOL transistor characteristics and MOL/BEOL parasitics to SRAM circuit performance metrics.

Parameter	Value
Gate Pitch	45 nm
Fin Pitch	24 nm
Fin Width	5 nm
Fin Height	60 nm
Nanosheet Thickness	5 nm
Nanosheet Width	8-24 nm
Gate Length	14 nm
M0 Pitch	22 nm
M1 pitch	30 nm

Figure 2. Typical 3nm node dimensions used in this work

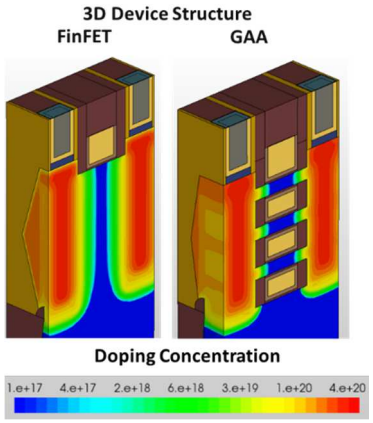

Figure 3. FinFET and GAA NMOS 3D device structures generated using process modeling.

III. Results and Discussion

Fig. 5 shows an example of 1:1:1 FinFET SRAM cell layout. For GAA SRAM layout, the fin mask pattern is

978-1-6654-0685-7/21/$31.00 ©2021 IEEE

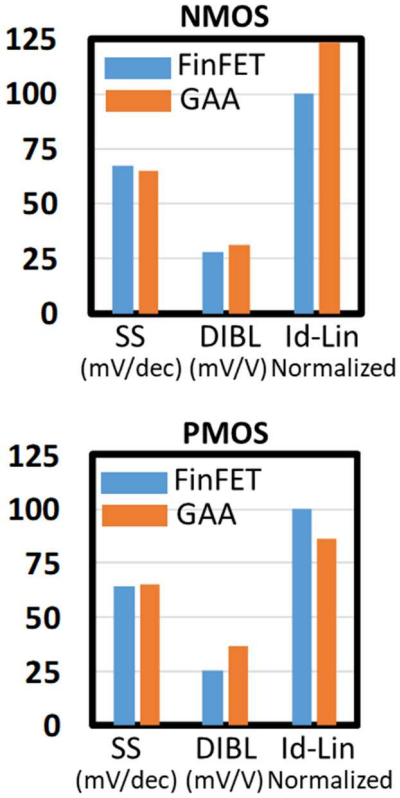

Figure 4. FinFET and GAA device performance comparison generated using device modeling for 16nm GAA nanosheet width. Both FinFET & GAA NMOS devices has similar DIBL and SS, whereas drive-current in NMOS GAA is higher due to higher NMOS mobility. For PMOS, GAA has higher DIBL due to enhanced dopant diffusion and lower Id-lin due to lower hole mobility.

replaced with the nanosheet mask pattern. To optimize SRAM performance, we varied the NSW in GAA between 8-24nm, for both NMOS and PMOS. Since the pull-down and access transistor in GAA SRAM share the same nanosheet, their NSW is assumed to be the same. The SRAM layout is used to generate a 3D structure of MOL/BEOL SRAM interconnects (Fig. 6). Using this 3D MOL/BEOL structure, along with typical material properties (resistivity and permittivity), the MOL/BEOL parasitic resistances and capacitances are extracted. By combining the BSIM-CMG compact models calibrated to individual transistors characteristics and the MOL/BEOL parasitics, SRAM circuit

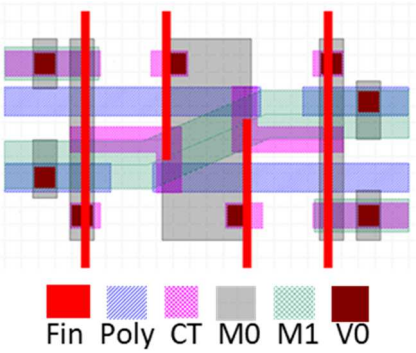

Figure 5. FinFET SRAM layout used in this study. For GAA, the fins are replaced by nanosheets.

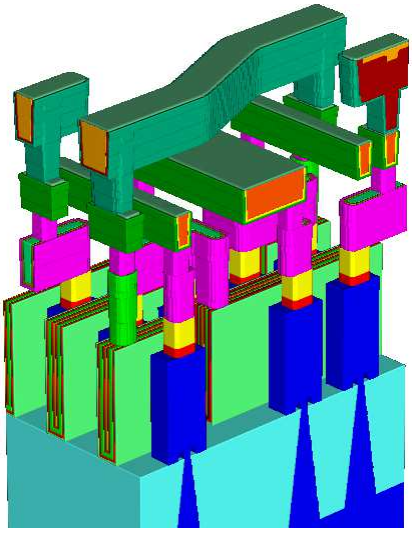

Figure 6. 3D MOL/BEOL structure of FinFET SRAM cell used for MOL/BEOL parasitic resistance and capacitance extraction. The S/D epi-shape is approximated as rectangular instead of a typical diamond one.

performance is evaluated (Fig. 7 and 8), and different performance metrics are extracted at both cell and array level [2]. The static noise margin, the most important stability metric is slightly lower in GAA SRAM compared to FinFET SRAM (Fig. 7). The other important stability metric, I-critical does not depend on PMOS NSW and here GAA SRAM

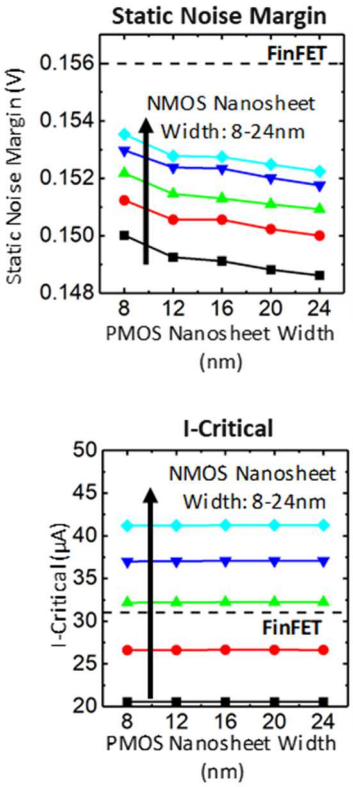

Figure 7. Comparison of static noise margin (SNM) and I-critical performance metrics between FinFET & GAA SRAM for different combination of GAA NMOS & PMOS nanosheet widths. GAA SRAM SNM is lower than FinFET SRAM SNM. To have better I-critical in GAA SRAM compared to FinFET SRAM, the GAA NMOS nanosheet width needs to be at least 16 nm.

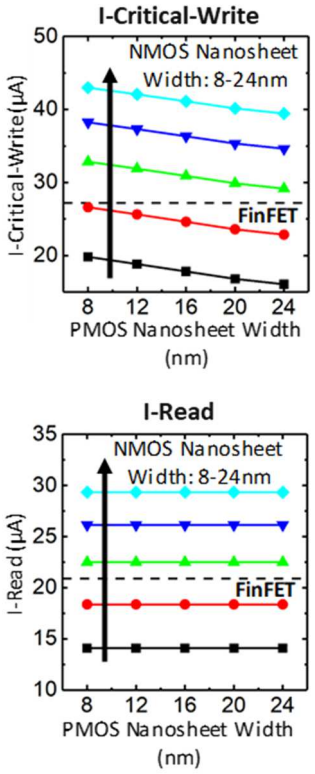

Figure 8. Comparison of I-critical-write and I-read performance metrics between FinFET & GAA SRAM for different combination of GAA NMOS & PMOS nanosheet widths. For better performance, the GAA NMOS nanosheet width needs to be at least 16 nm.

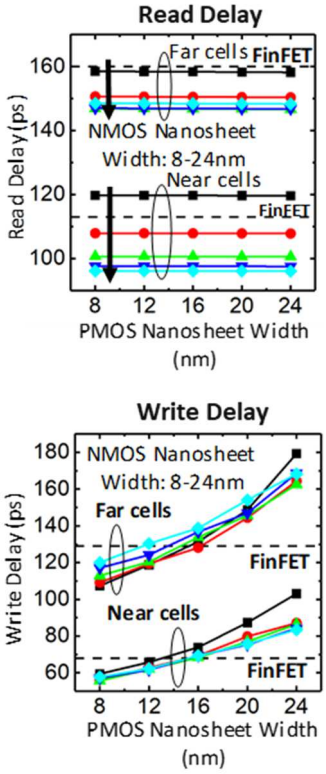

Figure 9. Comparison of read and write delay between FinFET & GAA SRAM. With optimized nanosheet widths, GAA SRAM performance can be better than FinFET SRAM.

shows better performance than FinFET one for NMOS NSW > 16nm (Fig. 7). To characterize the write operation, I-critical-write parameter is extracted. As PMOS or NMOS NSW reduces, I-critical-write reduces. To match FinFET write performance,GAA SRAM needs at least 16nm NMOS NSW (Fig. 8). The read-operation depends entirely on NMOS access and pull-down transistors and hence read-current is independent of PMOS NSW. The read current in GAA SRAM cell can be higher if the NMOS NSW is chosen to be 16nm or higher (Fig. 8).

Fig. 9 compares the time-domain performance – read and write delay of GAA SRAM with the FinFET one for a 128 x 128 SRAM array. As mentioned earlier, the read-operation is mostly dependent on the access and pull-down NMOS transistor and hence read delay is independent of PMOS NSW. The word-line and bit-line signals reach quicker to an SRAM cell near the bit-line drivers; hence the read-delay is lower for a near-cell compared to a far-cell. Lower NMOS NSW translates to lower drive-strength of the NMOS transistors, resulting in higher read delay. To achieve comparable read delay as in FinFET SRAM, the NMOS NSW needs to be at least 8nm or more. On the other hand, the write delay is a comparatively stronger function of PMOS NSW. Higher pull-up PMOS nanosheet width makes the switching difficult for the cell, resulting in higher write delay. To achieve similar write delay as in FinFET SRAM, a PMOS NSW of 16nm or below should be used in GAA SRAM.

Fig. 10 lists the key NMOS & PMOS NSW combinations along with the most important performance metrics for 1:1:1 SRAM cell. Technologically, it might not be feasible to use very different NSW for NMOS and PMOS, hence the difference between the NMOS and PMOS NSW is kept at 4nm or lower. With this constraint, higher NMOS NSW (20nm or higher) also calls for higher PMOS NSW, which results in write performance degradation for GAA SRAM cell. With lower NMOS NSW (12nm or lower), the drive strength of the NMOS transistors degrades, resulting in worse I-critical and I-critical write than FinFET. The GAA SRAM with 16nm NMOS and PMOS NSW performs comparably with the FinFET SRAM, with the advantage of 14% higher write ability, thanks to stronger NMOS and weaker PMOS in GAA. By reducing the PMOS NSW to 12nm, the GAA SRAM performance can be further improved by reducing the write delay by 7-9% compared to FinFET SRAM, therefore emphasizing the benefit of NSW optimization in GAA architecture.

IV. Conclusion

In this paper, we compared SRAM performance of FinFET and GAA architecture for 3nm technology node. Using process and device modeling, we first evaluated both

Comparison of Different Performance Metrics b/w FinFET & GAA SRAM for Different Nanosheet Width

Metric	FinFET SRAM	GAA SRAM w/ Different Nanosheet Widths				
		NMOS: 16nm PMOS: 16nm	NMOS: 16nm PMOS: 12nm	NMOS: 12nm PMOS: 12nm	NMOS: 20nm PMOS: 16nm	NMOS: 20nm PMOS: 20nm
SNM	0.156 V	- 3 %	- 2.9 %	- 3.5 %	- 2.4 %	- 2.2 %
I-critical	31 μA	+ 3.9 %	+ 3.9 %	- 14 %	+ 20 %	+ 20 %
Write Ability	27.2 μA	+ 14 %	+ 17 %	- 5.9 %	+ 33 %	+ 30 %
Write Delay	Near: 68 ps Far: 129 ps	Near: 0 % Far: + 3.9 %	Near: - 9.4 % Far: - 7.0 %	Near: - 8.2 % Far: - 7.4 %	Near: + 1.5 % Far: + 6.2 %	Near: + 10 % Far: + 14 %

Figure 10. Choosing NMOS & PMOS nanosheet widths combination for best GAA SRAM performance.

individual NMOS and PMOS transistor performances for both FinFET and GAA architecture. For same channel perimeter, the GAA NMOS and PMOS shows 23% higher and 14% lower drive-current respectively than the FinFET NMOS and PMOS. The NMOS and PMOS nanosheet widths are optimized for GAA to achieve the best SRAM performance. It is found that non-equal nanosheet widths (16nm for NMOS and 12nm for PMOS) are optimum for GAA SRAM, leading to 17% higher write-ability and 7-9% lower write delay than FinFET SRAM.

REFERENCES

[1] L. Jiang et al., "Complementary FET Device and Circuit Level Evaluation Using Fin-Based and Sheet-Based Configurations Targeting 3nm Node and Beyond," 2020 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2020, pp. 323-326, doi: 10.23919/SISPAD49475.2020.9241655.

[2] A. Pal etal., "Extending materials to systems co-optimizationTM (MSCOTM) modeling to memory array simulation", Proc. SPIE 11614, Design-Process-Technology Co-optimization XV, 116140G (22 February 2021); https://doi.org/10.1117/12.2583923.