Complementary FET for Advanced Technology Nodes: Where Does It Stand?

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***Abstract*— Nanosheet on nanosheet configured complementary FET (CFET) is investigated using the Materials to Systems Co-optimization (MSCO™) modeling framework at both device and circuit levels developed at Applied Materials. Compared to N3 FinFET with the same footprint for a single device, both nMOS and pMOS for CFET shows lower drive current than FinFET by 26% and 45% respectively. At the circuit level, CFET shows lower iso-power frequency by 20%, mainly due to lower drivability and high super-via resistance.**

Keywords— Complementary FET, FinFET, Nano-sheet FET, DTCO, Ring Oscillator, Circuit Modeling

I. Introduction

In order to maintain historical trend of continued MOSFETs scaling for logic technology, the industry has been driven toward a variety of technological innovations, including new transistor architectures. Complementary FET (CFET) is attracting considerable interest due to the active area saving by stacking nFET and pFET vertically [1-3]. At the same time, CFET can keep the excellent electrostatic integrity by using Fin or Gate-all-around (GAA) structures for channel. It enables further Lgate scaling down beyond 10 nm with acceptable electrostatics control (i.e., drain induced barrier lowering (DIBL) <100 mV/V). Additionally, vertical stacking of nMOS and pMOS offers simplified access of the transistor terminals [1] by shorting n/p drain contacts internally. This allows further reduction of the standard cells height and area. In this work, we compare the performance of CFET with nMOS on top of pMOS with FinFET at 3nm node at both device and circuit level.

II. CFET NMOS & PMOS Performance Comparison

FinFET consisting of 2 Fins is used as a reference device to compare with CFET. The same active footprint for single device is assumed for FinFET and CFET (Fig. 1). Following process integration flow (Fig. 2), we performed 3D TCAD process simulations based on device dimension assumptions (Fig. 3) and generated 3D structures for both CFET and FinFET(Fig. 4). For CFET, nMOS is on the top and pMOS at the bottom with 30nm isolation layer in between. Both nMOS and pMOS have 2 silicon nanosheets as channel. A dielectric layer at the bottom in S/D region is assumed to prevent the leakage under the bottom sheet [4]. SiGe with 50% Ge is used for S/D Epi for both FinFET and CFET pMOS. For FinFET, S/D Epi grows from the silicon substrate and the side of Fin, while for CFET, it only grows from the side of the sheets. The stress distribution for pMOS shows 745MPa and 200MPa compressive stress for FinFET and CFET respectively (Fig. 5).

To model electron and hole transportation accurately at 3nm node dimensions, mobility models are calibrated to semi-classical sub-band BTE (Boltzmann Transport Equation) [5]. Both nMOS and pMOS in CFET shows lower DIBL and subthreshold swing than FinFET (Fig. 6), indicating better electrostatics control for CFET. It benefits from all-around gate control and less dopant diffusion from S/D due to more interface segregation in GAA structure (Fig. 7). CFET channel is dominated by (100) surface, which provides higher electron mobility and lower hole mobility than FinFET main surface (110).

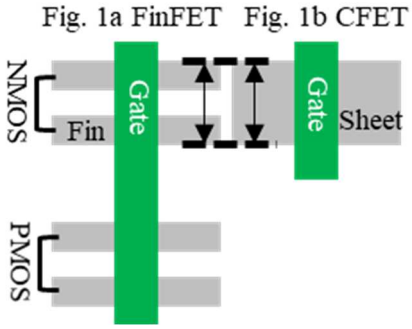

Figure 1. FinFET and CFET plan view, the same active footprint is assumed for single device.

Figure 2. CFET process flow

Parameter	FinFET	CFET
Gate Pitch	45 nm	45nm
Gate Length	15 nm	15nm
Fin Height	55nm	NA
Fin Width	5nm	NA
Nanosheet Width	NA	31nm
Sheet Thickness	NA	5nm
Channel Width	230nm	144nm

Figure 3. Device parameter used for FinFET and CFET

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However, nMOS still presents 26% lower Ion-Ioff performance than FinFET (Fig. 8a) due to 37% lower effective channel width. On the other hand, the gap between CFET and FinFET for pMOS is 45% (Fig. 8b) due to lower hole mobility in channel (Fig. 9). This is a result of lower hole mobility for (100) surface orientation as well as lower channel stress.

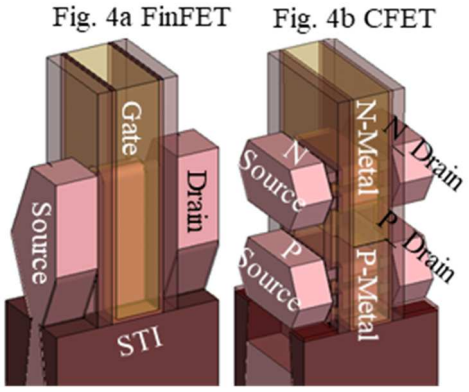


Figure 4. 3D structure for FinFET and CFET.

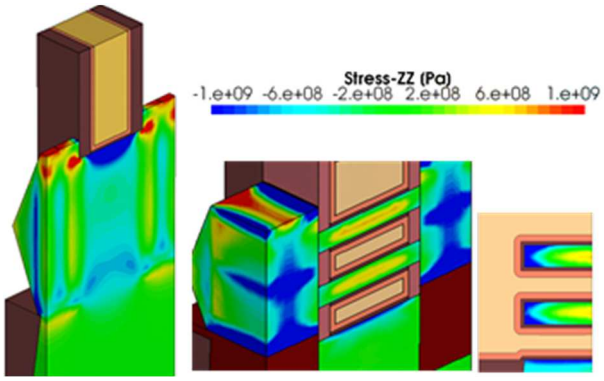


Fig.5. PFET stress distribution comparison. FinFET shows -745MPa stress while CFET shows -200MPa stress in channel.

Fig. 6a

NMOS	FinFET	CFET
DIBL(mV/V)	44.6	25.4
SS (mV/Dec)	68.2	64.5
Cov (fF)	0.0359	0.0183

Fig. 6b

PMOS	FinFET	CFET
DIBL(mV/V)	29.6	27.97
SS (mV/Dec)	65.12	64.46
Cov (fF)	0.0324	0.0196

Figure 6. Comparison of FinFET and CFET electrical characteristics

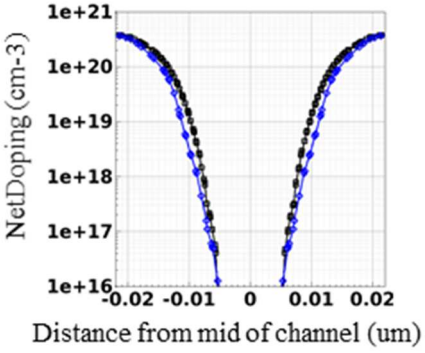


Figure 7. nMOS NetDoping Comparison. The same thermal budget is assumed for diffusion simulation.

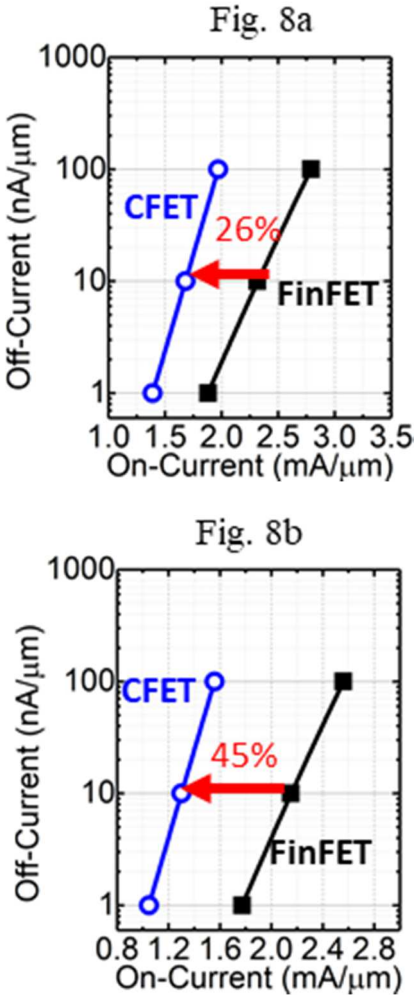


Figure 8. Comparison of FinFET and CFET Ion-Ioff performance for (a) NMOS and (b) PMOS

III. Area Scaling and CFET Circuit Performance

CFET is expected to reduce one signal track for standard cells, leading to an area benefit of about 19% for inverter (Fig. 10). CFET circuit performance is evaluated using a 31-stage ring oscillator (RO) [6].

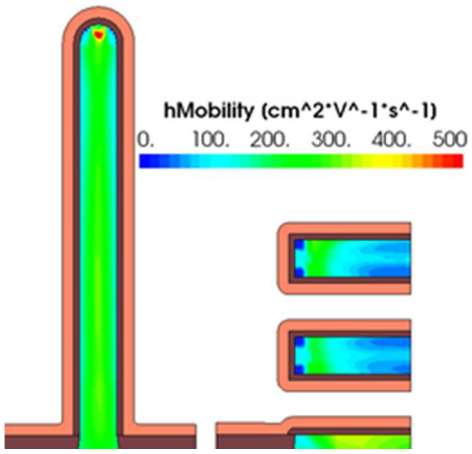


Figure 9. pMOS hole mobility comparison

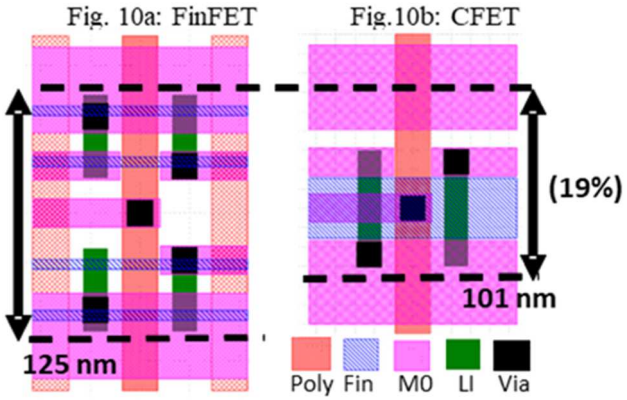
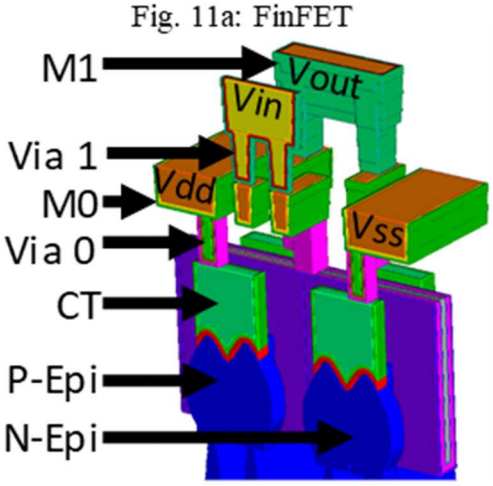


Figure 10. 3nm 4T inverter layouts design shows 19% area gain with CFET

First, 3D MOL/BEOL segments are built for CFET including the super-via, connecting PMOS source to V_{DD} (Fig. 11). For RO simulations, first only the FEOL device segment is included to study the impact of lower drive current in CFET. For iso-V_{DD} condition, CFET shows about 12% lower circuit performance than FinFET (Fig. 12a). However, CFET also shows 6% higher circuit performance at iso-power and 18% lower power consumption at iso-performance condition (Fig. 12b), indicating lower FEOL parasitic capacitance in CFET.



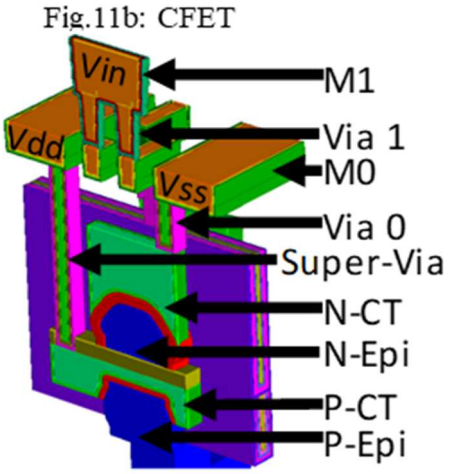
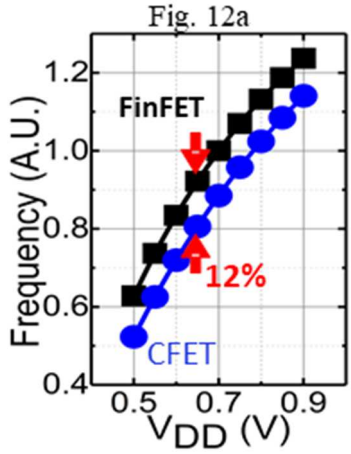


Figure 11. 3D Inverter structure showing S/D-epi, super-via and CT in CFET



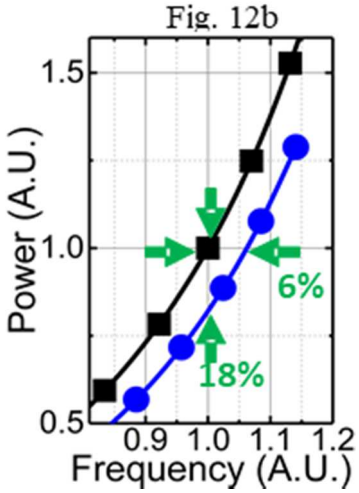
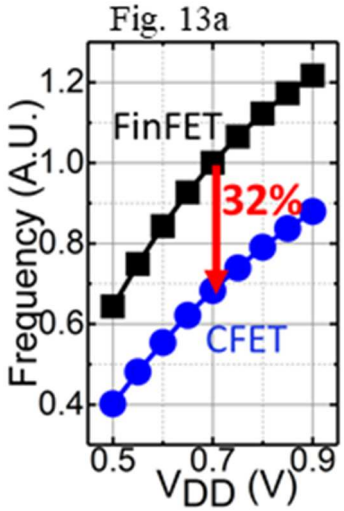


Figure 12. Comparison of FinFET & CFET RO performance with only FEOL device

The impact of lower drive current in CFET is more prominent when the MOL/BEOL parasitic are included in RO simulations. CFET shows 32% and 20% circuit performance degradation for iso-V_{DD} and iso-power condition respectively (Fig. 13) when compared to FinFET. It is observed that CFET has higher parasitic resistance due to presence of super-via and

higher parasitic capacitance due to scaled layout and device stacking (Fig. 14).



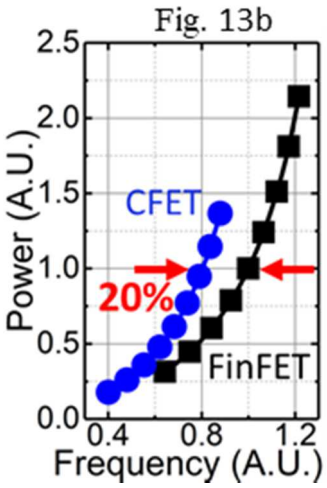


Figure 13. Comparison of FinFET and CFET RO performance after including MOL/BEOL parasitics

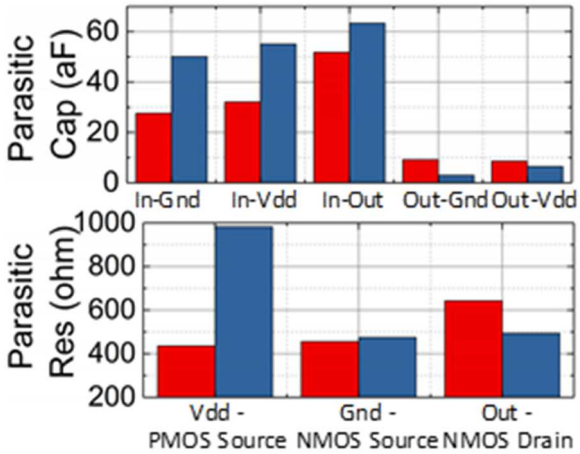


Figure 14. For same material system, CFET shows higher parasitic C and R than FinFET

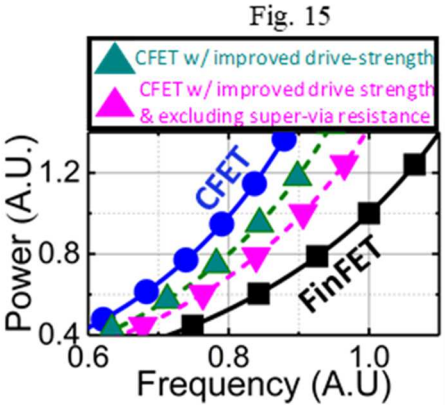


Figure 15. Impact of CFET FEOL drive and super-via on RO performance

IV. Technological Solution for CFET Circuit Performance

To take area -scaling advantage of CFET, both its FEOL and MOL/BEOL segments need to be improved. The CFET FEOL performance can be improved in several ways, such as by increasing the extension region doping concentration, by reducing the spacer dielectric constant and by other known techniques [2]. For CFET MOL/BEOL parasitic, the super-via resistance can be reduced by using bottom-up selective deposition techniques to eliminate the liner/barrier layers and to suppress seam formation as in conventional CVD process. Our modeling suggests that by improving CFET FEOL drive current, CFET circuit performance can be improved by 5% (Fig. 15). By reducing the super-via parasitic resistance and capacitance, CFET circuit performance can be further improved by another 5%, thus closing the gap between FinFET and CFET.

V. Conclusion

By MSCO™ modeling we show ring-oscillator performance for sheet-on-sheet CFET is 20% lower than 2-fin FinFET with 19% inverter area saving. CFET drivability at unit footprint and the dominant parasitic resistance of super-via are identified as the key schemes to be focused on for further improvement for CFET

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