Cost Simulations to Enable PPAC Aware Technology Development

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***Abstract* – industry standard practice for new technology definition by Power, Performance and Area (PPA) is evolving to add Cost (PPAC). The addition of cost will drive the need for new TCAD tools that can simulate cost as well as the structures and performance resulting from a process. In this paper the requirements for accurate process cost modeling will be presented along with the description of a commercial PPAC capable TCAD tool implementation.**

Keywords – PPA, PPAC, TCAD, Cost Modeling

I. Introduction

For many years, the standard when defining new technology targets has been PPA, Power, Performance, and Area, for example TSMC has described their 3nm technology as providing 25-30% lower power at the same performance (Power), 10-15% higher speed at the same power (Performance), and approximately 70% improvement in logic density (Area), relative to 5nm [1]. More recently there is a growing recognition that PPA is no longer sufficient, and that cost must be added (PPAC). Industry leaders such as TSMC [2], Imec [3], and Applied Materials [4] have all discussed the need for PPAC.

Current best practice in new technology design is to outline technology goals and then iterate with TCAD tools to develop the initial process. Current TCAD tools can simulate a process flow, produce a 3D representation of the resulting structure, and extract estimated performance, but what is missing is the ability to estimate cost during TCAD process design, meaning that while processes can be optimized for PPA, the C optimization during technology design is missing.

In this paper I will discuss the requirements for accurate process cost modeling and describe a commercial solution currently being developed by IC Knowledge LLC with Synopsys as a plug-in to Synopsys' Process Explorer.

II. Cost Modeling Overview

When simulating wafer fabrication cost, the fabrication process and fabrication facility must both be considered. The same process in two different fabs will have different costs, sometimes dramatically different, and within the same fab two different processes will also have different costs, sometimes dramatically different.

III. Fab Definition

To model fabrication cost in a process simulator, we must begin by defining a target fab. Key fab parameters include the capacity, wafer size, country where the fab is located and depreciation status. There is a wide variation in the capacity of fabrication equipment with throughputs ranging from tens of wafers per hour (wph) to over several hundred wph. The ability to match the throughput of a diverse equipment set improves as the fab capacity increases. As equipment throughput matching improves so does utilization and ultimately cost, see figure 1.

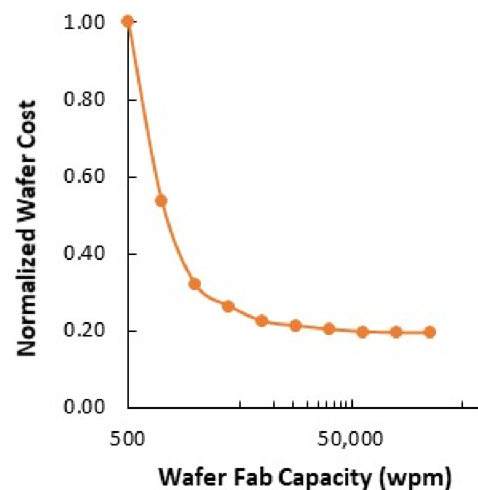

Figure 1. Normalized wafer cost versus fab capacity, new Taiwan fab, 5nm logic process [5].

The country where a fab is located strongly influences labor and utility rates although ultimately the difference in wafer cost at the leading edge is less significant than many believe (excluding taxes and incentives), see figure 2.

Typically, the biggest fab cost factor is the depreciation status of the equipment. For a new equipment set, depreciation can represent over 60% of the wafer fabrication cost with wafer costs dropping to less than half the initial costs over time, see figure 3.

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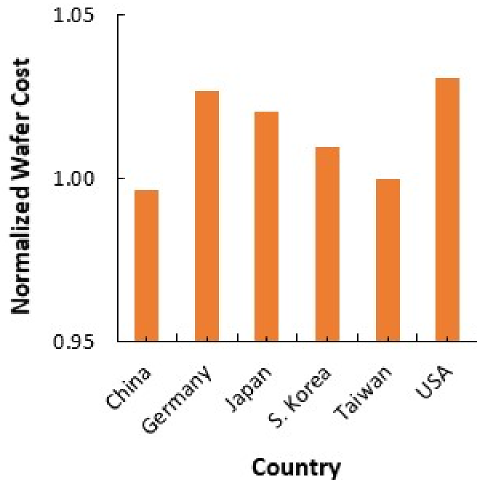

Figure 2. Normalized wafer cost versus country, new fab, 5nm logic process, 40,000 wpm [5].

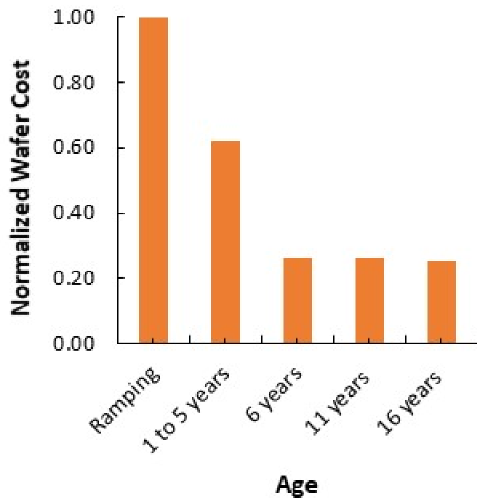

Figure 3. Normalized wafer cost versus fab age, 5nm logic process, 40,000 wpm, Taiwan [5]. Ramping is 50% utilization, 6 years is equipment fully depreciated, 11 years is building systems fully depreciated and 16 years is building fully depreciated.

A simulator must therefore allow the user to define a capacity, country, and depreciation status. Typical values for capacity would be approximately 40,000 wafers per month (wpm) for a logic fab and 75,000 wpm for a memory fab [6]. The simulator should have predefined labor and utility rates for the most common countries where fabs are located such as China, Japan, South Korea, Taiwan, the United States, and others. For new processes, a new fab with new depreciating equipment would typically be assumed, for older technologies the model should allow for partially and fully depreciated equipment to be selected. The industry standard for reporting depreciation is five-year straight line but other depreciation periods could also be supported. Since all leading-edge processing is done on 300mm wafers, 300mm may be used as a reasonable simplifying assumption for modeling.

IV. Process Definition

Each process flow will begin with one or more purchased starting wafers, a simulator should provide purchased wafer prices for typical starting wafers.

Each process step will require specific equipment, the equipment throughput will need to be specific to the process step being performed, for example a CVD deposition will have lower throughput for 1,000nm deposition than for 100nm deposition, also film type being deposited will affect deposition rates. With most fabrication equipment now provided as cluster tools with multiple chambers, the specific equipment configuration needs to be accounted for with number of chambers and types, number of robots and wafers transferred per move just a few of the factors that must be accounted for. With a defined fab capacity and step specific throughputs, an equipment set can be calculated once the full process is defined. A database of equipment configuration, cost and footprint can be used to not only calculate the number of equipment needed, but also the equipment set cost and footprint that ultimately drive the fab cleanroom size after grossing up the equipment footprint to account for equipment access, see figure 4.

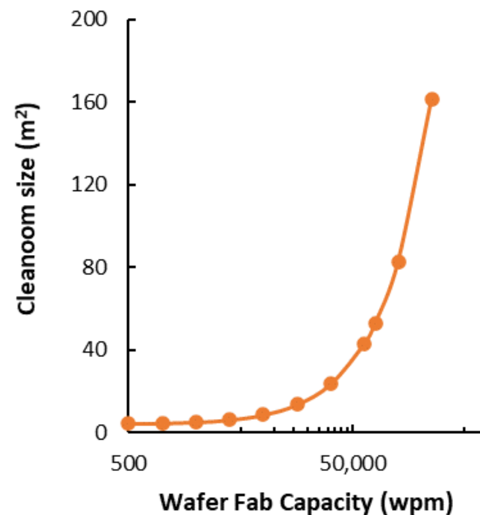

Figure 4. Calculated cleanroom size versus fab capacity, 5nm logic process [5].

Appropriate cost per meter squared can be applied to the cleanroom size to estimate the facility system and building capital costs.

Specific materials utilized and amounts will also depend on the films and film thicknesses and need to be defined.

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Calculations of labor costs, facility costs and equipment maintenance also need to be supported and ultimately all these factors must be allocated per step.

V. Commercial Implementation

IC Knowledge LLC (ICK) is the world leader in cost modeling of semiconductors and MEMS. ICK has developed Cost Explorer as a step-by-step wafer fabrication cost simulator and is currently working with Synopsys on implementing Cost Explorer as a plug-in module for Synopsys' Process Explorer TCAD tool (see figure 5.).

configuration and footprint by node, and materials required by film with material consumption by thickness, and tables of material cost by year. Specific equipment and equipment maintenance allocation to each step and materials cost per step are calculated.

The cleanroom size is estimated, and capital costs calculated, facilities costs are calculated for electricity, natural gas, water, maintenance, occupancy and insurance and the costs are allocated based on equipment footprint. Labor is also calculated and allocated.

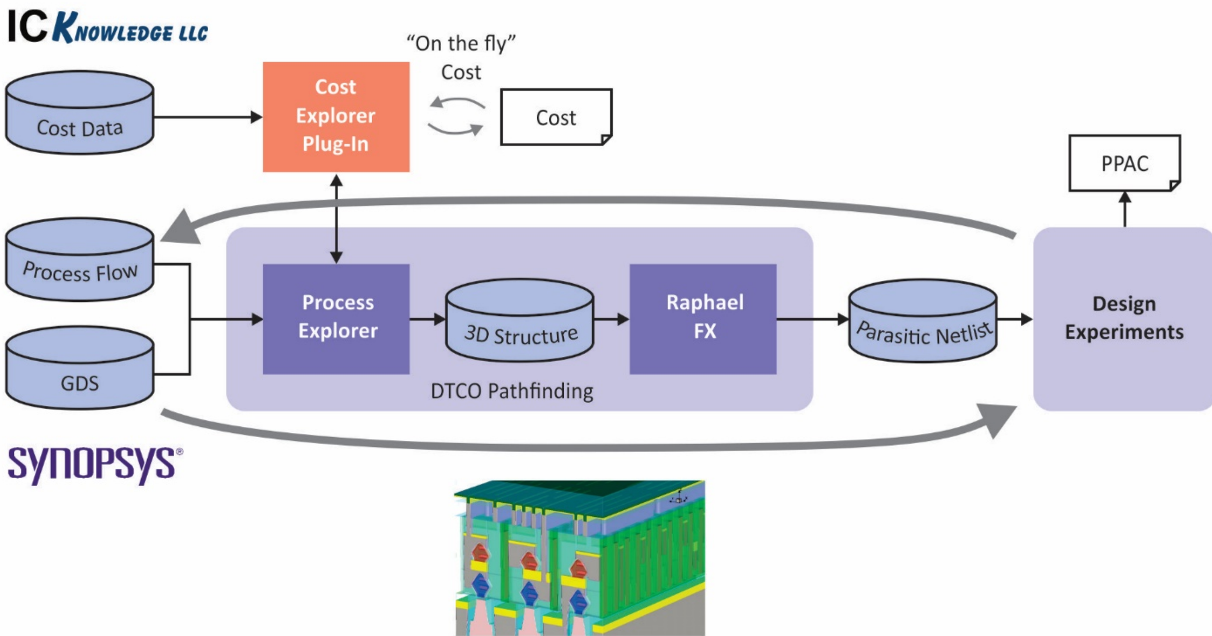

Figure 5. Cost Explorer commercial implementation in Synopsys DTCO suite.

Cost modeling begins with the user defining a wafer fab with capacity, operating policies (hours per week, weeks per year), country, and fab age. The model has labor and utility rates defined for 24 countries by year from 2010 to 2035.

Cost Explorer has a database of starting wafer types with pricing by year. The user selects a starting wafer(s) and model year, and the starting wafer cost populates.

As the user builds a process flow, they must select equipment types for each step, the model performs detailed throughput and material usage analysis for each step driven by the film and operation being performed with appropriate capture of parameters, for example a CVD step might require the user to select from a list of films that could be deposited and enter a thickness. The model has tables of equipment cost,

VI. Use Case and Examples

Cost Explorer estimates the cost for each process step with a detailed breakout of labor and capital costs, equipment maintenance, facility, and material costs. Because Cost Explorer is fully populated with configuration data including equipment, materials, utilities and labor, the plug-in allows technology designers to easily project the cost of individual steps and the process overall, see figure 6.

FinFETs are reaching scaling limits and horizontal nanosheets (HNS) are currently being developed for next generation logic technologies. Beyond HNSs, Complementary FETs (CFETs) stack nFET and pFET nanosheets and offer a promising solution for continued scaling. We have a large equipment manufacturer (OEM) that is a leading developer of CFETs, beta testing Cost Explorer in conjunction with Synopsys' DTCO suite.

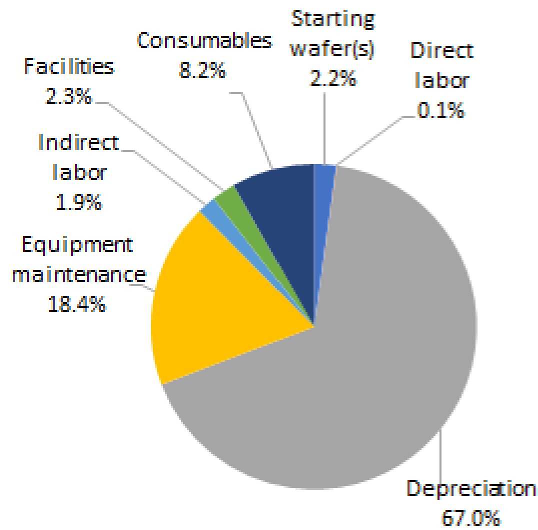

Figure 6. Wafer cost breakout by category, 5nm logic process, new fab, Taiwan, 40,000 wpm [5].

The OEM is simulating process flows in Process Explorer and evaluating the costs in Cost Explorer to generate PPAC. The OEM has evaluated four different node 3 processes up though the metal 2 level (BPR is Buried Power Rail):

1. Standard FinFET.
2. FinFET with BPR.
3. Monolithic CFET with BPR.
4. Sequential CFET with BPR.

The relative wafer costs are illustrated in figure 7.

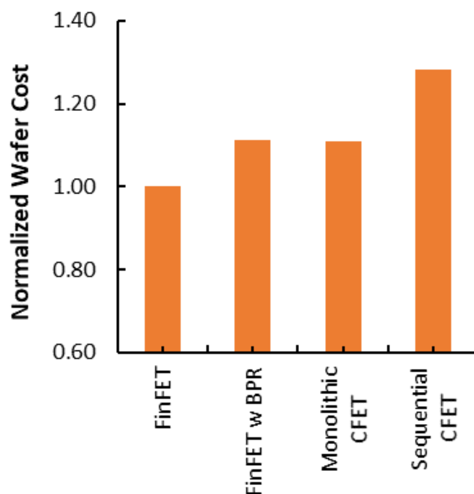

Figure 7. Relative Wafer Costs for N3 processes up through metal 2 [7].

Interestingly from figure 7, the Monolithic CFET that includes BPR is roughly the same cost as a FinFET with BPR. The CFET process in this case was designed to use a high degree of self-alignment and minimize cost. The monolithic CFET is also less expensive to fabricate than a sequential process CFET.

While building the process flows mentioned previously, the OEM has also evaluated patterning options. For example, two options were evaluated for local interconnect with via:

1. EUV local interconnect mandrel mask with EUV cut, and EUV via mask.
2. EUV local interconnect mandrel mask with multipatterned DUV cut, and EUV via mask.

The use of multipatterning for the local interconnect pattern cut was found to reduce the total patterning cost by approximately $52. The multipatterning process added process steps and therefore cycle time versus the EUV cut process. The availability of cost information enables users to trade-off EUV use, cycle time, process cost and process complexity.

I. Conclusion

The semiconductor industry is moving from PPA for leading edge technology definition to PPAC. To drive PPAC for future technologies, cost simulations need to be added to TCAD tools to provide cost aware technology development. IC Knowledge LLC has partnered with Synopsys and the two companies are in the process of adding IC Knowledge's Cost Explorer as a plus-in to Process Explorer within Synopsys' DTCO suite filling this critical industry TCAD need.

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