Impact of Random Phase Distribution in 3D Vertical NAND Architecture of Ferroelectric Transistors on In-Memory Computing

Gihun Choe
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA, USA
gchoe6@gatech.edu

Wonbo Shim
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA, USA
wshim30@gatech.edu

Jae Hur
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA, USA
jhur45@gatech.edu

Asif Islam Khan
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA, USA
asif.khan@ece.gatech.edu

Shimeng Yu
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA, USA
shimeng.yu@ece.gatech.edu

***Abstract*— Ferroelectric field-effect transistors (FeFETs) with 3D vertical NAND architecture (3D V-NAND) are investigated for in-memory computing. In polycrystalline ferroelectric Hafnia thin film, there are different phases such as monoclinic (M), and orthorhombic (O) phases. Those are randomly distributed throughout the ferroelectric gate stack. Such positional dispersion of two phases introduces read-out current variation in 3D V-NAND of FeFETs. Herein, we employ TCAD simulations to quantify such variation and optimize bias conditions for improving the accuracy of in-memory computing.**

Keywords*— *Ferroelectric, mixed phases, variations, nonvolatile memory, in-memory computing

I. Introduction

Ferroelectric field-effect transistors (FeFETs) using doped HfO_2-based materials have been extensively explored as the next-generation nonvolatile memory and in-memory computing [1]. In previous study, a 4-layer 3D V-NAND with FeFETs has been experimentally demonstrated [2]. 3D V-NAND array has been suggested promising for in-memory computing [3]. Similarly as CMOS devices, scaled FeFETs have intrinsic parameter fluctuations such as line-edge roughness and work function variation [4]. The random distribution of ferroelectric (FE) and dielectric (DE) phases is one of the random variation sources within the polycrystalline ferroelectric thin film, which comes from the physical atomic structure difference when it is deposited on a substrate [5]. FE phase can happen when the atomic structure is orthorhombic (*O*) phase. Other phases (e.g., monoclinic (*M*), and cubic (*C*) phases) exhibit non-FE behaviors [5]. Those FE/DE phases randomly disperse in the ferroelectric gate stack. In addition, the probability of each phase could be varied depending on the deposition method and type of dopant. Therefore, the ferroelectric properties is not uniformly applied for forming the channel. Previous study explored the impact of this variation source on the memory window of planar FeFET for device-to-device variation depending on the probability of each phase, size of grains and dimension parameters [6]. In this paper, we will study how this positional distribution of FE/DE phases affects the read-out current variation of 3D V-NAND architecture of FeFETs. First, we will propose the 3D V-NAND FeFETs structure and simulation method how we generate the FE/DE variation with its result. Second, the bias condition will be discussed to optimize the current distribution and on/off ratio for this architecture. Sequentially, the I_D-V_G characteristic under the adjusted voltage condition will be shown. Last, the read-out current distribution depending on the probability of FE/DE phase distribution will be exhibited under the aforementioned bias scheme.

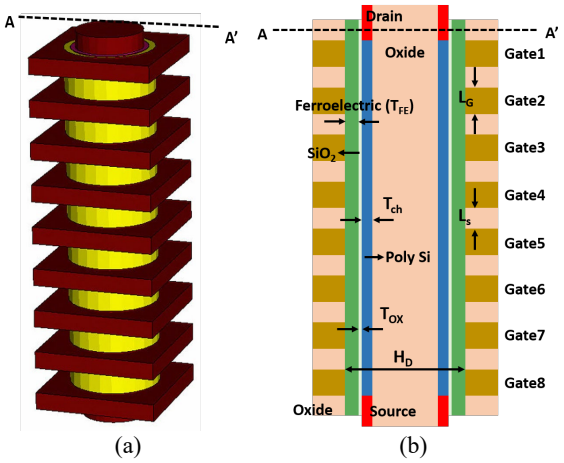


Fig. 1 (a) 3-D view and (b) cross-sectional view of vertical NAND architecture FeFETs.

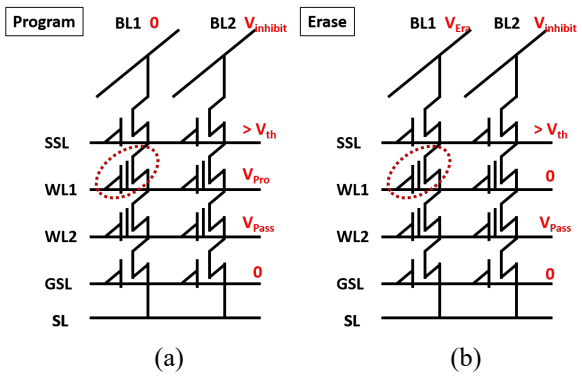


Fig. 2 V-NAND FeFETs (a) gate-program and (b) drain-erase scheme. The circled cell is selected.

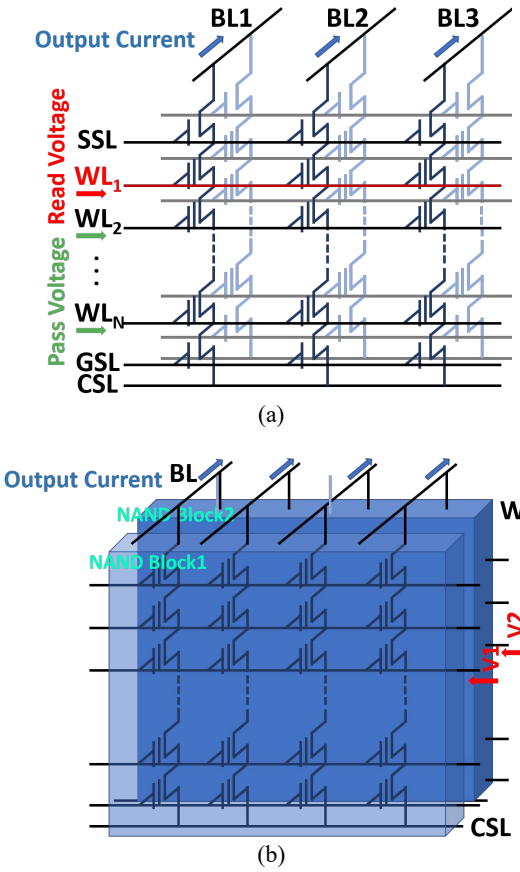


Fig. 3 (a) Circuit diagram and (b) schematic of V-NAND array consisting of multiple blocks for in-memory computing. V1 is for block 1, and V2 is for block 2.

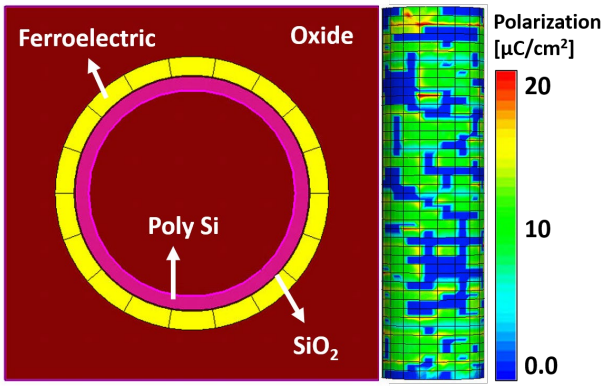


Fig. 4 Generated grains inside the ferroelectric layer for FE/DE phase distribution. Some grains are dielectric, thus no polarization in blue color.

II. Simulation Method

In this work, 8-layer 3D V-NAND of FeFET is designed using a Sentaurus TCAD to explore the read-out current variation induced by the spatial distribution of FE/DE phase (see **Fig.1**) [7]. The structural and material parameters used in this work are summarized in **Table I**. 1 nm interfacial SiO_2 layer and 8 nm $Hf_{0.5}Zr_{0.5}O_2$ layer are assumed. The source/drain is doped with n-type and the doping concentration is $10^{20}/cm^3$. The doping concentration of channel (p-type) is $10^{10}/cm^3$. Each gate length is 30 nm and space length is 20 nm. As shown in **Fig. 2(a)**, to program the selected cell on V-NAND, the programming voltage (V_{Pro} = ~4 V) will be applied to the word line (WL). The string selection line (SSL), ground selection line (GSL) and the other WLs should be turned on to prevent unselected cells on the same WL from being programmed with an inhibition voltage (~2 V) applied to unselected bit line (BL). To erase the selected cell, the erase voltage (V_{Era} = ~4 V) needs to be delivered from the BL via a drain-erase scheme (see **Fig. 2(b)**) [3]. Similar inhibition voltage (~2 V) needs to be applied to other unselected WLs due to the same reason above. Parallel read-out scheme could be used for in-memory computing in a layer-by-layer manner (**Fig. 3**).

Simulation method for generating random FE/DE phase is as below: 1) Make grains on ferroelectric layer [grain size = 10 nm×($2\pi \cdot R_{FE}/N_g$), N_G is the number of grains per L_{grain}, R_{FE} is $T_{FE}+T_{ch}+R_{BOX}$]. 2) Generate each grain's parameter for FE/DE phases as many as the total number of grains. 3) Apply random grain phases to ferroelectric parameter file. 4) Designate a phase of each grain using generated parameter file on the Sentaurus TCAD [7]. **Fig. 4** shows the polarization of generated grains and its positional FE/DE fluctuation. The blue color on the ferroelectric layer means those region does not have polarization. In other words, those grains are under dielectric phase.

Simulations are also comprised of doping-dependent model, thin-layer model, and high-field saturation model for mobility. Shockley-Read-Hall model and Auger model are used for recombination. For ferroelectric polarization, the Preisach model is employed [7].

TABLE I. Simulation Parameters

Name	Unit
Hole Diameter (H_D)	118 nm
Channel Thickness (T_{ch})	6 nm
Oxide Thickness (T_{OX})	1 nm
FE Thickness (T_{FE})	8 nm
Gate Length (L_G)	30 nm
Space Length (L_S)	20 nm
Grain Size (L_{Grain})	10 nm
Remnant Polarization (P_R)	15 μC/cm²
Saturation Polarization (P_S)	25 μC/cm²
Coercive Field (E_C)	1 MV/cm

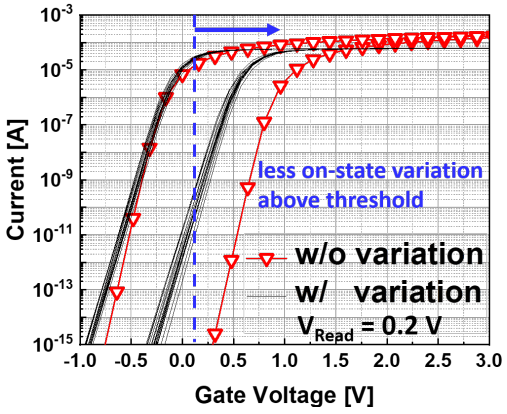
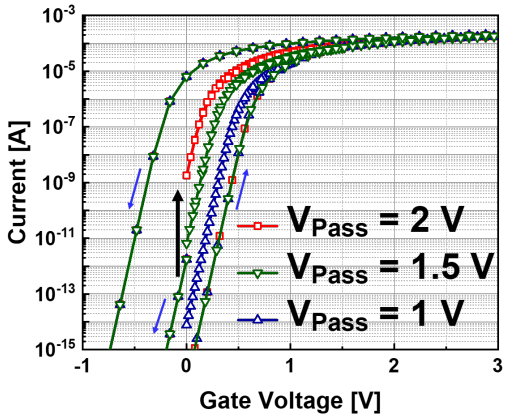
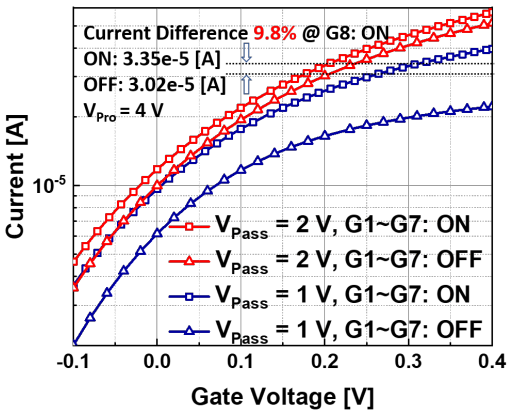


Fig. 5 I_D-V_G of a single cell of V-NAND FeFETs with and without FE/DE phase random variation. The voltage sweep range is from -4 V to 4 V. V_{Read} is designed to be 0.2 V.

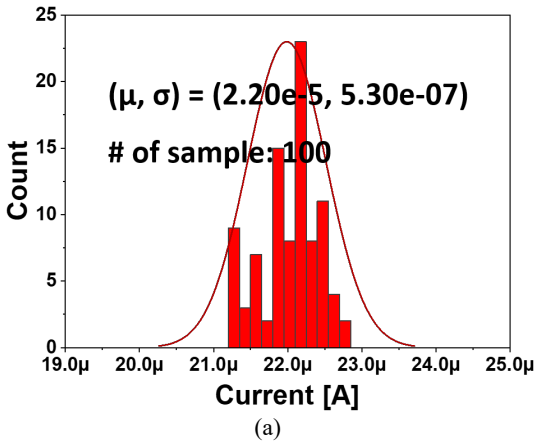


(a)

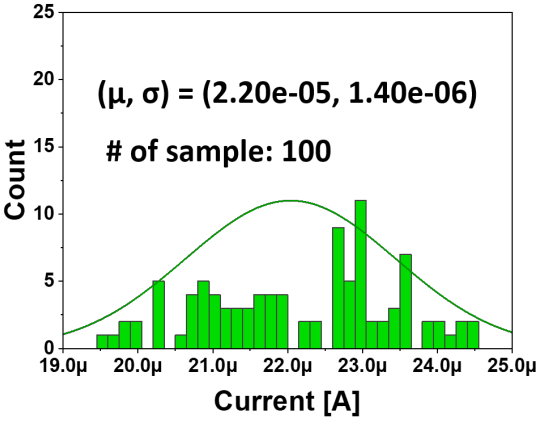


(b)

Fig. 6 (a) I_D-V_G of a V-NAND string: After applying V_{Pass}, off-state is disturbed with increasing current. (b) Read-out current of G8 *vs*. the data pattern of G1-G7.



(a)



(b)

Fig. 8 Distribution of V-NAND read-out currents with (a) 10% and (b) 30% of DE phase probability. Here, μ denotes the mean value and σ denotes the standard deviation.

III. Bias Optimization for Read-Out Current

Fig. 5 illustrated the I_D-V_G of a single cell of 3D V-NAND FeFETs with/without FE/DE phase distribution at V_{read} = 0.2 V. The gate voltage was swept from -4 V to 4 V and returned to -4 V to investigate the on-state current and off-state current. Red line I_D-V_G does not have FE/DE variation but has same structural dimension and polarization properties. As comparing with the result without phase variation, the memory window with phase variation is much smaller. This is because only 50% of total area has ferroelectric phase, whereby the leakage current could pass via the channel area under the other 50% of dielectric phase on the ferroelectric layer. Even though the FE/DE phase distribution, which is the result of the spatial phase variation, causes the read-out current distribution, the impact of this variation on on-state current is alleviated above the threshold where the read voltage (V_{Read}) should be biased at (see **Fig. 5**). As shown in **Fig 6**, there is a trade-off between on/off ratio of a single cell (G8) and its read-out current's dependence on the data pattern of other cells along the same vertical string. A higher the pass voltage V_{Pass} on unselected cells (G1 to G7) could minimize the current difference between the worst-case (all cells are off-states) vs. the best-case (all cells are on-states) since the other cells could much fully flow the current. However, a higher V_{Pass} may disturb the cell, whereby the on/off ratio is reduced. On the other hand, a lower the V_{Pass} on the unselected cells undesirably increases the read current variation for both on-state and off-state. Hence, by optimizing V_{Pass}, the current difference becomes less than 10% at V_{Read} = 0.2 V with V_{Pass} = 2 V. In addition, the other solution is using a higher programming voltage (V_{Pro} = 4 V). **Fig. 7** shows that the higher V_{Pro} helps achieve larger on/off ratio and reduced current difference between the worst-case and the best-case.

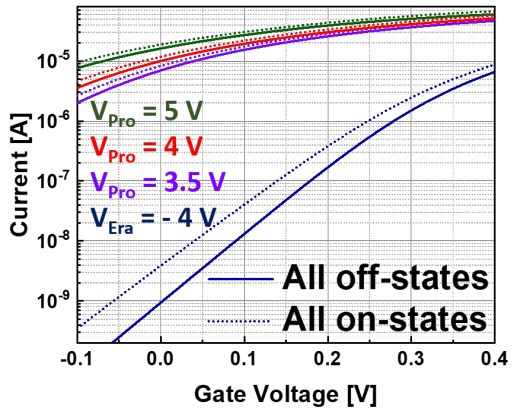


Fig. 7 Read-out current difference of G8 *vs*. gate voltage depending on V_{Pro}. With higher programming voltage, on/off ratio could be improved. Dot is G1 ~ G7 (all on-states) and straight line is G1 ~ G7 (all off-states).

IV. Impact of Variation on Read-Out Current

The probability of DE phase can be varied from 0% ~ 70% depending on the types and concentrations of the cation- and anion-based dopants used for the HZO deposition [5]. **Fig. 8** shows the read-out current distribution of the on-state G8 cells. The DE phase probabilities are 10% and 30%, respectively. The number of sample is hundred for each phase probability case. As shown in **Fig. 8**, when the probability of DE phase decreases, the read-out current variation decreases. Although both 10% and 30% of cases have the same mean value, the 10% DE probability of V-NAND shows 62% smaller standard deviation in read-out current than the 30% DE probability. This means that lowering the DE phase probability, in other words increasing the orthorhombic phase, is critical to ensure the read-out accuracy for in-memory computing.

V. Conclusion

3D V-NAND FeFETs for in-memory computing have been simulated. We optimized the bias conditions for mitigating the read-out current's data pattern dependency while maintaining more than at least 10 times of on/off ratio. The read-out current variation caused by the positional fluctuation of FE/DE phases is quantified, suggesting future material engineering is required to improve the purity of the FE phases.

Acknowledgment

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