8-1 A TCAD Study on Mechanism and Countermeasure for Program Characteristics Degradation of 3D Semicircular Charge Trap Flash Memory

N. Kariya[1], M. Tsuda[1], T. Kurusu[1], M. Kondo[1], K. Nishitani[1], H. Tokuhira[1], J. Shimokawa[1], Y. Yokota[1], H. Tanimoto[1], S. Onoue[1], Y. Shimada[1], T. Kato[1], K. Hosotani[1], F. Arai[1], M. Fujiwara[1], Y. Uchiyama[2], and K. Ohuchi[1,2]
[1]Institute of Memory Technology Research & Development, Kioxia Corporation, Yokkaichi, Mie, Japan
[2]Advanced Memory Development Center, Kioxia Corporation, Yokkaichi, Mie, Japan
Email: nayuta.kariya@kioxia.com

***Abstract*— A TCAD model to simulate program/erase characteristics of 3D charge trap flash memory cells is constructed and calibrated with the experiment. The mechanism of the program characteristics degradation of the semicircular cells are studied using the TCAD model and it is clarified that the current leakage path due to the fringe parasitic transistor causes the degradation. An initial charge injection technique is proposed to suppress the parasitic leakage current to improve the program characteristics of the semicircular cells.**

I. Introduction

Bit density of 3D flash memories has been grown for years by increasing the number of stacking layers [1]. However, the key process technology of memory hole etching becomes more challenging as the number of stacking layers increases. Shrinking the area per cell is another approach to increase bit density. Especially, bit density can be almost doubled if two strings of cells are formed in each memory hole. Several types of 3D flash memory technologies to shrink the area per cell have been proposed [2], [3]. We have recently developed a new 3D flash memory technology with semicircular shaped cell to boost bit density further [4].

Fig. 1 compares plane view of a conventional circular cell and a new semicircular cell. Fig. 2 illustrates a bird's eye view of an array of semicircular cells. In the circular cell, a control gate (CG) surrounds a cell all around and one NAND string is formed in each memory hole. While in the semicircular cell, the control gate is divided with insulator and two NAND strings are formed in each oval shaped memory hole.

However, experimental results revealed that the program characteristics of the semicircular charge trap cells are degraded compared to the circular cells. In this work, we have clarified the mechanism of the program characteristics degradation and proposed a countermeasure through TCAD simulations.

II. Simulatoin Model

Fig. 3(a) shows a structure for simulating program/erase characteristics of a semicircular cell. The structure has three CGs on two sides of a memory hole. The cell at the middle layer of front side CG is evaluated. Source and drain electrodes are attached to the lower and upper end of the channel, respectively. Bias conditions for simulating read, program, and erase operations are shown in Table 1. Sufficiently low bias V_{off} is applied to the back side CGs to cut off the current along the back side part of the channel in

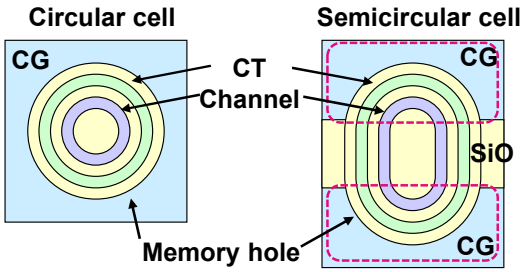

Fig. 1. Plane view of a circular and a semicircular cell.

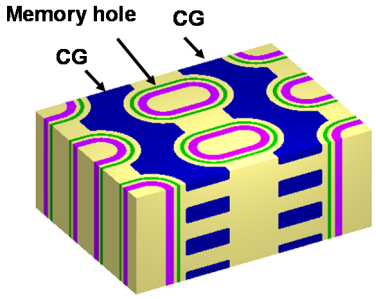

Fig. 2. Bird's eye view of an array of semicircular cells.

read operations. Fig. 3(b) shows enlarged view of a cell. Cell stack films consist of block (BLK), charge trap (CT) SiN, tunnel (TNL), and polycrystalline silicon channel layers.

Fig. 4 illustrates a conduction band diagram and an electron transport model in a program operation. We consider the following four processes [5]: (1) injection from the channel to conduction band of the CT layer according to tunneling effect, (2) drift motion and diffusion in conduction band of the CT layer, (3) capture and emission by traps in the CT layer, and (4) tunneling effect from the CT layer to the CG. The carrier transport model in an erase operation is similar to the program operation, except that injected carrier type is a hole. To obtain accurate current voltage characteristics of the polycrystalline silicon channel, grain boundary mobility and interface/bulk electron traps are considered.

III. Simulation and Experimental Results

First, we calibrated TCAD model parameters associated with CT SiN layer and channel polycrystalline silicon by comparing with the measured electrical characteristics of a conventional circular cell in order to guarantee accuracy of simulations. Fig. 5 shows simulated and experimental program/erase characteristics of a circular cell, and Fig. 6

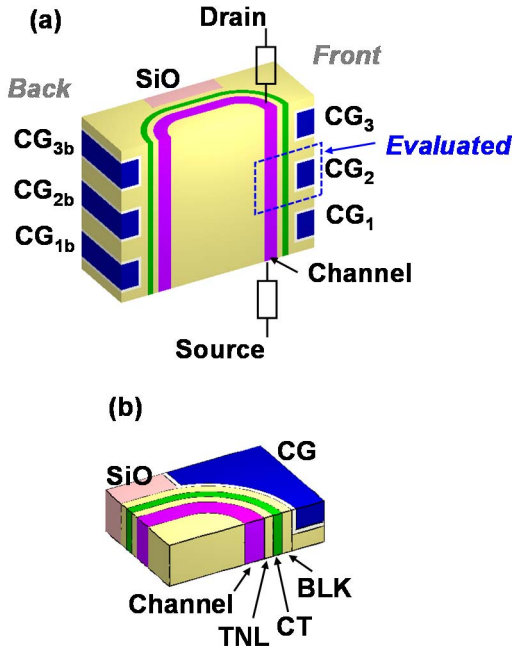

Fig. 3. (a) Simulation structure of a semicircular cell. (b) Enlarged view of a semicircular cell.

Table 1. Bias conditions for simulating read, program, and erase operations.

	Read	Program	Erase
Source	0	0	0
Drain	V_{DD}	0	0
CG_2	V_t	V_{pgm}	$-V_{era}$
CG_1, CG_3	V_{read}	V_{pass}	$-V_{era}$
CG_{1b}–CG_{3b}	V_{off}	V_{pass}	$-V_{era}$

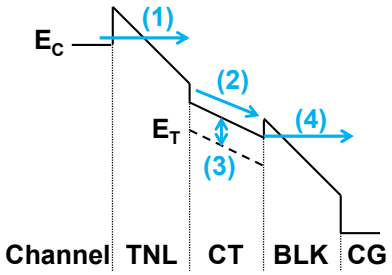

Fig. 4. Conduction band diagram and electron transport model in a program operation.

shows cell current from the initial state to programmed states. The simulated results are in good agreement with the experimental results.

Second, we carried out simulations for a semicircular cell with parameters calibrated by the first step. As shown in Fig. 7, the experimental program/erase characteristics of the semicircular cell are well reproduced again. It is noted that the same model parameters are used in the simulation of both circular and semicircular cells, which indicates that the

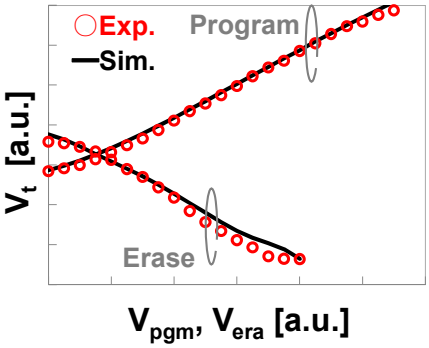

Fig. 5. Experimental and simulated program/erase characteristics of a circular cell.

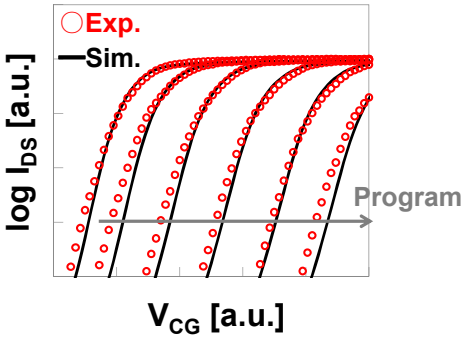

Fig. 6. Experimental and simulated cell current of a circular cell from the initial state to programmed states.

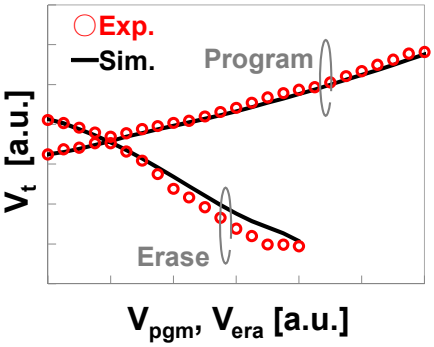

Fig. 7. Experimental and simulated program/erase characteristics of a semicircular cell.

difference in program characteristics results from the difference in the device geometry.

IV. Discussion

A. Mechanism of Program Slope Degradation

Fig. 8(a) compares simulated program characteristics of a circular and a semicircular cell. The program slope, the ratio of the threshold voltage (V_t) change to the program voltage (V_{pgm}) change, of the semicircular cell is extremely lower than that of the circular cell. Fig. 8(b) shows the subthreshold slope (SS) at each programmed state in the circular and semicircular cell. The SS remains almost constant in the circular cell, while the SS increases with V_{pgm} in the semicircular cell. The change in SS indicates that the current path changes as the program state becomes higher.

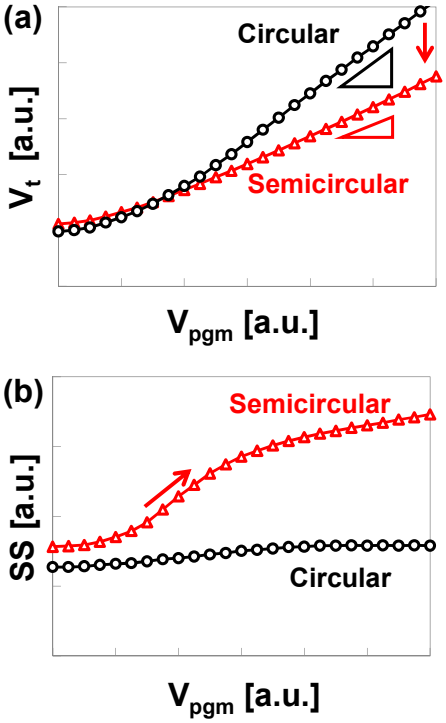

Fig. 8. Simulated program characteristics comparing circular and semicircular cells. (a) V_t and (b) SS.

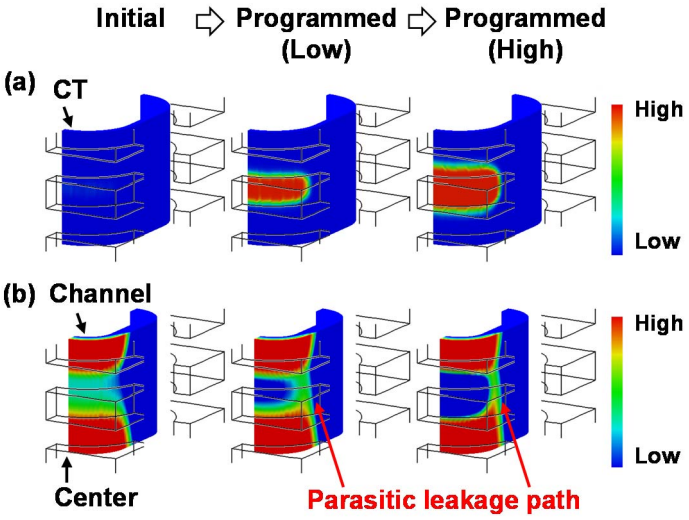

Fig. 9. (a) Simulated trapped electron density in the CT layer and (b) corresponding electron density in the channel at $V_{CG}=V_t$ of the initial state and programmed states of two different program voltages (Low/High).

Fig. 9 shows simulated trapped electron density in the CT layer and electron density in the channel when the CG voltage is equal to V_t. In the initial state with no trapped charge in the CT layer, the current path is formed at the center part of the channel. As the program state becomes higher, electrons are injected mainly at the center part of the CT layer and the current leakage path at the edge part manifests itself.

Based on the above observation, the mechanism of the program slope degradation is explained as follows. A semicircular cell transistor can be expressed as a parallel connection of a main transistor and a parasitic transistor due to fringe field effect as shown in Fig. 10(a). The main transistor has similar characteristics to a circular cell. The parasitic transistor has higher initial Vt and larger SS than the main transistor because of its thick gate dielectric, but it has extremely lower program slope since electrons are not injected around the parasitic transistor. As a result, the cell current and threshold voltage in the high program states are controlled by the parasitic transistor as shown in Fig. 10(b). Thus, the program slope of the semicircular cell is degraded.

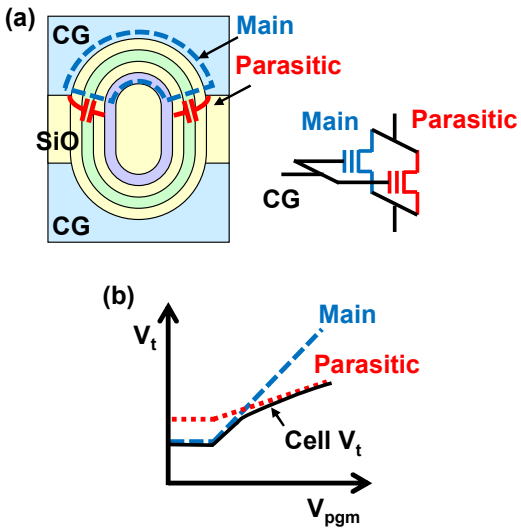

Fig. 10. (a) Cell transistor model in the semicircular cell expressed as a parallel circuit of a main part transistor and a parasitic part transistor. (b) Schematic explanation of program characteristics of a cell transistor, which is controlled by a parasitic transistor in high program states.

B. Program Slope Improvement by Initial Charge Injection

A technique called initial charge injection is proposed to raise the program slope by suppressing the current leakage in the parasitic transistor. Fig. 11(a) depicts the concept. Before normal program operation, a high program voltage is applied to inject electrons to wide part of the CT layer, then a relatively low erase voltage is applied to inject holes so that electrons are extinguished at the center part and localized near the CG edge. The amount of the localized electrons can be controlled by voltage and pulse time of the first program step and the subsequent erase step. The localized electrons switch off the parasitic transistor during subsequent program operation. Fig. 11(b) shows an example of simulated trapped electron density in the CT layer after the initial charge injection.

Fig. 12(a) shows the simulation results of program characteristics without initial charge injection and with initial charge injection of two different conditions, and Fig. 12(b) shows the simulated SS. In the high injection condition, remarkable improvement of the program slope and weaker dependence of SS on V_{pgm} are predicted. The program slope improvement with the initial charge injection is verified in experiments as shown in the previous report [4].

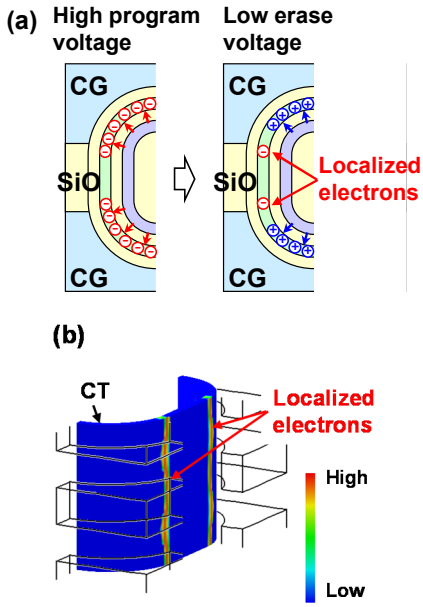

Fig. 11. (a) Procedure of initial charge injection. (b) Trapped electron density in the CT layer after initial charge injection.

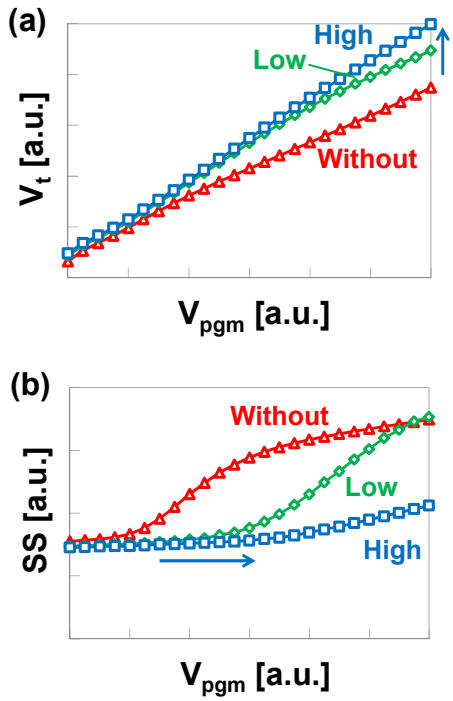

Fig. 12. Simulated program characteristics without initial charge injection and with initial charge injection of two different conditions (Low/High). (a) V_t and (b) SS.

V. SUMMARY

We have constructed a TCAD model to simulate program/erase characteristics of the 3D CT flash memory cells. The model was calibrated to the experiment with high accuracy. We studied the program characteristics of the novel semicircular cells through TCAD simulation and clarified that the current leakage path due to the parasitic transistor causes the program slope degradation. We demonstrated that the initial charge injection technique is effective to suppress the parasitic current leakage to improve the program slope of the semicircular cells.

ACKNOWLEDGMENT

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