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Predictive Compact Modeling of Abnormal LDMOS Characteristics Due to Overlap-Length Modification

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***Abstract*—Further compact-model development for LDMOS is reported, enabling concurrent device and circuit optimizations by only varying the ratio between gate-overlap length (L_{over}) and resistive-drift length (L_{drift}). Different from the conventional carrier-dynamics understanding within these two regions, LDMOS shows abnormal characteristics during such a ratio variation. The pinch-off condition occurs under the gate overlap region, and the pinch-off point is found to move along L_{over} with increased drain voltage, even under the accumulation condition. This means that carrier conductivity is no longer controlled by the gate voltage but by the drain voltage. The precise pinch-off condition is determined by the field balancing within gate-overlap and resistive-drift regions. The pinch-off length (ΔL) within L_{over} sustains V_{ds} together with L_{drift}. Thus, the pinch-off region contributes as a part of L_{drift} and improves the device's high-voltage applicability. A new model is developed to describe this balancing phenomenon analytically, where the key physical quantity is ΔL. The developed ΔL model considers the potential distribution along L_{over} together with L_{drift}. At the pinch-off point, the field induced by V_{gs} and that by V_{ds} are assumed to be equal, which derives an analytical description for ΔL. Evaluation results with the developed model are verified with 2D-numerical-device-simulation results.**

Keywords—power MOSFETs, LDMOS, compact model, overlap length, conductivity modulation

I. Introduction

LDMOS (lateral double-diffused MOS) [1] is widely used for power applications. A schematic LDMOS structure is depicted in Fig. 1a. It can be seen that the device consists of an intrinsic MOSFET and a long lightly-doped drift region with the length of L_{drift}, where most of the applied voltage is sustained. Additionally, the gate-overlap length, L_{over}, is relatively long, which controls the carrier flow together with the channel region. Geometrical dependence with L_{over} and L_{drift} varied were studied [2], [3]. This geometrical freedom would lead to an optimization of LDMOS for different voltage-rating, through varying the ratio of the conductive L_{over} and the resistive L_{drift}. For this device technology to be truly usable in actual circuit designing, a good compact model equipped with geometrical scaling capabilities is helpful. Measured I_{ds}-V_{gs} characteristics are shown in Fig. 1b, where L_{drift} is fixed to 0.4μm and L_{over} is varied from short to extremely long length. Though the measurements show conventional features for low V_{ds} for all lengths L_{over}, the I-V characteristics, especially in case of g_m, show no clear tendency as a function of L_{over}. Current-driving capability is kept high for relatively short L_{over}, which, however, reduces drastically for long L_{over}.

II. Analysis of Observed Phenomenon

Simulation experiments using 2D device simulator [4] were undertaken to analyze the measured results. Fig. 2a shows the results of the I_{ds}-V_{gs} characteristics, where L_{drift} was kept to 0.6μm and L_{over} was varied. The simulated set of structures reproduces the experimental features depicted in Fig. 1b. It can be seen that the I_{ds}-V_{gs} characteristics are identical in case of small V_{gs} for all L_{over} lengths. However, a drastic current reduction occurs with increased L_{over} length according to a V_{gs} increase, which can be recognized more clearly in the g_m curves. In summary, the long L_{over} devices show two specific features, as depicted in Fig. 2b. One is a drastic increase of the resistance effect, leading to a reduction of g_m, and the other is a recovery of this reduction, when V_{gs} is still further increased. Fig. 3 shows a parameter extraction result with the existing open-release version of the HiSIM_HV industry-standard compact model [5], which demonstrates that the observed abnormal device features cannot be reproduced. The reason for the first sharp peaks, observed in Fig. 2b, is due to the weak V_{gs}, which cannot induce the accumulation condition yet, so that the applied V_{ds} is mostly consumed at the channel/drain junction as demonstrated in Fig. 4. Once the accumulation condition is formed, the overlap region becomes conductive.

On the left side of Fig. 5, simulated carrier-density distributions of the current characteristics, shown in Fig. 2, are compared at fixed specific V_{gs} values. The corresponding potential distributions along the current-flow contour are depicted on the right side of Fig. 5 together with the injected carrier densities from the channel. Current flows away from the surface for the whole L_{over} region under low V_{gs} condition and thus the whole L_{over} region is under the pinch-off condition. A nearly flat potential distribution is observed for this case and most of the applied potential is consumed at the channel/drift junction. Thus, the pinch-off

region contributes as a highly resistive-drift region, together with L_{drift}. However, the current moves towards the surface as V_{gs} increases. With still further increased V_{gs}, carrier injection from the channel increases and the overlap region becomes conductive. The remaining resistive region stays in the pinch-off condition and acts as a part of L_{drift}.

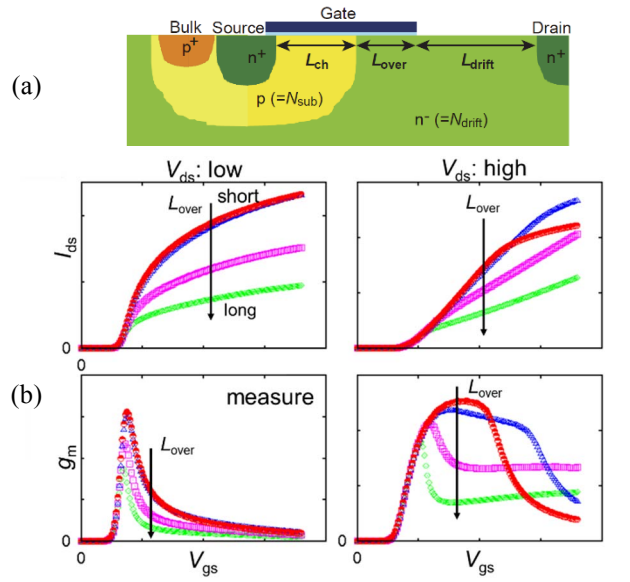

Fig. 1. (a) Schematic of LDMOS structure. (b) Measured I_{ds}-V_{gs} characteristics (upper) and g_m-V_{gs} characteristics (lower) for different L_{over} for low (left) and high (right) V_{ds}.

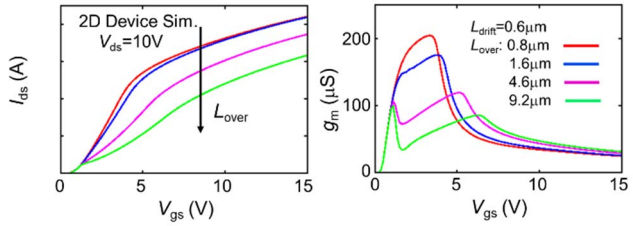

Fig. 2. 2D numerical device simulation results of I_{ds}-V_{gs} characteristics and g_m-V_{gs} characteristics for different L_{over} lengths.

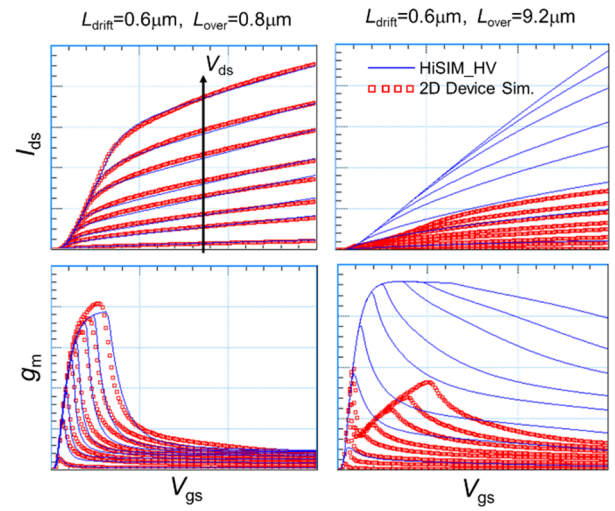

Fig. 3. Parameter extraction results with the industry-standard HiSIM_HV model. A single set of model parameters should predict L_{over} length scaling. For identical LDMOS devices (except for different L_{over} lengths), TCAD-generated data (red dots) of the device with shortest L_{over} were fitted. I_{ds}-V_{gs} and g_m-V_{gs} as a function of V_{ds}, are shown on the left to be reproduced well. However, for the longest L_{over} device, accurate representation of the characteristics failed with this extracted model parameter set, i.e., L_{over} scaling is not achieved.

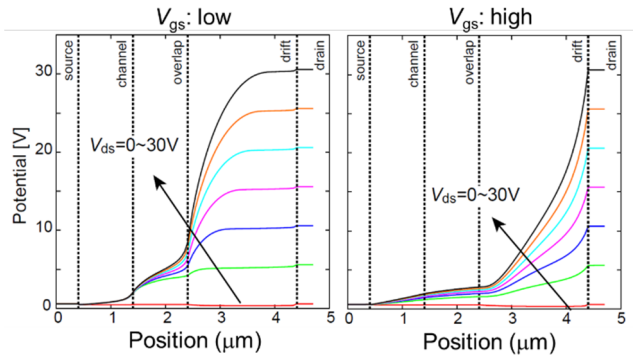

Fig. 4. Comparison of potential distribution along the device small V_{gs} (left) and for large V_{gs} (right).

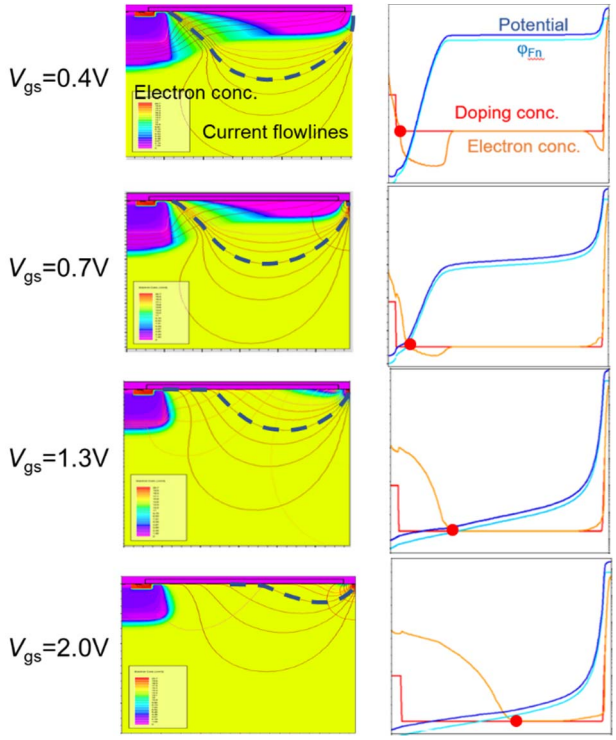

Fig. 5. 2D-device simulation results of (a) the current flow (left side) and (b) the potential as well as the electron-concentration distribution (right side) are compared for different V_{gs} values at V_{ds} =10V along the median current flowline (dashed lines in (a)). The median current flowline falls on the maximum current densities when the current density distribution is peaked and symmetrical around the peak. This is not the case when the distribution is skewed and hence not symmetrical around the peak. The high electron density refers the accumulation condition, which is observed more clearly for large V_{gs} values. The red circles denote an end point of accumulation, where electron concentration has decreased to the doping concentration.

Fig. 5 (left column) shows the maximum current-density path by dashed lines. It can be seen that weak gate control causes a deep current flow. This long way of the current flow increases the resistance effect. The depth of the current flow becomes shallower as V_{gs} increases, referring to a stronger accumulation condition. The main reason for the deep current flow is the pinch-off formation underneath the gate-overlap region in accordance with a diminished V_{gs} control, where no electrons exist (see red circles in the right column of Fig. 5). Since the applied voltage of V_{ds} =10V at the drain contact cannot be sustained only within the short L_{drift} region, the sustaining region extends even into the overlap region for small V_{gs}. As a result, the gate control

of the current flow is limited to only within the non-pinch-off region, where injected carriers from the channel prolong the path to the electrode. The details of the observed pinch-off feature are determined by the balancing of the two fields, induced within the conductive gate-overlap region and within the pinch-off region.

III. Modeling of ΔL and Verification

Our task here is to develop a compact model for the pinch-off length ΔL in the lightly-doped resistive region under the gate. The pinch-off occurs at the point where the gate-oxide field becomes equal to the lateral electric field, and thus the lateral electric field starts to dominate beyond this point. Since HiSIM_HV solves the potential distribution along the device iteratively, the key potential value V_{dp}, referring the end of the gate control, is known as demonstrated in Fig. 6 [5]. Here the potential distribution is approximated by a quadratic function within the drift region as

$$\phi = a\left(x + x_0\right)^2 + b \tag{1}$$

$$\begin{cases} a = \dfrac{\Delta V}{L_{\text{total}}^{\ 2} - L_0^{\ 2}} \\ b = V_{\text{dp}} - \dfrac{\Delta V \cdot x_0^{\ 2}}{L_{\text{total}}^{\ 2} - x_0^{\ 2}} \end{cases} \tag{2}$$

$$\begin{cases} \Delta V = V_{\text{ds}} - V_{\text{dp}} \\ L_{\text{total}} = L_{\text{over}} + L_{\text{dri}} \\ x_0 = L_{\text{over}} - \Delta L \end{cases} \tag{3}$$

An analytical equation for ΔL is derived as

$$\Delta L = L_{\text{over}} + \frac{\Delta V - \sqrt{\Delta V^2 + E_{\text{ov}}^{\ 2} L_{\text{total}}^{\ 2}}}{E_{\text{ov}}} \tag{4}$$

$$E_{\text{ov}} = \frac{\epsilon_{\text{ox}}}{\epsilon_{\text{si}} T_{\text{ox}}}\left(V_g - \phi_{\text{ov}} - c\right) \tag{5}$$

where E_{ov} is the field strength at the pinch-off point (x=0). The surface potential within L_{over} under the gate control ϕ_{ov} is also calculated by solving the Poisson equation iteratively, which determines the electric field within L_{over}. An adjustable parameter c denotes the threshold voltage of the accumulation start. Therefore, the field strengths can be calculated analytically. Thus the current equation within the drift region is written as

$$I_{\text{ddp}} = W_{\text{eff}} X_{\text{ov}} q N_{\text{drift}} \mu_{\text{drift}} \frac{V_{\text{ddp}}}{L_{\text{drift}} + \mathbf{RDRDL1} + \Delta L} \tag{6}$$

where W_{eff} is the device width, X_{ov} is the width of the current flow and μ_{drift} is the carrier mobility within the drift region [5]. As can be seen, the pinch-off length ΔL is treated as an extension of the length of the resistive region [5], and thus ΔL reduces the electric field within the drift region. HiSIM considers the continuity condition between the channel current I_{ds} and I_{ddp} to determine V_{dp} [5], [6].

The pinch-off length ΔL is calculated and compared with 2D device simulations results in Fig. 7. It can be seen from Eq. (6), that a large ΔL for small V_{gs} leads to an increased resistance effect. Agreement of the model calculation results to those of 2D device simulation is quite well. Slight deviation of the V_{gs} dependence might be caused by the quadratic approximation of the potential distribution for deriving the analytical description of ΔL. To compensate this approximation, a model parameter could be introduced to obtain better fittings.

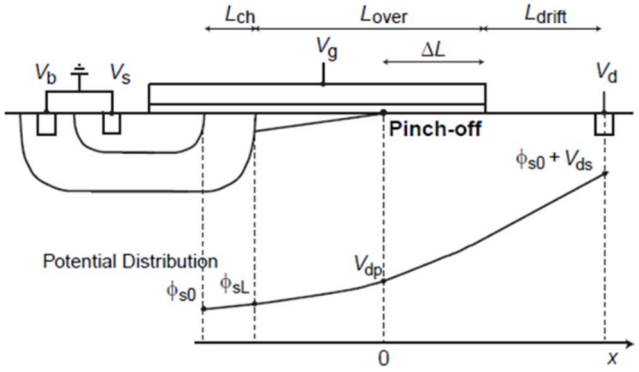

Fig. 6. Potential distribution along the device, as considered in HiSIM_HV. The internal-node potential V_{dp} refers the end of the gate control, namely, the pinch-off point for the presently studied case. Surface accumulation vanishes at the pinch-off point within the gate overlapped region.

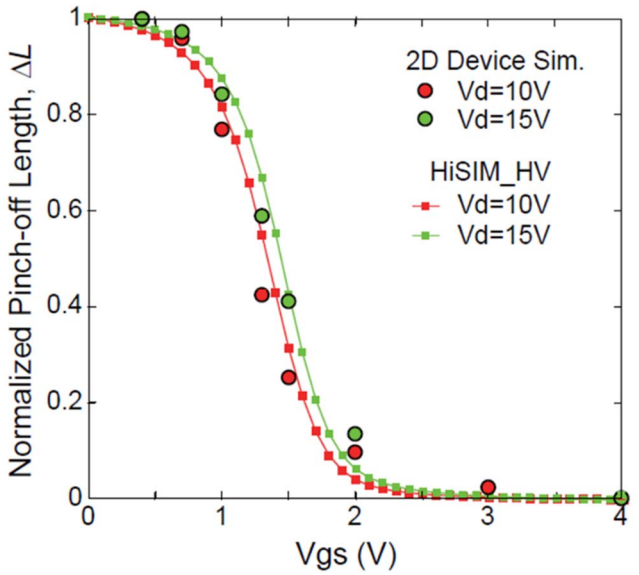

Fig. 7. Comparison of ΔL as extracted with 2D-device simulation and calculated with developed model. The 2D-device simulation results of ΔL are extracted as the points, where the vertical component of electric field turns to negative from positive. The developed model assumes a quasi 1D potential distribution along the device, into which the electron distribution along the depth direction is practically integrated. In spite of the

assumptions introduced for deriving the analytical formulation, agreement is acceptable.

Figs. 8a and b compare the model-calculated *I-V* characteristics and g_m with those of 2D-device simulation results. The model calculation is done only by introducing the ΔL values extracted in Fig. 7. The first sharp peak in g_m for small V_{gs} refers to the condition that ΔL is nearly equal to L_{over}. According to the V_{gs} increase, ΔL approaches to zero, resulting in a lowering of the resistance effect and the start of the g_m recovery. After ΔL becomes zero, only the carrier mobility within the drift region determines the feature as demonstrated in Figs. 8c and 8d. In particular, Fig. 8c clearly shows that drain current depletes from that for ΔL=0. However, it reverts to that for ΔL=0 at higher V_{gs}.

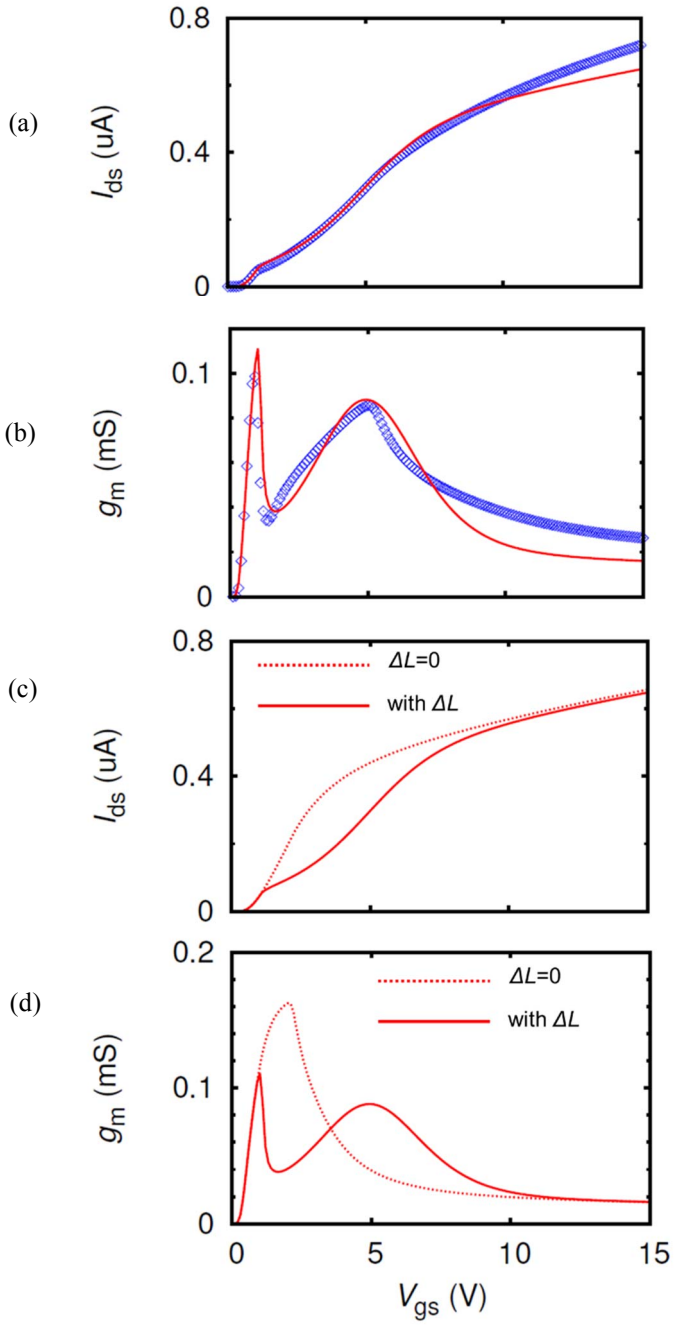

Fig. 8. Comparison of I-V characteristics between the developed model (red line) and 2D-device simulation (blue symbols). a) I_{ds}-V_{gs} and b) g_m-V_{gs}, at V_{ds}=10 V. The observed distinctive modulation in g_m, has been captured by the developed compact model, while in Fig.3 it was completely misrepresented using the industry-starndard HiSIM_HV model, where the developed model for the ΔL modulation is not yet included. c) I_{ds}-V_{gs} and d) g_m-V_{gs}, at V_{ds}=10 V, both with and without ΔL.

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