Verilog-A model for avalanche dynamics and quenching in Single-Photon Avalanche Diodes

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***Abstract*— We present a Verilog-A model accounting for the temporal avalanche buildup and its statistics in Single-Photon Avalanche Diodes (SPADs). This physics-based approach is compared to TCAD mixed-mode analyzing predictions, as well as measurements. The buildup that can be in the order of hundreds picoseconds, affects the statistical pulse width distribution, which is experimentally verified. Furthermore, we address in detail the voltage swing across the device during avalanche and its quenching, studying its impact on power consumption. This model can help a chip designer to optimize circuits for quenching the SPAD photodiode.**

Keywords*— *Silicon SPAD, avalanche dynamics, quenching circuits, Verilog-A code, TCAD.

I. INTRODUCTION

Single-Photon Avalanche Diodes (SPADs) are reverse-biased p-n junctions used in Geiger mode. In this regime and when a large voltage is applied, the electric field in the depletion layer becomes strong enough that the charge carriers may acquire sufficient energy to trigger an avalanche through impact ionization mechanisms. Hence, when an absorbed photon leads to a photo electron-hole pair generation, a measurable current rises swiftly and keeps flowing rendering the device insensitive to subsequent detections. Therefore, the avalanche must be stopped and the device brought to its quiescient state using ancillary readout electronics: this is the basic principle of quenching. Literature enumerates different types of quenching circuits for which a specific application is best-suited [1]. The passive version is the simpliest way which consists of a high-value quench resistor connected in series to the diode (Fig.1). SPADs were developed in the late sixties [2] and related Physics reviewed by Spinelli and Lacaita [3]. Nowadays, these devices are gaining popularity in automotive industry (Light Detection and Ranging systems [4]) and time-of-flight imaging [5].

In this work, we present a Verilog-A model to assess the SPAD buildup and its statistics. For accurate behavior description, we developed a Verilog-A diode model including the underlying physics and calibrated on Technology Computer Aided-Design (TCAD) solver [6]. The buildup rising time statistics impacts the output pulse width, which is confirmed by measurements, as discussed later. Additionally, we investigate the voltage swing on the SPAD sensing node and we confirm that its value can exceed the excess bias as it has already been demonstrated in [7]. Furthermore, this voltage swing directly affects the circuit power consumption.

The paper organization is as follows. After this general introduction, the Verilog-A model incorporating the physics of avalanche is described in Section II. Moreover, the empirical method for the electric field, reproducing TCAD simulations is outlined. Section III summarizes the main results: the current buildup statistics and its impact on the pulse width on the one hand, and the voltage swing on the sensing node affecting the power consumption, on the other hand. Then, the paper is concluded in Section IV.

II. MODEL DESCRIPTION

As stated previously, a SPAD is a transient behavioral device operating via the avalanche effect and utilizing the fact that a p-n junction can stay stable for a finite time above its breakdown voltage. A photon's arrival initiates a measurable current that increases reaching a peak value, until it is quenched using an ancillary circuit: the initial conditions are then restored. The choice of the quenching resistance R_Q and capacitance C_Q (from a modelling standpoint, we add the intrinsic capacitances of the SPAD, the sensing and quenching transistors, including also parasitic elements from circuit routing) is of a high importance, since it dictates the peak of current/voltage. We consider as a representative device a SPAD with a large collection volume as in [8]. The breakdown voltage at room temperature is of 17.1volts.

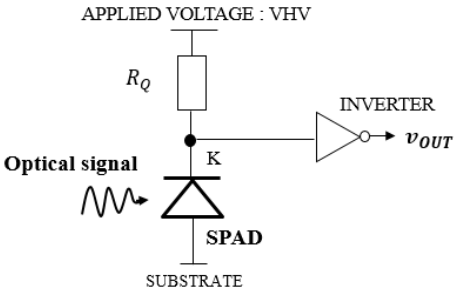


Fig. 1: The cathode terminal of the SPAD diode (sensing node) connected to a quench restor ($R_Q \sim 500\,K\Omega$). During the avalanche, a high generated current gives rise to a detectable swing of the cathode. The inverter allows a square output pulse and reflects the overall time constant of the circuit.

The currents I_e for electrons and I_h for holes follow:

$$\begin{cases} \frac{dI_e}{dt} = [M_e.I_e + M_h.I_h - I_e]/\tau_e & (1) \\ \frac{dI_h}{dt} = [M_e.I_e + M_h.I_h - I_h]/\tau_h & (2) \end{cases}$$

Where τ_i is the transit time and M_i the multiplication factor (i represents e for electrons and h for holes). When an electron-hole pair is created, a current $I_0 = \frac{q.v_s}{w}$ (v_s is the carriers saturation velocity, q the elementary charge and w the effective multiplication region width) can initiate the avalanche process. Hence, starting from the assumption that the total current I_T is the sum of both carrier types contributions ($I_T = I_e + I_h$), which is also a succession of ionizations: $I_T = I_0(1+M+M^2+M^3+...)$, it can be written in a more familiar way as: $I_T = \frac{I_0}{1-M}$ where $M = M_e+M_h$.

Theoretically, the coefficient M_i is given by:

$$M_i = \alpha_i . w_i \quad (3)$$

It depends on w_e and w_h [9], as well as on the electric field through the expression:

$$\alpha_i = a_i . exp\left(\frac{-b_i}{F}\right) \quad (4)$$

The ionization coefficients α_i describing the carriers multiplication and increasing with the electric field, express the mean rate of ionization per unit distance and can be also obtained by the inverse of the mean distance a carrier travels before an ionizing collision. a_i and b_i are parameters measured by van Overstraeten and de Man in [10] where different values are tabulated depending on the field ranges.

Regarding previous statements, an accurate estimation of the maximum electric field variation with the diode biasing is compulsory. Even though analytical models exist in certain simple cases (e.g. abrupt junction); we used for this study an empirical method that reproduces well-calibrated TCAD predictions on more complex SPAD architectures. This approximation is based on a polynomial exploiting the low and high field values.

Fig.2 reports the electric field evolution with the applied voltage where we compare the profile obtained by Verilog-A model to TCAD simulation. As can be seen, a change in the slope is observed at ~17V, which corresponds approximately to the breakdown voltage given by TCAD. This is a not surprising effect since it occurs when the device starts to deplete its collection volume with the increasing excess bias.

Once we calculate the ionization coefficients according to equation (4), we deduce the multiplication factor from equation (3).

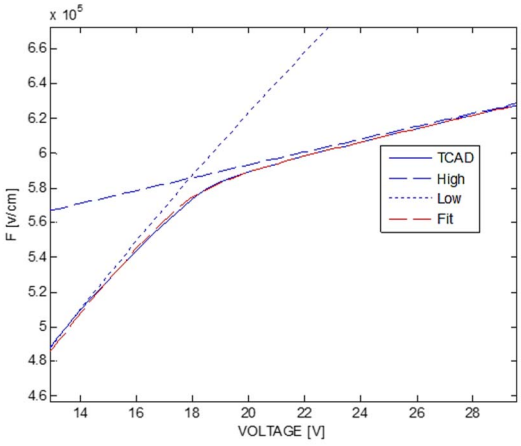


Fig. 2: The empirical model of the electric field (red dashed line) implemented in a Verilog-A code and expressed through a polynomial exploiting the high and low values of the field range. This model is calibrated on TCAD (solid).

Fig.3 illustrates M as a function of applied voltage VHV. When Adjusting the effective multiplication width for electrons at a value $w_e = 0.0736\ \mu m$ and for holes at $w_h = 0.092\ \mu m$ (fitting parameters), we obtain M=1 for a voltage V_B= 17.1 V (at 25°C) which corresponds to the experimental breakdown voltage. The dependence on temperature of the multiplication factor is also attested but in this paper we do not address particularly this issue.

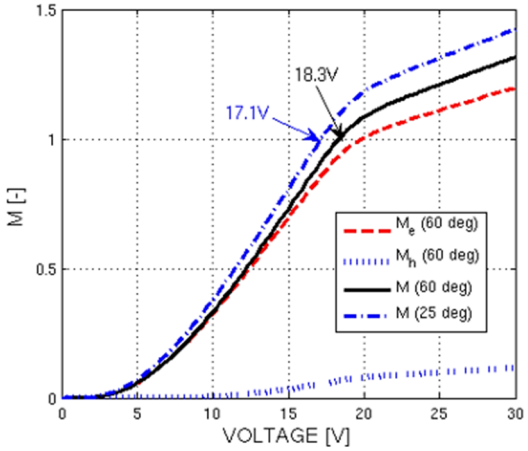


Fig. 3: The mean multiplication factor versus voltage, for two temperatures. M= 1 corresponds to V_B= 17.1 volts at 25°C.

III. SPICE SIMULATION RESULTS

A. *Modelling of the avalanche buildup time*

Using a Verilog-A code we describe the SPAD behavior. Studying the statistical buildup consists first in determining the conditions in which the device switches from the no-avalanche to the avalanche state (turn-on). In particular, the mechanisms that corroborate the triggering avalanche in SPADs are the photon arrival, the carrier generation and the release of some carriers after they had been captured by a trap in the depletion zone. The latter effect may cause an undesired breakdown event (the so-called afterpulsing phenomena, a major contributor to the Dark-Count Rate (DCR)).

Fig.4 (a) shows the SPAD current and voltage for various applied biasing (different curves refer to a bias increasing from V_B to V_B+5 volts) as a function of time. The buildup takes typically ~ $150ps$ at operational voltage (~20.5V) and can be even larger for lower biasing, which is in line with TCAD simulations (not shown in this paper). Furthermore, as we set a threshold current value (corresponding to the presence of a certain number of carriers in the depletion region) as a criterion for the breakdown event, in some biasing conditions the current does not build up which is also shown on the figure. This behavior occurs especially at low voltages where the electric field is not strong enough to enhance the triggering probability.

B. *Description of the quenching operation*

After the breakdown event, the bias voltage supply *VHV* exceeds the breakdown voltage V_B by an amount called the excess bias V_{EX} = *VHV* - V_B. The choice of V_{EX} is directly affecting the device performance. As the electric field increases with the excess bias, other SPAD's Figures-of-Merit -which are drived by the electric field- increases too (time-resolution or jitter, photon-detection probability (PDP), dark-count rate…etc).

Ultimately, the current reaches its maximum value and causes a voltage drop to the asymptotic steady-state mode: the SPAD is rearmed at the end of this regime. In parallel, the choice of R_Q and C_Q values defines the quenching time constant, which is a fundamental metric for the device performance as it limits the total number of detectable photons over one time period.

Fig.4 (c) shows the SPAD transient simulation using a Passive-Quenching Circuit (PQC). The anode current is plotted versus the SPAD cathode voltage. When the quenching circuit components have low values, it induces a non-quench behavior: the current is not completely brought below the triggering threshold and the device starts second avalanches.

C. The voltage swing on the sensing node

As soon as a photon impinges the SPAD surface, its the probability to trigger an avalanche is expressed through the Photon Detection Efficiency (PDE). Upon the detection, the device generates a current pulse and subsequent charges accumulate on capacitive components before they are drained out by the quenching resistance, which results in recharging the SPAD. However, the amount of accumulated charges enables a voltage swing during the avalanche on the SPAD sensing node. This issue is a new topic in the field of modelling and characterization of these devices. Reference [7] addresses in detail this phenomenon and some solutions are proposed to circumvent it, mainly through new design methodologies for preventing carriers overflow by controlling the total number of charges on the total capacitance of the SPAD sensing node. In our simulations and as can be noticed from Fig.4 (b), the voltage swing (that we denote V_{KMAX}) exceeds the excess bias by a factor ~1.4, (remember that the breakdown voltage is of 17.1volts and the excess bias is varying from 1 to 5 volts) which has also been recently reproduced in [7]. This is a drawback to minimizing the power consumption. In fact, an increase of V_{KMAX} results in a growth of the total charge of the SPAD.

Finally, Fig.4 (d) shows the output pulse v_{out} for different applied biasing. The pulse width reflects the circuit recovery time (recharge cycle).

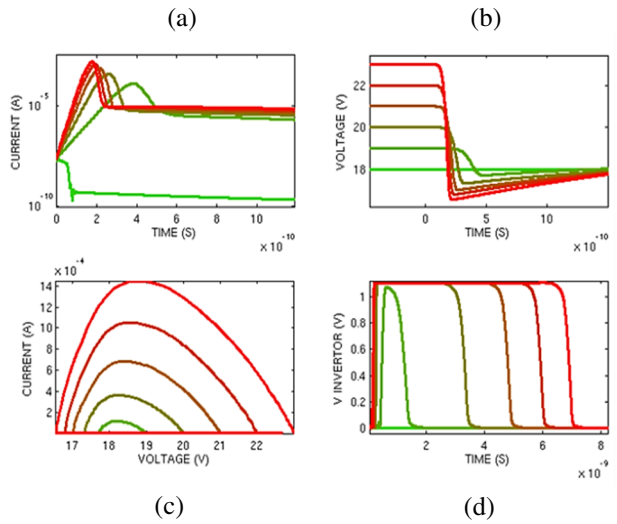


Fig. 4: (a) The current buildup evolution with applied voltage. (b) The voltage drop seen from the SPAD cathode exhibiting a swing. (c) SPAD I-V curve. The breakdown voltage is of 17.1 V (d) The output pulse v_{out}.

More importantly, the pulse width distribution (Fig. 5) which can be inferred from the statistics of the buildup dynamics itself, is accounted for using a statistical distribution of the ionization rates α_i . The modelling approach reproduces accurately the measurements.

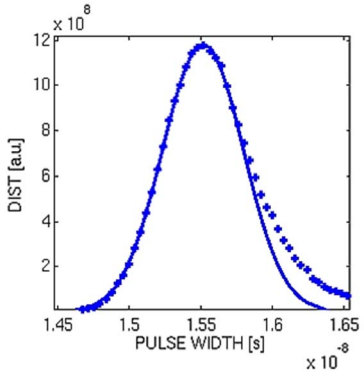


Fig. 5: The pulse width distribution. Solid curve refers to Verilog-A model; symbols to measurements (at VHV= 20.5V and T=60°C).

Furthermore, it is noted that the voltage swing V_{KMAX} affects the charge per pulse C_{PP} (reflecting the power consumption) since:

$$C_{PP} = C_K \,.\, V_{KMAX} \quad (5)$$

Where C_K is the total capacitive charge in the cathode node (including parasitic). Generally and for the sake of completeness, we recall that the transient behavior takes into account the parasitic capacitances modelling, as the total charge Q (which is given by the integral of the total current) is directly proportional to parasitic capacitive contribution. Reducing the latter leads to optimizing the power consumption and the quenching time.

To investigate theoretical Verilog-A model accounting for the swing voltage on the SPAD sensing node, we compare SPICE results to the approximation: $V_{KMAX} = VHV - V_B$ (standing for the excess bias). Results are illustrated in Fig.6 and feature the regime where V_{KMAX} exceeds the excess bias. The statement is then valid.

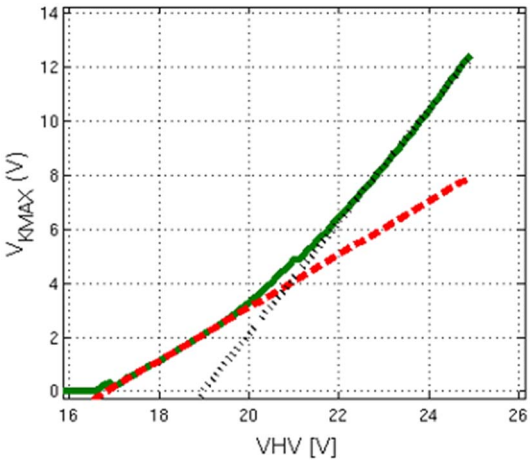
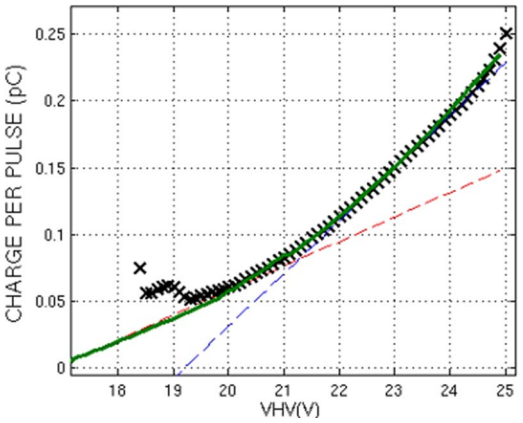
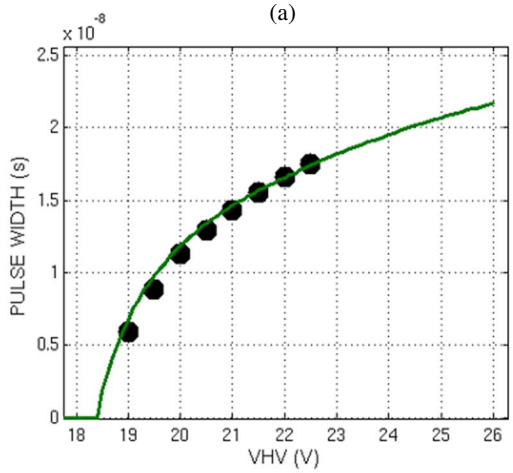


Fig. 6: (a) The swing voltage V_{KMAX} versus *VHV*. Verilog-A model (solid curve), V_{KMAX} = *VHV* - V_B (dashed line) and the regime where V_{KMAX} exceeds the excess bias (dotted line).

Fig.7 shows the charge per pulse and the pulse width as a function of *VHV* voltage: both not only depend on C_K, but also on the dynamics of the avalanche. It can be noticed at first sight that C_{pp} follows the two asymptotic regimes of V_{KMAX} demonstrated in Fig.6. SPICE simulation results reproduce accurately measurements. Therefore, the model can predict the power consumption on complex architectures.



(a)



(b)

Fig. 7: (a) The charge per pulse C_{PP} and (b) the pulse width versus VHV; Verilog-A model (solid line) versus measurements (symbols).

IV. CONCLUSION

We have developed a physics-based Verilog-A model for SPADs accounting for the buildup of the avalanche and its statistics. The model compares favorably with more complex TCAD mixed-mode predictions. Throughout this study, numerical results are confronted with characterization measurements: a good agreement is shown. Moreover, this model allows SPICE simulations of realistic circuits, including quenching and sensing transistors. It provides an accurate way to estimate qualitative outputs such as the power consumption, the voltage swing of the sensing node and the SPAD recovery time, which allow a chip designer to optimize circuits.

REFERENCES

[1] S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa, “Avalanche photodiodes and quenching circuits for single photon detection,” Applied Optics, vol. 35, no. 12, pp. 1956–1976, 1996.

[2] R. H. Haitz, “Model for the electrical behaviour of a microplasma,” J. Appl. Phys., vol. 35, no. 5, pp. 1370–1376, May 1964.

[3] A. Spinelli and A.L. Lacaita, “Physics and numerical simulation of Single Photon Avalanche Diodes,” IEEE transactions on electron devices, vol. 44, No. 11, pp. 1931-1943, November 1997

[4] I. Takai, H. Matsubara, M. Soga, M. Ohta, M. Ogawa, T. Yamashita, "Single-photon avalanche diode with enhanced NIR-sensitivity for automotive LIDAR systems", Sensors, vol. 16, no. 4, pp. 459, 2016.

[5] F. Mattioli Della Rocca, T. A. Abbas, N. A. W. Dutton and R. K. Henderson, "A high dynamic range SPAD pixel for time of flight imaging," 2017 IEEE SENSORS, Glasgow, 2017, pp. 1-3.

[6] Synopsys, Inc. Version O-2018.06, June 2018.

[7] Inoue, A., Okino, T.,Koyama, S., Hirose,Y, “Modeling and Analysis of Capacitive Relaxation Quenching in a Single Photon Avalanche Diode (SPAD) Applied to a CMOS Image Sensor”, Sensors 2020, 20, 3007.

[8] C. Veerappan and E. Charbon, "A Low Dark Count p-i-n Diode Based SPAD in CMOS Technology," in *IEEE Transactions on Electron Devices*, vol. 63, no. 1, pp. 65-71, Jan. 2016, doi: 10.1109/TED.2015.2475355.

[9] G.J.Rees and J.P.R David, “Nonlocal impact ionization and avalanche multiplication”. Journal of Physics D: Applied Physics, IOP Publishing, 2010, 43 (24), pp.243001.

[10] R. van Overstraeten and H. de Man, “Measurement of the Ionization Rates in Diffused Silicon p-n Junctions,” Solid-State Electronics, vol. 13, no. 1, pp. 583–608, 1970.