

6-5 Model analysis for effects of spatial and energy profiles of plasma process-induced defects in Si substrate on MOS device performance

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Abstract—This paper comprehensively discusses impacts of defect profiles in a Si substrate induced by plasma processing on MOS device performance. Both spatial and energy profiles of the defects considering practical plasma parameters were implemented into a conventional device simulation. Unique capacitance–voltage characteristics of MOS capacitors were obtained depending on the energy profiles, which shows good agreement with experimental results. The relationship between the defect profile and device parameter variation was clarified for n- and p-channel MOSFETs. The prediction results suggest the significance of precise control of spatial and energy profiles of defects for future MOS device design and fabrication.

Keywords—plasma process, plasma process-induced defect, defect profile, density-of-state, Si, MOSFET

I. INTRODUCTION

Plasma processing plays an essential role in manufacturing present-day scaled electronic devices [1]. In the fabrication of high-performance devices, suppressing unexpected impurities and defects is a primal concern for both classical and emerging devices. In particular, defects generated during plasma processes—plasma process-induced defects (PD)—have attracted interests in accordance with the device scaling [2]. The PD modifies physical properties of materials, which results in the degradation of device performance and reliability [2]. In the case of Si, the existence of PD changes the effective doping concentration and increases the junction leakage current [3]. The impacts of PD on device parameter variations have been studied in terms of the areal defect density [4]. In the present-day plasma processes, it is expected that PD shows various profiles depending on the process conditions employed for the fabrication of complicated fine structures [5]. However, there have been few reports on the effects of spatial and energy profiles of PD on the device performance. In this study, we performed model prediction for MOS devices with PD in Si substrates by taking into account various conceivable defect profiles. The assumed energy profiles of PD were verified by simulated and experimentally-obtained MOS capacitor characteristics. On the basis of this result, the effects of both spatial and energy profiles of PD on MOSFET performance were analyzed in detail.

II. MODEL ANALYSIS FRAMEWORK

A. Definition of PD profile in Si Substrate

In the course of etch processes, a Si substrate is exposed to plasma and defects are generated on the surface primarily due to ion bombardments. In MOSFETs, defect sites are created in the source/drain (S/D) extension region as shown in Fig. 1. The typical localized structures are displaced-Si atoms and interstitials, which play a role as carrier trapping and detrapping sites at an energy level E in the Si bandgap. Here, considering the group of individual defects, the PD profile $n_{\text{dam}}(x, E)$ is defined by,

$$n_{\text{dam}}(x, E) = n_{\text{dam}}(x) \cdot f_{\text{dam}}(E), \quad (1)$$

where $n_{\text{dam}}(x)$ is the depth profile of the defect density and $f_{\text{dam}}(E)$ is the normalized energy distribution function of the defect level—the energy profile of PD—in the Si bandgap.

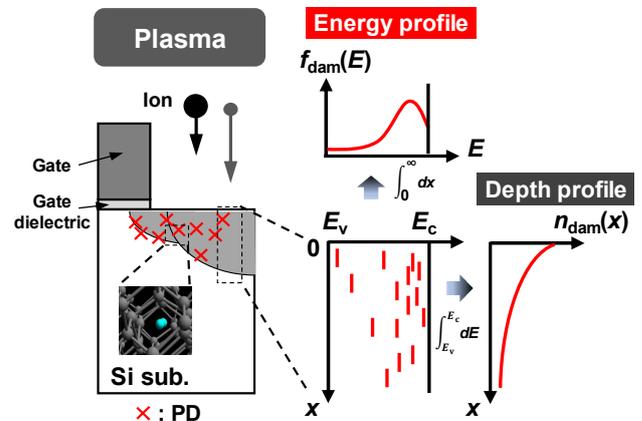


Fig. 1. Schematic illustration of a MOSFET structure with PD in the S/D extension region. PD profile is characterized by both depth $n_{\text{dam}}(x)$ and energy $f_{\text{dam}}(E)$ profiles.

B. PD profile model

The spatial profiles of PD exhibit an abrupt decrease along the depth depending on the projection range of injected ions. It was reported that the distribution tail of PD is significantly dependent on incident species and the energy [6,7]. First-principle calculations predicted various types of density-of-state (DOS) of local damaged structures, i.e. the energy profile, depending on the species inserted in the Si lattice [8]. In the present model analysis, several PD profiles were assumed to reproduce these features above.

The depth profile of PD $n_{\text{dam}}(x)$ was assumed to be an exponential distribution expressed by,

$$n_{\text{dam}}(x) = n_0 \exp\left(-\frac{x}{\lambda_{\text{dam}}}\right), \quad (2)$$

where n_0 is the peak density and λ_{dam} is the characteristic depth of defects. In this profile, the areal density of PD is $n_0 \cdot \lambda_{\text{dam}}$. For the energy profile of PD $f_{\text{dam}}(E)$, three profiles: (A)(B) Boltzmann-type and (C) Gaussian-type distributions were assumed as shown in Fig. 2. Profiles (A) and (B) indicate the cases that the major portion of defects is located close to the conduction or valence bands, respectively. Profile (C) corresponds to the case that the DOS has a local maximum value in the bandgap, which is defined by the average energy level \bar{E} and the variance σ_E .

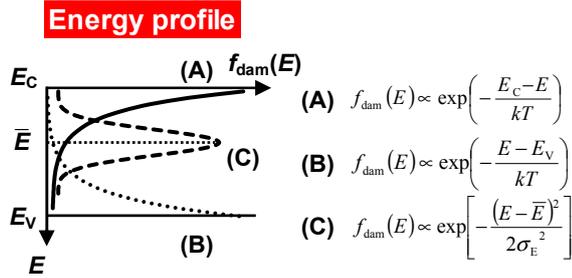


Fig. 2. Energy profiles $f_{\text{dam}}(E)$ of PD and their mathematical expressions implemented in the model analysis in this study.

C. Simulation methodology

Device simulations for MOS device performances were carried out solving carrier transport equations in the drift-diffusion approximation with density gradient quantum corrections [9]. The interface traps between Si and a gate dielectric film were also considered, while the trapped and fixed charges in the gate dielectric bulk were neglected.

III. VERIFICATION OF ENERGY PROFILES OF PD USING CAPACITANCE-VOLTAGE CHARACTERISTICS OF MOS CAPACITOR

MOS capacitors with PD on a p-type Si substrate are focused on. The dopant concentration and effective oxide thickness (EOT) are $1 \times 10^{18} \text{ cm}^{-3}$ and 7 nm, respectively. The depth profile of PD is fixed ($n_0 = 2 \times 10^{19} \text{ cm}^{-3}$, $\lambda_{\text{dam}} = 6 \text{ nm}$). Figures 3(a) and (b) show the predicted modulation frequency f_{mod} dependent $C-V$ curves assuming the profile (A) and (B) with respect to the energy profiles of PD, respectively. f_{mod} dispersions of the $C-V$ curves in the vertical and horizontal directions are observable. This feature is attributed to the change in the f_{mod} -dependent activated defect density and the formation of a shallow n-p junction. Figure 3(c) shows the low- f_{mod} $1/C^2-V$ curve assuming the profile (C) ($E_c - \bar{E} = 0.7 \text{ eV}$ and $\sigma_E = 0.2 \text{ eV}$). A characteristic hump is observable in the depletion region due to the presence of defects located at the deep levels near the mid-gap. Figures 3(d), (e), and (f) show the experimental $C-V$ and $1/C^2-V$ curves of damaged devices after Ar, SF_6 or HBr/O_2 plasma exposure, respectively. The characteristic deviations predicted by the model prediction are seen under the process gas conditions. These results confirm the validity of the energy profiles of PD assumed in the model analysis.

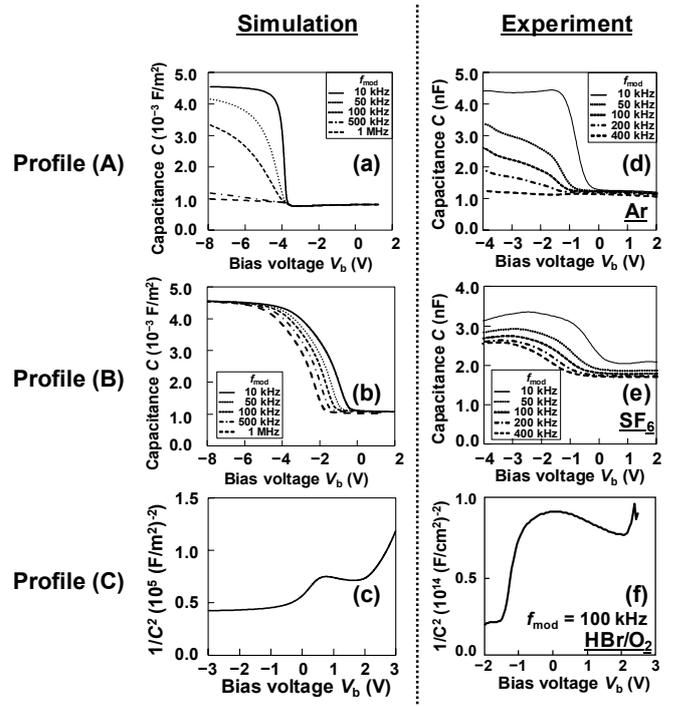


Fig. 3. Simulated $C-V$ curves of MOS capacitors assuming (a) profile (A), (b) profile (B), and (c) profile (C). Experimental $C-V$ curves of damaged devices exposed to (d) Ar, (e) SF_6 , and (f) HBr/O_2 plasmas [10].

IV. PREDICTION OF DAMAGED MOSFET CHARACTERISTICS

A. Effects of spatial profiles of PD

45-nm bulk MOSFETs containing PD are considered to investigate the effects of the spatial profile of PD. EOT is 1.5 nm and the substrate doping is $1 \times 10^{18} \text{ cm}^{-3}$. The peak concentrations of the S/D, S/D extension, and halo regions are 1×10^{20} , 1×10^{19} , and $1 \times 10^{18} \text{ cm}^{-3}$, respectively. Figure 4 shows the I_d-V_g curves at the drain voltage $|V_d| = 0.05 \text{ V}$ in the case of n- and p-channel MOSFETs assuming the energy profile (A) with various λ_{dam} ($n_0 = 1.5 \times 10^{19} \text{ cm}^{-3}$). A device without PD is denoted as Ref. The threshold voltage shift ΔV_{th} and the on-current variation were observed mainly due to the modification of the effective doping profile. A sharp contrast in the parameter variations is seen between n- and p-channel devices. These features become remarkable with an increase in λ_{dam} . In the case of the profile (B), in contrast to the profile (A), V_{th} shifts to the positive direction.

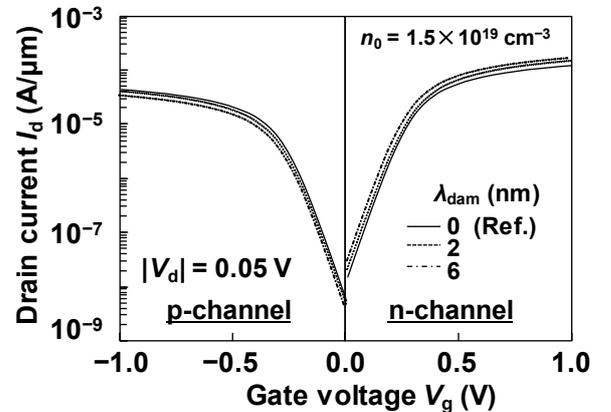


Fig. 4. Simulated I_d-V_g characteristics for n- and p-channel MOSFETs assuming the energy profile (A) with various λ_{dam} .

Figure 5 summarizes the n_0 and λ_{dam} dependences of ΔV_{th} assuming the profile (A) for n-channel MOSFETs. V_{th} is defined at $I_{\text{d}}(V_{\text{th}}) = 10^{-6}$ A/ μm . It was found that the device characteristics significantly depend on the depth profiles even when the total amount of PD is constant. This result implies that design and control of the depth profiles of PD in response to doping profiles are indispensable to improve the device performance.

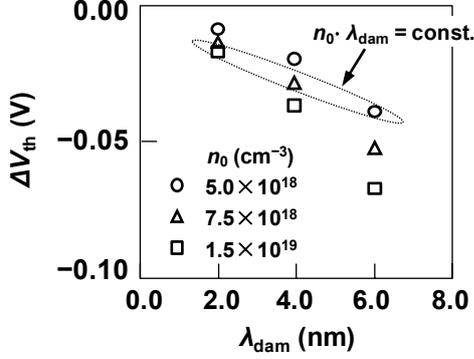


Fig. 5. Simulated ΔV_{th} as a function of λ_{dam} for n-channel MOSFETs assuming the energy profile (A) with various n_0 .

B. Effects of energy profiles of PD

32-nm FD-SOI MOSFETs with PD are focused on to investigate the effects of the energy profile of PD. EOT is 1.2 nm, and the thicknesses of the Si body and buried oxide are 7 and 20 nm, respectively. The peak concentration of the S/D region is 5×10^{19} cm^{-3} , while the channel is weakly doped (1×10^{15} cm^{-3}). The depth profile of PD is fixed ($n_0 = 1 \times 10^{19}$ cm^{-3} , $\lambda_{\text{dam}} = 5$ nm). Figure 6 shows the $I_{\text{d}}-V_{\text{g}}$ curves at $|V_{\text{d}}| = 0.05$ V for n- and p-channel MOSFETs assuming two energy profiles of PD. In addition to ΔV_{th} and on-current variation, off-leakage current I_{off} increases in the profile (C) in comparison with the profile (A). This feature is attributed to the carrier generation and recombination by PD located near the middle of the Si bandgap.

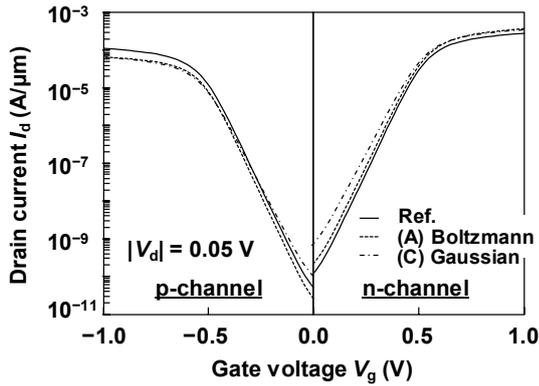


Fig. 6. Simulated $I_{\text{d}}-V_{\text{g}}$ characteristics for n- and p-channel MOSFETs assuming two energy profiles of PD.

Figure 7 shows the \bar{E} dependences of I_{off} assuming the profile (C) ($\sigma_{\text{E}} = 0.2$ eV) for n- and p-channel MOSFETs. As the \bar{E} lowers toward the mid-gap, i.e. the portion of defects at deeper levels increases, the I_{off} value drastically increases for both n- and p-channel devices. This result implies that the precise control of the energy profiles of PD

as well as the reduction of defect density is key to reduce the power consumption of damaged MOSFET devices.

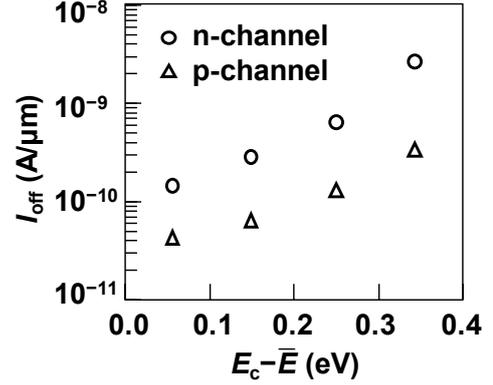


Fig. 7. Simulated I_{off} as a function of $E_{\text{c}} - \bar{E}$ assuming the energy profile (C).

V. CONCLUSION

We clarified by model predictions that the spatial and energy profiles of defects created during plasma processes have significant impacts on MOS device performances. It was found that the defects at deep levels in the Si bandgap degrade the subthreshold characteristics of damaged MOSFETs. Present findings imply that the consideration of the presence of PD after plasma processes is indispensable for designing future high-performance devices.

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REFERENCES

- [1] H. Abe, M. Yoneda, and N. Fujiwara, "Developments of Plasma Etching Technology for Fabricating Semiconductor Devices," *Jpn. J. Appl. Phys.*, vol. 47, pp. 1435–1455, 2008.
- [2] K. Eriguchi, "Defect generation in electronic devices under plasma exposure: Plasma-induced damage," *Jpn. J. Appl. Phys.*, vol. 56, pp. 06HA01, 2017.
- [3] Y. Sato, S. Shibata, K. Urabe, and K. Eriguchi, "Evaluation of residual defects created by plasma exposure of Si substrates using vertical and lateral pn junctions," *J. Vac. Sci. Technol.*, vol. B38, pp. 012205, 2019.
- [4] K. Eriguchi, Y. Nakakubo, A. Matsuda, Y. Takao, and K. Ono, "Plasma-Induced Defect-Site Generation in Si Substrate and Its Impact on Performance Degradation in Scaled MOSFETs," *IEEE Electron Device Lett.*, vol. 30, pp. 1275–1277, 2009.
- [5] V. M. Donnelly and A. Kornblit, "Plasma etching: Yesterday, today, and tomorrow," *J. Vac. Sci. Technol.*, vol. A31, pp. 050825, 2013.
- [6] T. Ohchi *et al.*, "Reducing Damage to Si Substrates during Gate Etching Processes," *Jpn. J. Appl. Phys.*, vol. 47, pp. 5324–5326, 2008.
- [7] M. Fukasawa *et al.*, "Structural and electrical characterization of HBr/O₂ plasma damage to Si substrate," *J. Vac. Sci. Technol.*, vol. A29, pp. 041301, 2011.
- [8] Y. Yoshikawa and K. Eriguchi, "First-principles predictions of electronic structure change in plasma-damaged materials," *Jpn. J. Appl. Phys.*, vol. 57, pp. 06JD04, 2018.
- [9] T. Toyabe, "Two and Three Dimensional MOSFETs Simulation with Density Gradient Model", Proc. SISPAD, pp. 279, 2004.
- [10] T. Hamano, K. Urabe, and K. Eriguchi, "Investigation of spatial and energy profiles of plasma process-induced latent defects in Si substrate using capacitance–voltage characteristics," *J. Phys. D*, vol. 52, pp. 455102, 2019.

