6-4 A TCAD Framework for Assessing NBTI Impact Under Drain Bias and Self-Heating Effects in Replacement Metal Gate (RMG) p-FinFETs

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***Abstract*— Sentaurus TCAD is enabled to calculate interface trap generation (ΔN_{IT}) during Negative Bias Temperature Instability (NBTI) under drain bias (V_D) and self-heating (SH) effects. The setup is calibrated with pure NBTI (V_D=0V) experimental data, and is further used to determine the NBTI component during Hot Carrier Degradation (HCD) stress. Such decomposition of NBTI and HCD is demonstrated for multiple fin length (FL) p-FinFETs to model HCD experimental data at different V_G/V_D stress.**

Keywords— FinFET, HKMG, BTI, SH, Fin length variation

I. INTRODUCTION

NBTI [1] and HCD [2], [3] are the key issues that impact reliability of advanced FinFETs [4]. Although a digital circuit (Fig.1) can suffer from BTI and HCD of both FETs, the BTI for NFET (Positive BTI) is negligible in modern FinFETs [4]. As per the standard practice, BTI and HCD are evaluated at device level during technology development, compact models are developed and are calibrated with measured data, and circuit simulations are done with calibrated compact models. The worst-case HCD mode for FinFETs is at V_G=V_D stress. While NFETs are only impacted by HCD, PFETs are impacted by both NBTI and HCD in this stress condition. It is important to isolate their contribution to aid compact model development. The presence of SH effect in FinFETs, due to increased phonon confinement and less heat dissipation area [5], [6] further complicate this effort.

II. SCOPE OF WORK

Our earlier TCAD framework for pure NBTI for V_D=0V [7], [8], is enhanced to simulate non-zero V_D values. The pure NBTI framework is calibrated with experimental data, and the resulting setup is used to estimate NBTI contribution under non-uniform carrier density and electric field along the channel together with local T rise near drain due to SH effect. It is shown that ΔN_{IT} distribution is non-uniform along the channel (higher ΔN_{IT} near the source end), and transfer I-V sweeps are needed to calculate its impact on threshold voltage shift (ΔV_T). The usual electrostatic approach using average ΔN_{IT} is shown to be invalid for non-uniform ΔN_{IT} distribution under non-zero V_D. Careful decomposition of NBTI and pure HCD are demonstrated across multiple FL p-FinFETs.

III. FRAMEWORK

Sentaurus Process and Device TCAD [9] are used respectively for structure generation and NBTI simulation. The Reaction-Diffusion model (RDM) is incorporated in Sentaurus Device to calculate interface traps Capture-Emission Depassivation (CED) and Multi-State Configuration (MSC) frameworks [7]. MSC model (Fig.2) deals with breaking of X-H bonds at the channel/oxide interface and Y-H bonds inside gate oxide bulk, (the exact chemical nature of electrically active defects is debated, hence generic states are used) and resulting diffusion of atomic H and molecular H_2 species. CED model (Fig.3) handles forward reaction (k_{F1}) of X-H bond dissociation, which depends on inversion hole density and vertical field, *i.e.*, V_G (and also V_D when applicable) and temperature (T), which includes ambient and SH effect (when applicable). It also depends on mechanical stress coming from raised S/D epi of the FinFET and hence FL (Fig.4), the strain alters the hole bandstructure [7], [8]. All other reaction parameters and diffusivities (Fig.2) are only T activated. The 3-D FinFET is simulated with a backend of 1µm (Fig.4), the latter is necessary for H_2 diffusion. 2D cross-section of the gate stack is also shown depicting IL, High-K, TiN cap, and Tungsten (backend) layers to make it realistic as actual measured device.

IV. NBTI CALIBRATION

Pure NBTI setup is calibrated first. However, the as-measured ΔV_T during NBTI stress is influenced by hole trapping (ΔV_{HT}) and bulk trap generation (ΔV_{OT}) in addition to interface traps (ΔV_{IT}) [10]. Hence, the BTI Analysis Tool (BAT) [10] is used to isolate these and obtain the dominating (primary) component which is ΔV_{IT} due to ΔN_{IT} (Fig.5). The time kinetics of measured ΔV_T at various V_G and T is typically calibrated [10], [11]. Fig.6 shows the modelling of experimental time kinetics of ΔV_T at few V_G and T for fixed FL. Fig.7 shows that of ΔV_T versus V_G at different FL but fixed T, the underlying subcomponents are also shown for the smallest FL. Fig.8 shows the comparison of ΔN_{IT} time kinetics extracted from BAT (symbols) and calibrated pure-NBTI TCAD (lines). Fixed time ΔN_{IT} versus V_G at fixed T (Fig.9 (a)) and versus T at fixed V_G (Fig.9 (b)) are compared for BAT extraction (symbols) and calibrated TCAD (lines). Data in Fig.7 through Fig.9 are shown for different FL. ΔN_{IT} reduces at lower FL due to compressive stress [8], [12].

V. DRAIN BIAS AND SELFHEATING

The above calibrated TCAD deck is used under V_D to evaluate the generation of traps. Non-zero V_D would reduce inversion hole density and vertical field near drain. This in turn would reduce ΔN_{IT} distribution towards the drain, shown in Fig.10 when the SH effect is switched off. However, the SH effect induced T increase in the fin (Fig.11) should be invoked as NBTI is T activated. The thermal resistances of the contacts are calibrated for proper estimation of SH effect induced T rise [5]. SH results in higher ΔN_{IT} magnitude near

source compared to pure NBTI (Fig.12), but a smaller ΔN_{IT} distribution towards the drain compared to the no SH effect case of Fig.10, when V_D is applied. The shape of average ΔN_{IT} time kinetics does not change without and with SH as V_D is applied, and stays the same as pure NBTI (Fig.13 (a)). However, the average ΔN_{IT} magnitude monotonically reduces at higher V_D when SH is not invoked, but a turn-around is seen with SH (Fig.13 (b)).

VI. Impact of Localized ΔN_{IT}

Average ΔN_{IT} is sufficient to use for ΔV_{IT} (=q.$\Delta N_{IT}/C_{OX}$, where C_{OX} is gate capacitance) for pure NBTI as defects are uniform [7]. This is invalid for the case of localized ΔN_{IT} distribution, since average ΔN_{IT} underestimates ΔV_{IT} when compared to that from transfer I-V sweeps before and after NBTI (Fig.14). ΔV_{IT} under different V_G and V_D space for 20nm and 60 nm FL FinFETs are shown respectively in top and bottom panels of Fig.15. These are used to calibrate a compact model (CM) for NBTI, details of which are in [3]. The calibrated CM is further used to decouple NBTI and pure HCD contributions in experiments. Fig.16 shows ΔV_T for measured HCD and modeled subcomponents for 20nm FL device (top panel) where HC is hot carrier degradation (using CM in [3]), IT is from BTI interface trap generation (shown in Fig.15), HT is hole trapping. Fig 16 bottom panel shows the same for the 60nm FL device. Fig 17 shows the time kinetics of measured ΔV_T at different V_G and V_D conditions, for (a) low FL and (b) high FL devices. Note the BTI is being computed from the TCAD shown in Fig 15. Detailed modeling details are mentioned for various V_G and V_D is discussed in [3].

VII. Conclusion

TCAD simulation of NBTI under V_D and SH effect is necessary for proper decomposition of experimental HCD data into pure HCD and NBTI components. Although NBTI should reduce under non-zero V_D due to reduction in vertical field near drain, SH effect increases T and arrests the amount of reduction in modern FinFETs. Non-uniform ΔN_{IT} with higher value near the source results in underestimation of ΔV_T when calculated by average ΔN_{IT} based charge impact, and transfer I-V sweeps are necessary. Properly decomposed NBTI and HCD contributions are necessary for compact model calibration and circuit analysis.

Acknowledgment: Narendra Parihar for NBTI measurements, KaranSingh Thakor and Ravi Tiwari for pure NBTI TCAD framework.

VIII. Reference

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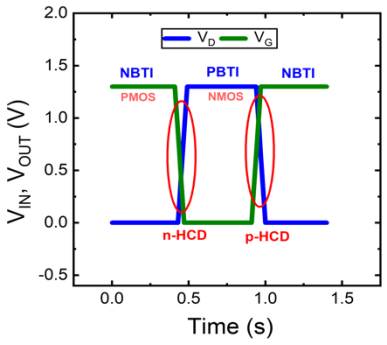

Fig.1. Time dependence of V_G and V_D and degradation mechanism in RO.

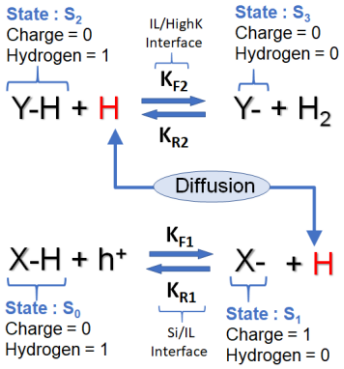

Fig. 2 MSC-HCD TCAD framework for interface trap generation. k_{F1} is bond dissociation rate and comes from CED model. Details in [7].

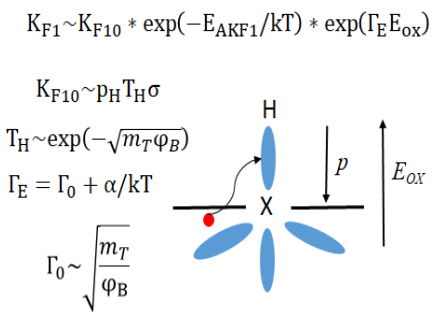

Fig. 3. Schematic of Si-H bond dissociation at the channel/IL interface. Inversion layer holes tunnel into interfacial Si-H bonds aided by the oxide electric field (E_{OX}).

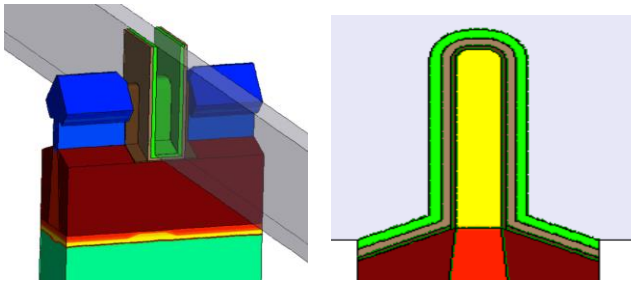

Fig. 4 (a) Isometric view of a 3D p-FinFET structure (FL = 20nm,) having raised epitaxial SiGe S-D and lateral Tungsten backend for H_2 diffusion. (b) 2D cross section of the fin showing IL, High-K, TiN cap and Tungsten layers in the gate stack

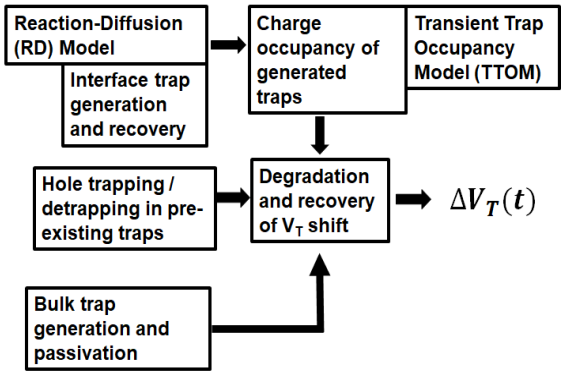

Fig. 5. Schematic of a BAT (BTI Analysis Tool) framework consisting of uncorrelated ΔV_{IT}, ΔV_{HT} and ΔV_{OT} components.

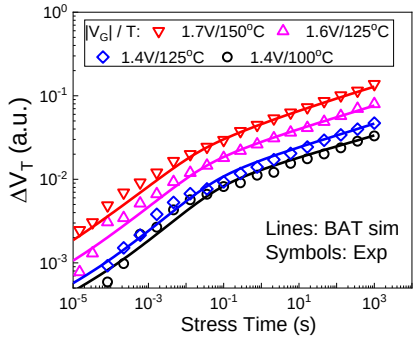

Fig. 6. Time evolution of ultrafast (10µs) measured ΔV_T for DC stress with model estimation at multiple V_G and T for FL 20nm.

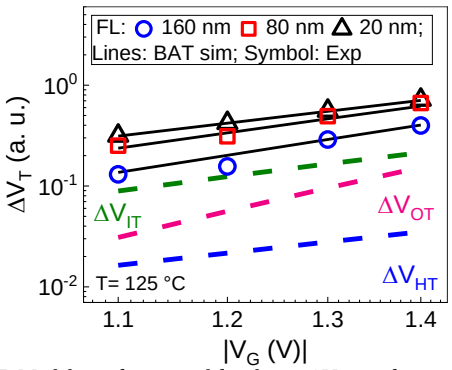

Fig. 7. Modeling of measured fixed time ΔV_T as a function of V_G for a fixed T for different FL. Sub-components of overall ΔV_T for FL 20 nm is shown.

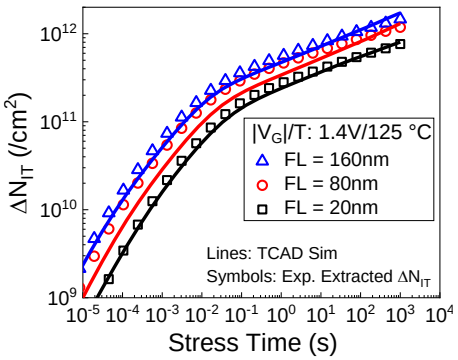

Fig. 8. TCAD modeling of BAT extracted ΔN_{IT} stress time kinetics for different FL for fixed V_G and T conditions.

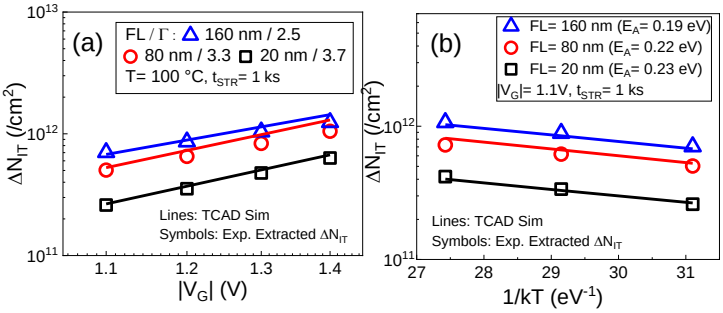

Fig. 9. (a) Fixed time ΔN_{IT} as a function of V_G is shown for a fixed T, (b) plots fixed time ΔN_{IT} as a function of T for a fixed V_G for different FL. Symbol: BAT extracted; Lines: TCAD

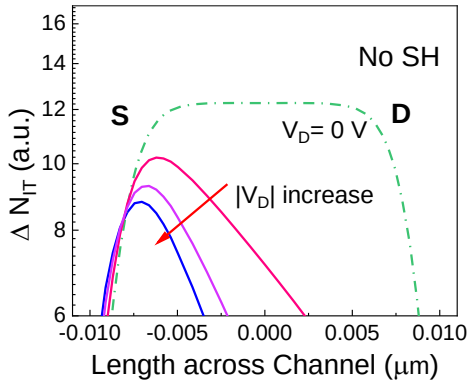

Fig. 10. Spatial distribution of ΔN_{IT} across the channel with varying V_D without SH. It shows the reduction of ΔN_{IT} due to decrease in vertical field (responsible for BTI) as V_D increase. Source (S) and Drain (D) side are marked.

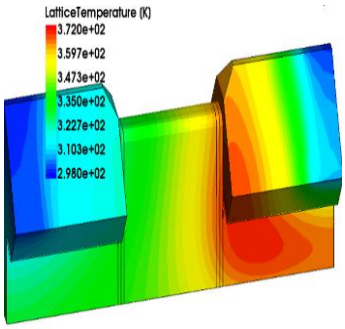

Fig. 11. 3D Lattice Temperature Profile along the channel in presence of V_D. Due to SH localized temperature rise at the drain side.

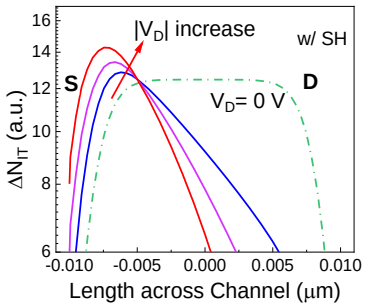

Fig. 12. Spatial distribution of effective ΔN_{IT} across the channel with varying V_D with SH. Source (S) and Drain (D) side are marked.

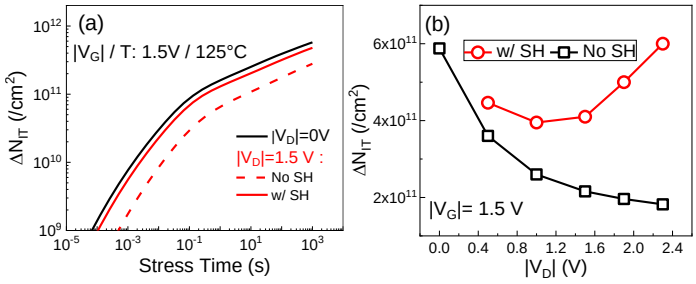

Fig. 13. (a) TCAD extracted ΔN_{IT} time kinetics for different V_D and (b) fixed time ΔN_{IT} as a function of V_D, with and without SH, at fix V_G.

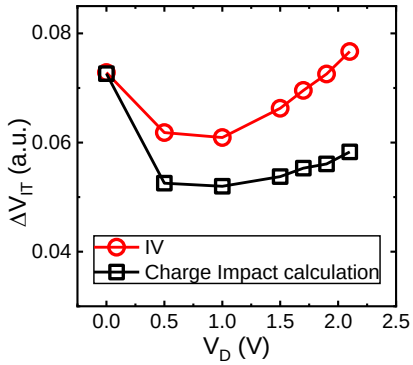

Fig. 14. ΔV_T using avg. N_{IT} and transfer IV under NBTI stress as a function of V_D. Note that charge impact calculations are not valid due to localized trap generation under non-zero V_D. Post stress IV is needed for degradation calculations.

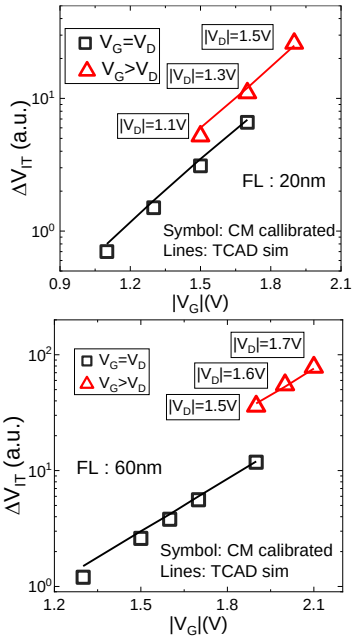

Fig. 15. Fixed time ΔV_{IT} simulated using TCAD under different stress bias (V_G and V_D) for FL of 20nm (top) and 60nm (bottom).

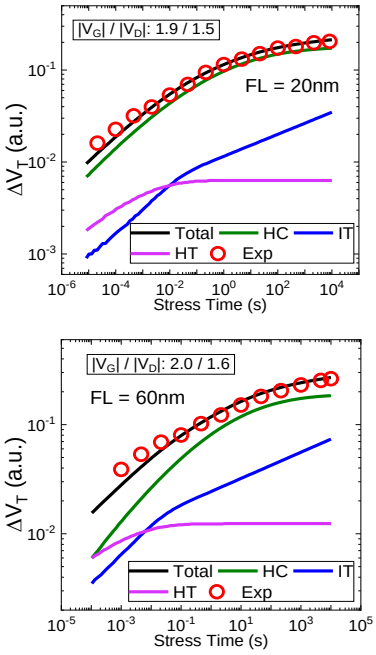

Fig. 16. Overall ΔV_T under V_G>V_D stress for FL of 20nm (top) and 60nm (bottom). ΔV_{IT} kinetics is simulated using TCAD for NBTI with SH. Symbols: Exp Data; Lines: Simulation

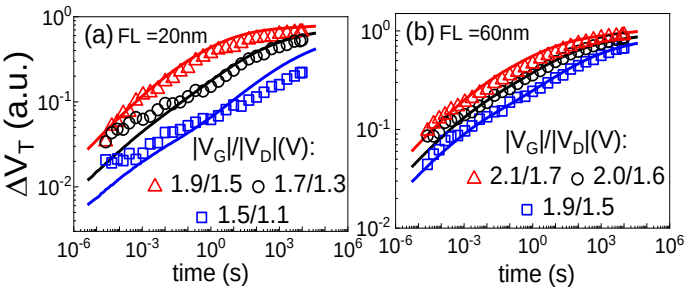

Fig. 17. Time kinetics of measured and modeled ΔV_T at different stress V_G/V_D conditions, for (a) FL= 20 nm and (b) FL= 60 nm devices. Symbols: data, lines: model.