6-1 Universal Feature of Trap-Density Increase in Aged MOSFET and Its Compact Modeling

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***Abstract*—Our investigation focuses on accurate circuit aging prediction for bulk MOSFETs. A self-consistent aging modeling is proposed, which considers the trap-density N_{trap} increase as the aging origin. This N_{trap} is considered in the Poisson equation together with other charges induced within MOSFET. It is demonstrated that a universal relationship of the N_{trap} increase as a function of integrated substrate current, caused by device stress, can describe the MOSFET aging in a simple way for any device-operating conditions. An exponential increase with constant and unitary slope of the N_{trap} is found to successfully predict the aging phenomena, reaching a saturation for high stress degradation. The model universality is verified additionally for any device size. Comparison with existing conventional aging modeling for circuit simulation is discussed for demonstrating the simplifications due to the developed modeling approach.**

***Keywords*—MOSFET aging/reliability, Trap-density increase, channel-length dependence, compact model, aging simulation**

I. INTRODUCTION

Circuit-reliability prediction requires several different simulation processes and tools to cover the whole range of chip development, from device-level to circuit-level aging. Such tools contain aging models, which are implemented in these tools separate from the MOSFET model [1]. Although the simulation tools provide advanced techniques, the accuracy of the results relies on the accuracy of the aging model itself, which is used to predict the device reliability during circuit operation. Our focus is therefore given on the development of an improved device-aging model for circuit-reliability prediction.

Conventional modeling for predicting transistor aging is derived on the basis of measurements. The accurate modeling of the device aging is normally based on the stress-degradation time and the bias stress applied in experiments with single devices, which covers one of the degradation issues. However, estimating the actually applied stress for each device during circuit operation is more complicated and therefore another issue. Consequently, important tasks for improving the reliability of the circuit simulation are to estimate each individual device stress accurately and also to model the resulting device aging accurately. Particularly, in N-MOSFETs the aging effect is caused by the hot-carrier effect, which is enhanced in new technology-node generations due to higher lateral electric field applied. Here, we investigate the aging effect in leading-edge technologies.

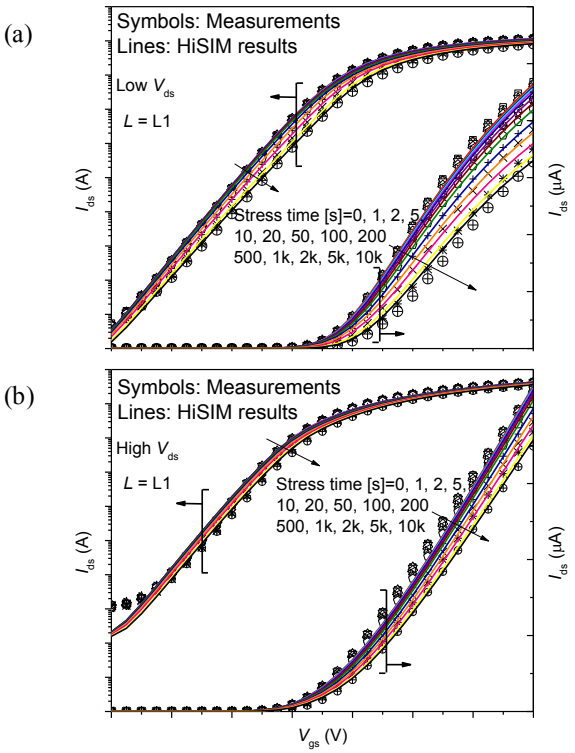


Fig. 1. Comparison of model calculation results with measurements for low (a) and high (b) V_{ds} values for the whole I-V characteristics.

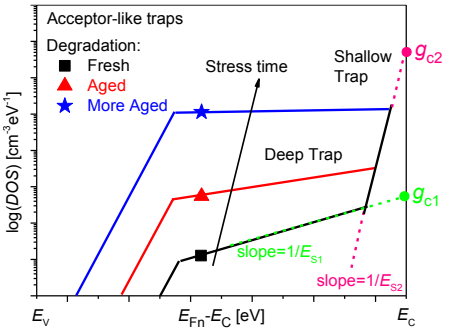


Fig. 2. Comparison of model calculation results with measurements for low (a) and high (b) V_{ds} values for the whole I-V characteristics.

Fig. 1 shows typically measured drain-current *vs.* gate voltage (I_{ds}-V_{gs}) aging characteristics for a 60nm MOSFET technology node at low (Fig. 1a) and high (Fig.1b) drain voltage V_{ds}. Usually, modeling is done separately for different operating conditions, considering individual macroscopic aging observables, such as threshold voltage (V_{th}) and maximum of I_{ds} ($I_{ds\ max}$), and adjusting the aging-model parameters associated with each of these observables [2] [3]. As a result, the burden for constructing an aging model becomes huge, with a complex model-parameter extraction. Such conventional models incorporate the model-equation deviations according to the stress for these operating conditions in order to describe the aging effect [4]. Here, our investigation aims at developing a new modeling approach, which considers the N_{trap} increase as the aging origin in a consistent way.

II. AGING MODELING: TRAP-DENSITY INCREASE BASED

Fig. 2 depicts a schematic of the density-of-state (DOS) model as a function of the state-energy difference from the conduction-band edge, where two parameters g_c and E_s are introduced to model the important features.

Measured 1/*f* noise I_{ds}-V_{gs} data is used for extracting the DOS parameters, because they allow N_{trap} extraction under exclusion of carrier-mobility effects [5]. The relation between N_{trap} and DOS is shown in Table I. From the analysis of measurements, it has been found that a universal relationship exists for DOS as a function of the integrated substrate current I_{sub} during stress time [6].

The obtained results for DOS aging (see Fig. 3a) exhibit an initial linear relationship with unity gradient, when plotted in double-log form (Fig. 3b). Only the extrapolated DOS-axis intercept is different, which is exactly a linear function of the I_{sub} for a fresh device (unstressed device), as depicted in Fig. 4. However, DOS does not increase unlimitedly, but starts to saturate around the value of 4×10^{18}cm^{-3}eV^{-1}. The N_{trap}-increase shows a universal relationship as a function of the substrate current I_{sub} and stress time t

$$N_{trap} = N_{trap0/max} + C \times I_{sub0} \left(I_{sub,t} \right)^{n} \qquad (1)$$

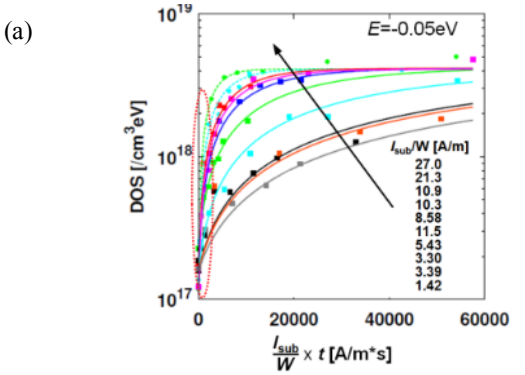
where n=1 is obtained for relatively short t conditions; $I_{sub,t}$=I_{sub}·t. The n=1 relationship verifies the fact that aging is a linear function of $I_{sub,t}$, independently of the bias stress conditions. However, in Fig. 3b the universal relationship is shifted in parallel according to I_{sub0} (I_{sub} of fresh device) following a linear offset increase as Fig. 4 indicates. This result demonstrates that the stress-bias condition and the stress-duration time do not influence the aging equivalently, but that the stress-bias condition determines mainly the initial aging value. This initial aging is a linear function of I_{sub0} (see Fig. 4) and the fresh trapped charge N_{trap0}. Further, enhanced DC-stress reduces the N_{trap} rate (i.e. n<1) for longer stress times t, when reaching N_{trap} saturation at N_{trap} = N_{max} of 4×10^{18}cm^{-3} (see Fig. 3b). Practically, I_{sub}/W·t has a value of the order of 100As/m and therefore the N_{trap} saturation will become hardly observable. N_{trap} is explicitly included in the Poisson equation to assure an accurate calculation of the surface-potential degradation and to determine the aged *I-V* characteristics [7] with the highest achievable physical consistency and correctness. Table I summarizes the main developed model equations and model parameters.

III. DISCUSSION

In order to validate the developed aging model, comparison of modeling and measurement results are performed for three different channel lengths: L1, L2=1.2·L1 and L3=1.7·L1. The studied devices have been stressed at high biases for both V_{ds} and V_{gs} and for several different stress times from 1s to 10ks. *I-V* characteristics are obtained for low and high V_{ds} cases.

TABLE I. MAIN MODEL EQUATIONS AND MODEL PARAMETERS

Symbol	Quantity	Value
N_{trap}	Trap-density increase under stress	$N_{trap0} + C \times I_{sub0} \left(I_{sub,t} \right)^{n}$
N_{trap}	Trap-density increase under long-term stress	$N_{max} + C \times I_{sub0} \left(I_{sub,t} \right)^{n/2}$
N_{trap0}	Initial trap-density	
N_{max}	Maximum trap-density	4×10^{18} cm^{-3}
C	Coefficient for trap-density increase	$\approx4\times10^{15}$ cm^{-3}
n	Initial slope of trap-density increase	1
I_{sub0}	Substrate current	
$I_{sub,t}$	Total stress condition with t duration	$I_{sub}\times t$
$d^2\phi_S/dx^2$	Poisson equation	$-q/\varepsilon_S \cdot (N_D-N_A+p-n-N_{trap})$
N_{trap} (g_c)	Trap-density equation based on DOS	$g_c E_s \cdot \frac{kT/E_s}{\sin(kT/E_s)} \times \exp\left(\frac{E_F - E_C}{E_s}\right)$



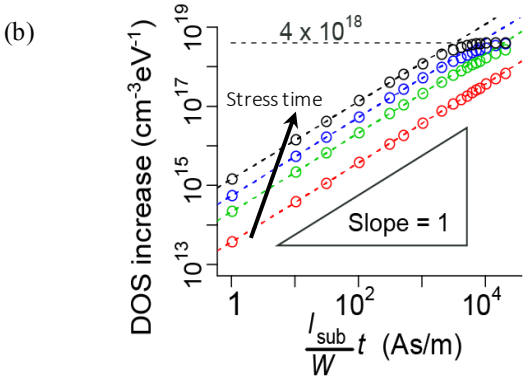


Fig. 3. Extracted DOS as a function of $I_{sub,t}$ for different stress conditions at the energy E of 0.05eV away from E_c in (a) semilog and (b) double-log scale, where N_{trap} is proportional to DOS.

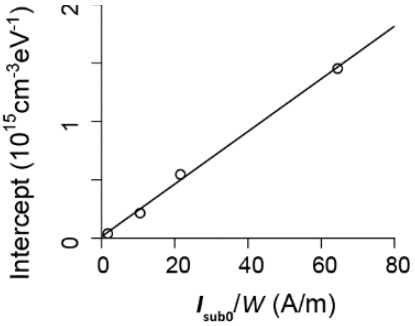


Fig. 4. Initial N_{trap} value at t=1s as a function of I_{sub0}.

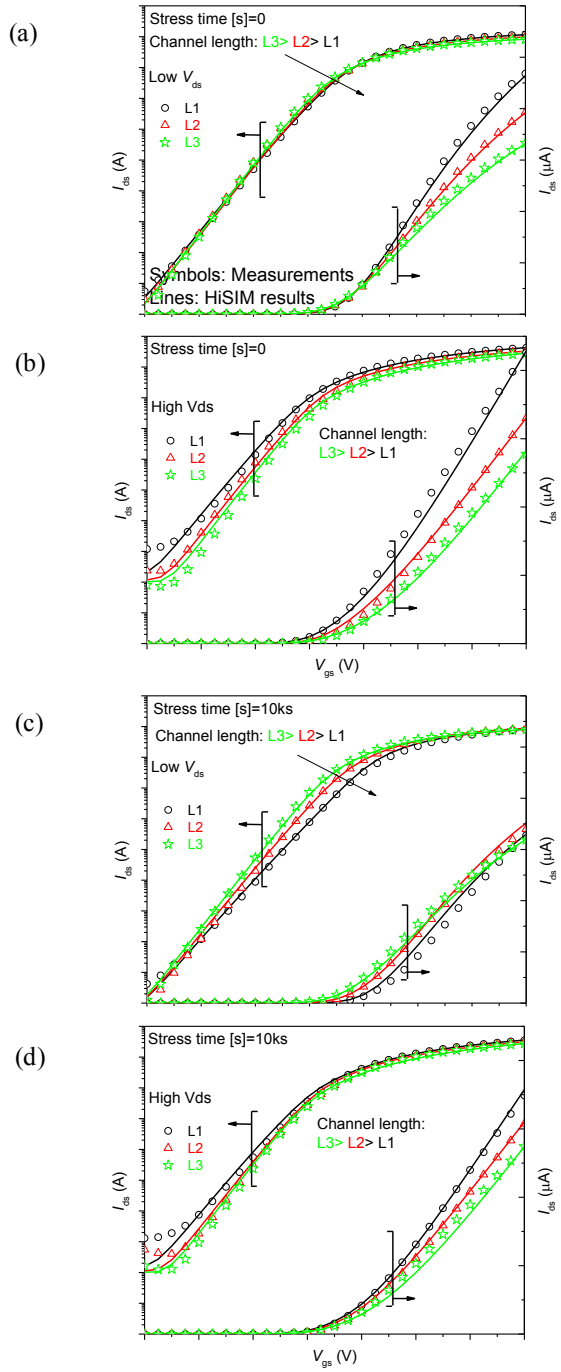


Fig. 5. Comparison of model calculation results with measurements at t=0 for low (a) and high (b) V_{ds} values and for an aged device with t=10ks at (c) low and (d) high V_{ds}. Three different channel lengths are compared by using one single model-parameter extraction. Channel lengths are L1, L2=1.2·L1 and L3=1.7·L1 of model Initial N_{trap} value at t=1s as a function of I_{sub0}.

Fig. 1 shows the aged I_{ds}-V_{gs} characteristics for the transistor with the largest expected aging effects, namely for the case of the shortest channel length L = L1. An accurate prediction for the drain-current degradation is achieved for the whole operation range. Further drain-current comparison is drawn for the three different channel-lengths in Figs. 5a and b before stress at t=0 and in Figs. 5c and d after a stress time of t=10ks. In particular, the model is able to predict the subthreshold-slope degradation due to the trap-density increase.

To understand the degradation of the I-V characteristics, the N_{trap} extraction of the studied devices is shown Fig. 6a. As can be observed, the N_{trap} first increases linearly in this double-log-scale plot and tends to saturate for longer stress times. In Fig. 6b, the N_{trap} is plotted in log-log form as a function of the total stress for the maximum-stress case of 100 A/m·s, which can be a typical value reached for the devices in a circuit. The extracted slope is n=1 for all 3 channel lengths. Finally, Fig. 7 shows a comparison for typical aging parameters that are conventionally considered individually. Our modeling approach follows a cause-effect analysis, i.e., all aging observables are a consequence of the N_{trap} increase.

Therefore, these observables can be extracted without any further adjustment. Only one set of aging-model parameters can be used for all device structures and macroscopic aging observables.

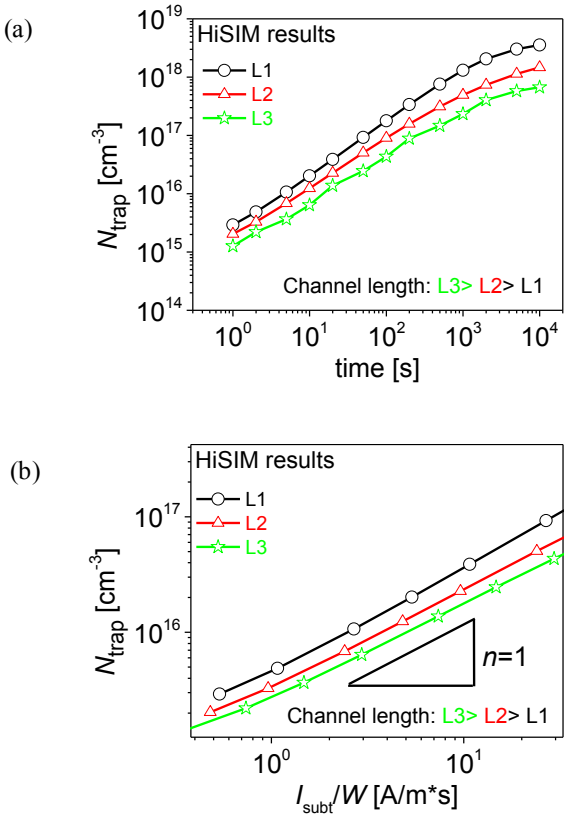


Fig. 6. Extracted N_{trap} as a function of (a) stress time t and (b) I_{subt} for three different channel lengths. A clear parallel offset is observed in Fig.6a for different channel lengths. Fig. 6b shows the range of interest for real applications. Aging saturation also occurs after very long degradation times with enhanced stress conditions. One single model-parameter set is used for the modeling of all structures.

IV. Conclusion

The trap-density increase, the origin of aging phenomena, has been verified to have a universal relationship with the degradation process, i.e., an exponential increase with constant slope that reaches a saturation condition at high degradation times. Only the initial point of the aging process has been found to be substrate-current dependent. Verification is done for a family of devices, using a unique set of model parameters for describing all of their aging phenomena. All aging observables have been properly predicted along with the *I-V* characteristics.

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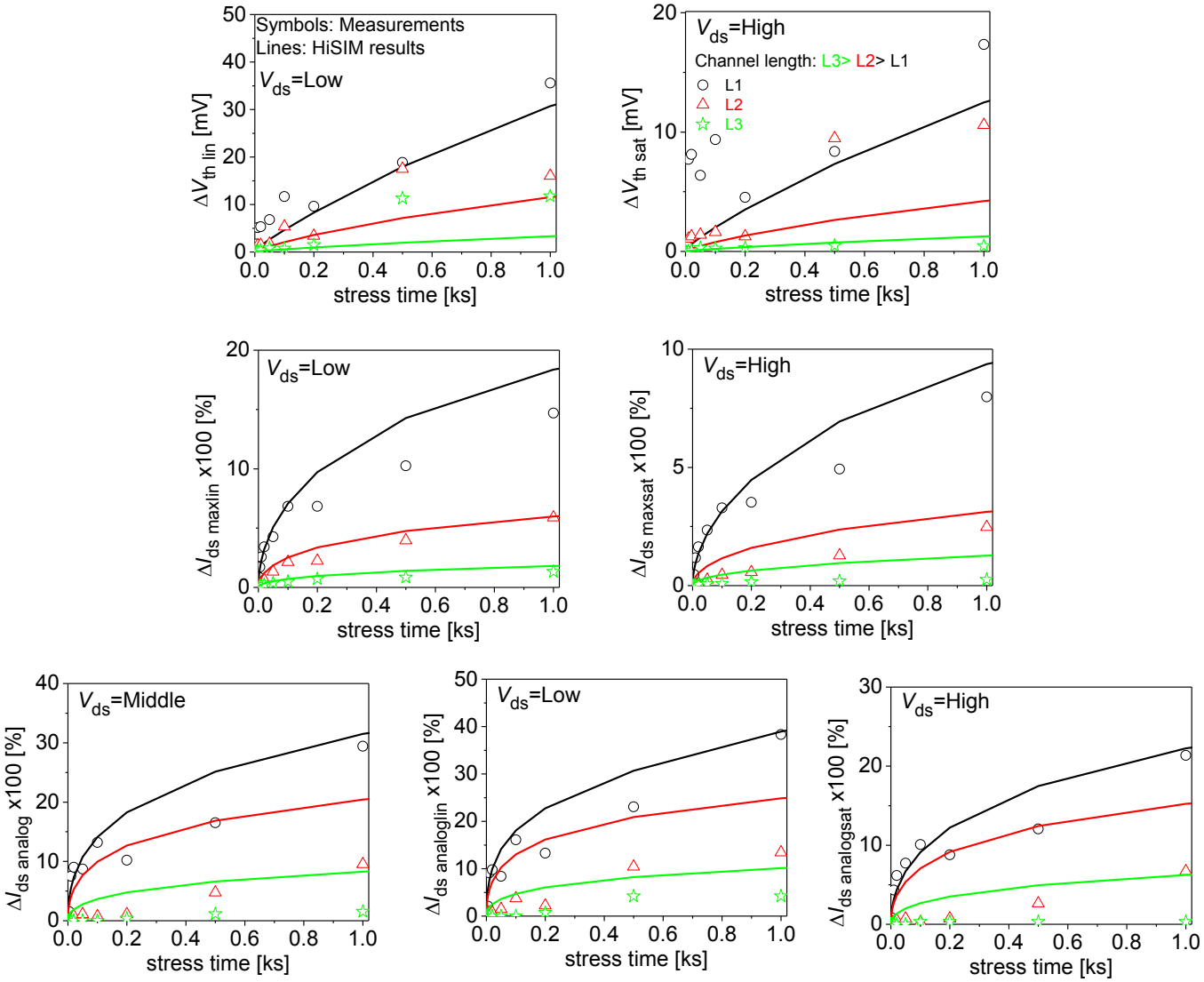

Fig. 7. Measured device characteristics as a function of stress duration for leading-edge MOSFET technology. Calculated results with the developed model are depicted together for the comparison. A single set of model parameters is used for all cases. Channel lengths are L1, L2=1.2·L1 and L3=1.7·L1. t=1ks corresponds to $I_{sub} \cdot t/W$=100As/m.