5-5

A Study of Wiggling AA modeling and Its Impact on the Device Performance in Advanced DRAM

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***Abstract*— In this paper, a wiggling active area (fin) in an advanced 1x DRAM process was analyzed and modeled using the pattern-dependent etch simulation capabilities of the SEMulator3D® semiconductor modeling software. Nonuniformity in sidewall passivation caused by hard mask pattern density loading was identified as the root cause of the wiggling profile. The calibrated model mimicked these phenomena, giving nearly the same output AA shape as the real fabrication process. The wiggling profile's impact on device performance was assessed using the built-in drift-diffusion solver of SEMulator3D. Our analysis confirmed that the wiggling profile, induced by micro-loading during a pattern-dependent etch, has a large impact on overall electrical performance in the device. This was especially apparent with the off-state leakage, primarily due to a worse drain-induced barrier lowering effect in a fatter fin.**

Keywords— DRAM; active area, sidewall passivation, micro-loading, modeling, virtual fabrication, device performance

I. Introduction

Most leading semiconductor manufacturers strive to decrease transistor dimensions to lower cost and improve device performance [1]. However, with transistor size approaching the lower limits of what is achievable, variations occurring during the fabrication process become more and more important for determining final product performance and yield.

Process variations often fail a product in one of two ways. Large variations in transistor properties may lead directly to a hard fail, such as an open or short between two components. Small variations can introduce shifts in the final device in terms of threshold voltage, drive current, off-state leakage, resistance, capacitance, or other parameters, which can then lead to a soft fail or performance degradation due to mismatches between the circuit design and real silicon.

In a DRAM structure, the charging and discharging process of capacitor-based memory is directly controlled by the transistor [2]. The operation speed is modulated by the drive current of the transistor, while the data retention capabilities are limited by the off-state leakage current. Thus, variability in device properties, such as the transistor's AA (active area) dimension and profile, is one of the most important factors influencing the yield and performance of an advanced DRAM product.

A hard mask created by SAQP and the LELE process is widely used to form the AA (transistor fin) in an advanced 1x DRAM process. During the fin etch process, density loading from the hard mask can cause fin profile loading, which mainly occurs in two ways: macro-loading between the fin array's center and edge, and micro-loading within a single fin. The fin profile loading causes wiggling of the AA profile.

In this paper, the wiggling AA profile seen in advanced DRAM processes is investigated and analyzed. The loading profile during pattern-dependent etch is modelled using the SEMulator3D virtual fabrication platform developed by Coventor Inc. [3]. In addition, the impact of the wiggling AA profile on device performance is simulated and analyzed based upon the modelled structures.

II. Wiggling AA Concepts and Model

A. Wiggling AA and its Mechanism

In a 1x/y DRAM reverse engineering report from TechInsights, wiggling AA profiles were found in almost all commercialized DRAM products made by leading DRAM manufacturers. The wiggling AAs show not only wiggling center lines, but also CD differences in the regions neighboring the cut areas. In a specific case where a whole array was inspected, a much larger wiggle was found at the array edge [4,5,6]. (see Fig. 1)

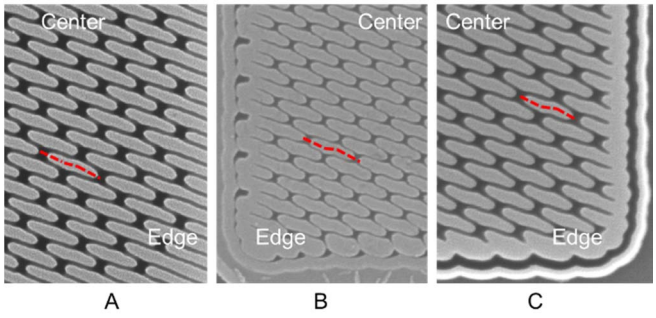

Fig.1. Planar view of the AA profiles of 1x/y DRAM from three different manufacturers [4,5,6] (Courtesy: TechInsights).

In the SAQP process, a spacer is usually deposited using an ALD process, which gives quite conformal and uniform results even in areas with different surface topography. Thus, the wiggling AA is unlikely to be due to a non-uniform spacer; rather, it more likely results from a phenomenon related to pattern dependent etching during the fin etch process, after the spacer is cut.

The main purpose of the fin etch process is to remove the exposed Si, which is not covered by the spacer hard mask, to form the AA and STI. Fig. 2 shows a brief illustration of the fin etch process. After the spacer cut process, the pattern density of the hard mask experiences loading between the cut area (see Fig. 2(a), site A) and the fin area (see Fig. 2(a), site B). During the fin dry etch process, the etch byproduct is more likely to stick to the sidewall of the structure than to be deposited on the bottom surface, because an anisotropic dry etch process provides a higher vertical etch rate on the bottom surface and a lower lateral etch rate on the sidewall. As a result, the sidewall will be passivated by the byproduct and exhibit a taper sidewall profile. Since more Si needs to be removed from the region around site A than the region around site B, more reagent will be consumed, and more byproduct will be generated around site A than around site B (see Fig. 2(b)). Finally, sidewall passivation near site A shows a much more tapered sidewall profile than the region near site B (see

Fig. 2(c)). A similar sidewall passivation etch profile is found in work reported by Yuri Granik et. al, which in that case is probably related to excessive polymer buildup [7].

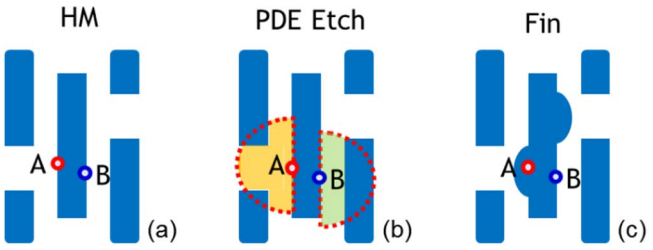

Fig. 2. Illustration of AA profile in Fin etch process (a) hard mask top view before etch, (b) pattern dependence etch amount comparison between site A and B, (c) top view after fin etch.

B. *Wiggling AA Modeling*

The SEMulator3D semiconductor platform provides a novel pseudo-3D approach to pattern dependence modeling based on 2D proximity functions. The proximity functions will be convoluted using a pattern-dependence mask, within a characteristic distance of a point of interest, and finally yield a 2D loading map. This 2D loading map modifies the behavior of a 3D behavioral etch algorithm in the software [8].

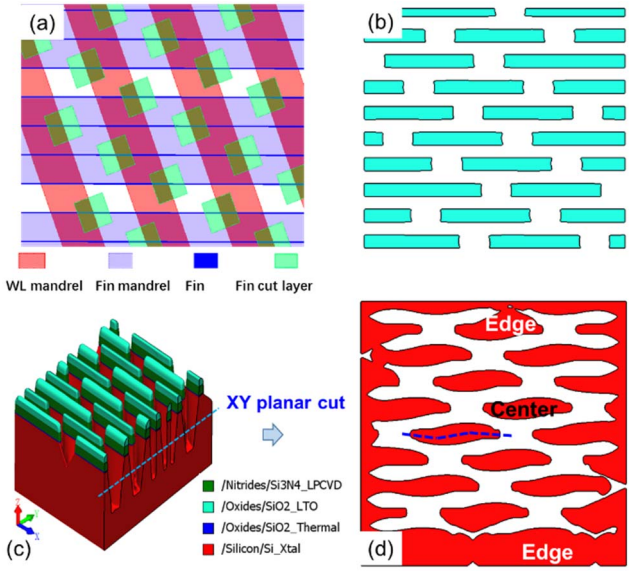

Fig. 3: (a) Layout design, (b) PDE mask generated from hard mask, (c) 3D structures after fin etch, (d) AA profile by planar cut on fin middle.

In this work, we create a pattern-dependence mask by cutting an XY plane from the 3D structure of the hard mask before fin etching occurs (see Fig. 3(b)). The related coefficients and characteristic distance in the proximity function can be calibrated from known Si data. Fig. 3(a) shows the layout design (rotated 20 degrees counterclockwise for easy viewing), 3(b) shows the generated pattern-dependent mask, and 3(c) and 3(d) show the 3D structure and planar view (polished to fin middle in the Z direction) from the simulation. These results were compared with hard silicon data shown in Fig. 1. Comparing 3(d) with Fig.1 (c), a similar wiggling AA profile is found at both the array center and the edge, demonstrating that the model properly reflects real Si. Fig. 4 displays the AA profile at different fin heights, providing 2D and 3D modeled views of the AA profile evolution from fin bottom to fin top.

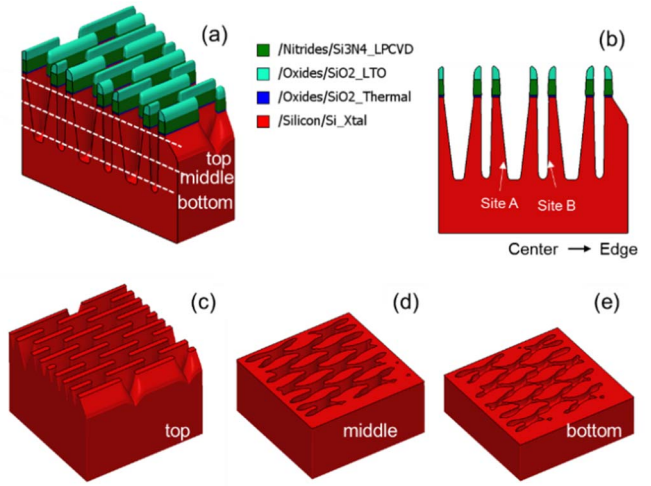

Fig. 4. AA profile at different fin heights (a)3d view cut on wordline, (b) cross-sectional view cut on wordline, (c) 3d view cut on fin top, (d) 3d view cut on fin middle, (e) 3d view cut on fin bottom

III. Device Performance Simulation and Analysis

A. *Split Condition and Flow Build up*

In the 1x/y DRAM cell with a buried wordline, the fin is recessed during the wordline formation process, and the final channel is a buried channel beneath the word line. Fig. 5(a) shows the top view of the structure after wordline formation (for easy observation, some metals and dielectric materials are made transparent). Fig. 5(b) shows a cross-sectional cut of the fin in the wordline direction while 5(c) shows the cross-sectional cut of the channel in the fin direction after wordline formation. The wiggling profile is more serious at the middle of the fin than at the fin top, due to the micro-loading effect occurring during the etch process (see Fig. 4 (c) and (d)). Since the channel is located near the middle of the fin, the final fin CD under the channel will be much larger due to micro-loading and sidewall passivation. Fin CD loading may introduce much different device performance, such as differences in the threshold voltage, off-state current, drive current, and so on.

To evaluate the impact of the wiggling AA profile on device performance, a full loop 1x DRAM process flow from the AA to the CC (capacitor contact) is built using SEMulator3D. In the flow, sidewall angle splits of 0.1, 2.5, and 5 degrees are used in the pattern-dependent etch process to understand the differences in final device performance. Fig. 6(a) shows the final 3D structure of the DRAM array, 6(b) shows a single device (cropped), and 6(c) shows the cross-section view cut along the fin, with ports defined for electrical analysis. Fig. 6(d), (e) and (f) show cross-sectional views of the fin profiles with different sidewall angle splits. A thicker and more asymmetrical fin is visible when the sidewall angle is larger.

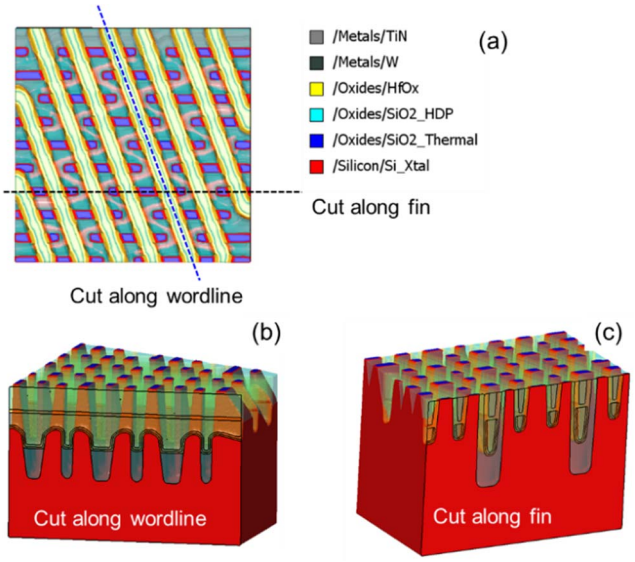

Fig. 5. DRAM structure after worldline formation (a) top view, (b) cross-sectional view along wordline, (c) cross-sectional view along fin.

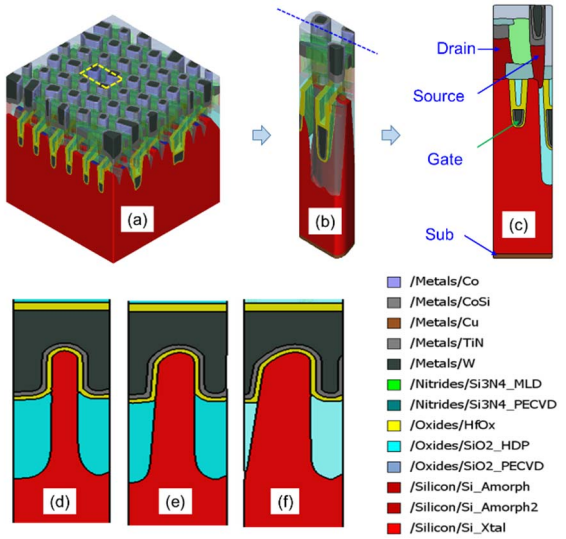

Fig. 6. DRAM structure after capacitance contact formation, (a) 3D view, (b) single device view, cropped, (c) View along fin cut with port definition, (d) SWA=0.1 deg (WL cut), (e) SWA=2.5 deg, (f) SWA=5 deg.

B. *Device Simulation and Analysis*

Based on the previously defined virtual structure, a single device is cropped out for electrical analysis (see Fig. 6(b)). The electrical ports for the source, drain, gate, and sub are assigned to the structure (see Fig. 6(c)). The built-in drift-diffusion solver of SEMulator3D is used to calculate electrical performance, including the Id-Vg curve, along with current distribution of these experimental sidewall angle splits. Fig. 7(a) shows the Id-Vg curve plotted on a log scale with V_d=3V, where V_g is swept from 0 to 1.2V. Fig. 7(b) shows the linear scale I_d-V_g curves of these splits.

From the linear I_d-V_g curves, it is noted that a slightly higher drive current can be obtained using a larger sidewall angle in the fin etch process. The on-state current difference is likely due to the differences in the effective channel width for different fin profiles. Usually, a fatter fin with a larger sidewall angle will have a wider effective channel width, which could be observed in Fig. 6(d, e, f).

From the logarithmic I_d-V_g curve, the off-state leakage and subthreshold swing of different splits can be observed. The fatter fin exhibits much higher off-state leakage and larger subthreshold swing, demonstrating that channel controllability is weak. Similar research with real Si data has been reported in a logic fin research paper [9]. Fig. 7(c) shows the drain-leakage current relationship for different drain voltages at V_g=0V. The leakage in a fatter fin will dramatically increase at higher drain voltages, while it is not so obviously changed in a thinner fin. Fig. 7(d) displays the drive current and leakage current (V_d=3V) with different splits. It shows that the drive current becomes slightly higher as the sidewall angle becomes tapered, but it saturates or even decreases with the fattest fin. On the other hand, the leakage current increases as the fin sidewall angle increases. The higher source-drain leakage current is due to the drain-induced barrier lowering effect (DIBL) in the short channel MOSEFT with weak gate controllability [10,11].

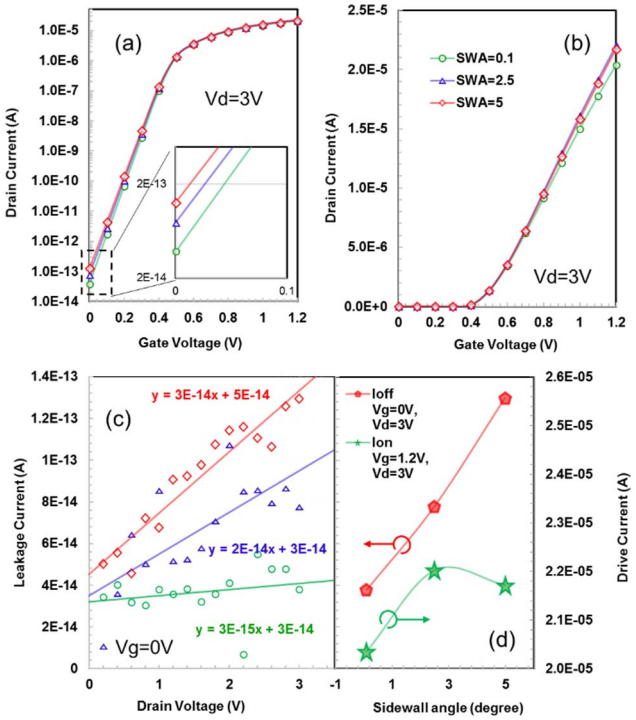

Fig. 7. Transfer characteristics (a) log I_d-V_g, (b) linear I_d-V_g, (c) off-state drain leakage at different V_d, (d) drain leakage and drive current at V_g=1.2V, V_d=3V.

Fig. 8 displays off-state leakage current distribution in the fin. It shows that most leakage current is concentrated in the fin center, far from the gate metal and not strongly controlled by the gate electrical field. Because of the diminished gate controllability in the fatter fin, the leakage current density is much higher than in a thinner fin.

Based on these results, it is easy to see that a narrower fin with a smaller sidewall angle and less micro loading during etching is preferred in an advanced DRAM process. The micro loading seems unavoidable due to the incoming hard mask density loading. However, if we change the integration scheme to first generate a uniform fin, and then cut the unnecessary fin after the fin etch process, the micro loading

issue may be avoided. The tradeoff is that more difficult process control is required during the fin cut last etch process.

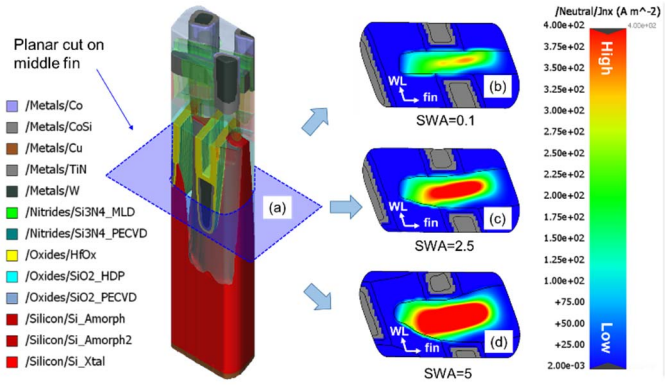

Fig. 8. Channel leakage profile from fin surface to fin center with different sidewall angle split.

IV. Conclusions

In this paper, wiggling AA in an advanced DRAM process was analyzed and modeled using the SEMulator3D platform. The impact of wiggling AA on device performance was reviewed using a drift-diffusion solver. The analysis shows that micro loading, induced during pattern-dependent etching, can cause a wiggling AA. This micro loading has a large influence on the device's electrical performance, especially the off-state leakage, which is a key factor in determining the data retention capabilities of DRAM cells. Effort should be devoted to minimizing this micro loading effect to further enhance device performance and yield. Potential solutions include optimizing the fin etch process, or changing the integration scheme from fin cut first to fin cut last in the fin formation process.

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5-6

Reactive Force-Field Molecular Dynamics Study of the Silicon-Germanium Deposition Processes by Plasma Enhanced Chemical Vapor Deposition

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***Abstract*— In order to form a SiGe thin film by chemical vapor deposition (CVD) with a suitable quality for advanced devices, the relationships between materials/process and structure/composition are needed to be clarified at the atomic level. We simulated SiGe CVD by using reactive force-field (ReaxFF) molecular dynamics simulations, especially on binary systems of SiH_x + GeH_x, and derived the influence of the substrate temperature and these ratios of gaseous species on the crystallinity and compositions in the thin films. The crystallinity increases as the substrate temperature increases, and the lowest crystallinity is obtained at the ratios of gaseous species 0.5 and 0.7 for the SiH_3 and SiH_2, respectively. As the substrate temperature increases, the hydrogen content decreases while Si and Ge content tend to increase. These trends can be seen in relevant studies. Through this simulation we successfully observe that the reactivity of gaseous species greatly affects the crystallinity and compositions in the thin films.**

Keywords*— *Chemical Vapor Deposition, Reactive Force-Field Molecular Dynamics Simulation, Silicon-Germanium, Thin Film Deposition

I. Introduction

In the field of semiconductor manufacturing, chemical vapor deposition (CVD) and atomic layer deposition (ALD) are known as one of the common and powerful methods to deposit a high-quality thin film. In order to deposit promising thin films using CVD/ALD methods, the materials/process, structure/composition, and properties should be simultaneously optimized. For several decades, advances in semiconductor manufacturing have been increasing the number of materials and processes used for advanced device productions. As a result, an optimal combination should be selected from enormous number of options. This is hard issue and lead to increase the cost and development periods for device productions in the semiconductor manufacturing.

A new materials development tool called as "Materials integration" have appeared to deal with the hard issue. Materials integration aims to support the material development from an engineering viewpoint by combining all science and technology as shown in Fig. 1. In point of fact, some inorganic materials such as battery components have been successfully discovered for several years. Materials integration has also shown promising results in the semiconductor manufacturing. Chopra *et al.* developed a software tool for creating plasma etch recipes based on physical models and Bayesian inference [1] and applied it to prediction of experimental results [2]. They showed that the etching rate of SiO_2 with CF_4/Ar gases could be predicted. Suzuki *et al.* adopted machine learning approaches to optimize the plasma enhanced ALD process such as the uniformity [3]. They succeeded in achieving the target values and even outperforming the knowledgeable engineers. Chopra *et al.* and Suzuki *et al.* simply optimized only the process. The researches by Tanaka *et al.* are outstandingly noticeable from the viewpoint of simultaneous optimizing (co-optimization) materials and their processes [4]. They developed a predictive method to co-optimize by combining Bayesian optimization with data extracted from scientific papers, experimental data, and material databases. However, unfortunately, the results based on predictive model could not represent experimental results well.

Two approaches typically are known to improve the accuracy of materials integration; data-driven approach and physics-driven approach. The data-driven approach is based on correlations of material performance and structure extracted from systematically accumulated data. The physics-driven approach is based on the establishment of principles through elucidating controlling factors for material properties at each scale. Both approaches are necessary for all material development regardless of semiconductor manufacturing, and we selected latter. In order to proceed with the physics-driven

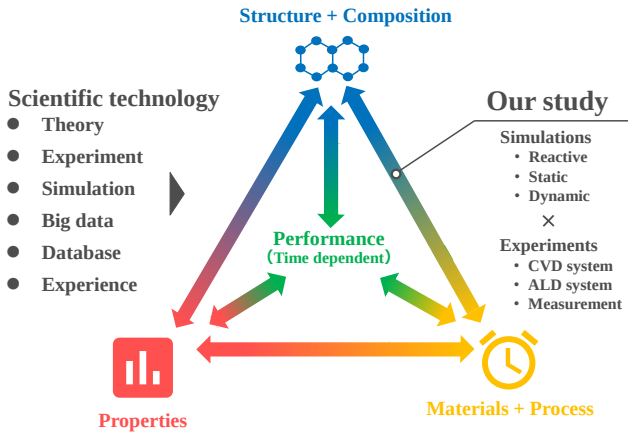

Fig. 1. A schematic diagram of Materials integration and our study position.