On the Physical Mechanism of Negative Capacitance Effect in Ferroelectric FET

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***Abstract*—Negative capacitance FET is a promising CMOS technology booster which may break the limit of 60mV/dec in subthreshold swing (SS) without degrading performance. We investigated the physical mechanism of negative capacitance in ferroelectric FET (FeFET) by considering the dynamics of the polarization in ferroelectric gate insulator: transient negative capacitance (TNC). Polarization switching and depolarization effect are essential to cause negative capacitance effect, that is, apparent surface potential amplification in deep subthreshold region with small depletion layer capacitance. Moreover, unique features of reverse DIBL and negative differential resistance (NDR) are also reproduced by the transient negative capacitance theory. Modeling charged defect in FeFET, hysteresis-free sub-60mV/dec SS can be realized. TNC theory is regarded as a comprehensive framework to model subthreshold characteristics of FeFET.**

Keywords—negative capacitance, ferroelectric FET, polarization, subthreshold swing, DIBL, NDR, charged defect.

I. INTRODUCTION

For future energy-efficient computing, ferroelectric FET (FeFET) with sub-60 mV/dec subthreshold slope (SS) caused by negative capacitance (NC) effect has been proposed [1]. NC effect was originally proposed based on a static model (Quasi static NC: QSNC). The metastable NC region in double well-shaped free energy landscape and S-shaped polarization-voltage (P-V) curve of ferroelectric (FE) based on the phenomenological Landau theory can be stabilized and accessible with an appropriate positive capacitor connected in series [1, 2]. According to this theory, the capacitance matching for steep SS should be achieved near inversion region instead of subthreshold region with standard channel design [2]. However, many experimental results of long channel transistors show steep SS in deep subthreshold region with negligible hysteresis in quasi-static condition, which may not be fully explained only within the framework above [3-5]. Moreover, the original theory assumes single-domain configuration in which all domains flip simultaneously in response to electric field as a large single-domain. This is not consistent with the classical FE physics. It is natural that multi-domain switching occurs via anti-parallel configuration from the perspective of thermal dynamics [6, 7]. In addition, it was reported that polarization switching plays an important role in steep SS phenomenon. While the stabilized NC in S-shaped P-V curve can be accessed without polarization switching in unipolar sweep according to the original theory, in Ref. [5], sub-60 mV/dec SS happens only when the gate voltage sweep range is large enough to initialize polarization and trigger large polarization switching in bipolar sweep. Furthermore, NC is static and steep SS behavior should be time independent according to the original theory. However, in Ref. [8], sub-60 mV/dec SS can be only realized within certain measurement time window determined by switching dynamics of polarization, which indicates that NC effect has a transient aspect. Therefore, several groups have been exploring alternative interpretations for the NC effect as well as steep SS phenomenon [6, 9-13]. what is the physical mechanism of such transient NC (TNC) and how it affects subthreshold behavior of FeFET are not fully clarified yet and need to be investigated.

FeFET with sub-60mV/dec SS also exhibits unique device characteristics such as reverse drain-induced barrier lowering (R-DIBL) and negative differential resistance (NDR) [14-17]. Previously, these special behaviors were predicted by the QSNC theory and regarded as the indication of the stabilized NC in ferroelectric [18-20]. The theory of NC needs to give reasonable explanation not only for steep SS but also R-DIBL and NDR consistently. It should be also investigated that TNC theory can also explain R-DIBL and NDR based on transient device simulation.

One another important aspect is an impact of defects such as fixed charge and charge trapping in FeFET on hysteresis behavior. There are quite a number of reports that shows almost hysteresis-free and sub-60mV/dec subthreshold characteristics. Charge trapping appears to compensate the ferroelectric hysteresis, resulting in hysteresis-free. But this has not been fully investigated yet.

In this paper, we overview our research progresses and explain the current understanding of negative capacitance in FeFET from TNC perspective.

II. MODEL DESCRIPTION & SIMULATION METHOD

The static saturation polarization-voltage (P-V) loop of ferroelectric (Fig. 1 (a)) is described by Miller model which is an analytical version of multi-domain Preisach model [21]. Here, P_s and P_r are saturation and remnant polarization, respectively. V_{fe} and V_c are voltage across ferroelectric and coercive voltage of ferroelectric, respectively. By considering a paraelectric component, the static saturation charge-voltage (Q-V) loop (Fig. 1 (b)) is calculated by the sum of spontaneous polarization and the paraelectric component. Here, ε_r and t_{fe} are the relative dielectric constant and the thickness of ferroelectric, respectively.

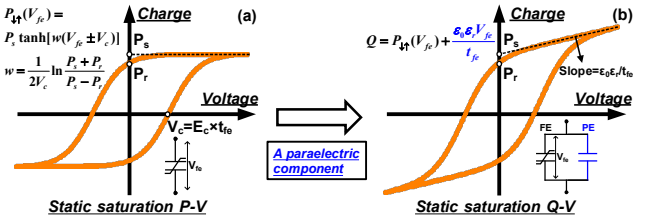

Fig. 1. The static saturation (a) P-V and (b) Q-V of a ferroelectric capacitor.

In order to capture minor loops due to partial polarization switching and ferroelectric history, the turning point method

is applied [22, 23]. Fig. 2 (b) is an example of minor P-V loops staring from the saturation loop and passing through points a, b, c, d, and e in sequence. The minor loop is calculated according to the last two turning points ((V_{i-1}, P_{i-1}) and (V_i, P_i)), as shown by the equations in Fig. 2 (b). Then, the minor Q-V loop can be obtained by considering the paraelectric component, which is the same as the method in Fig. 1.

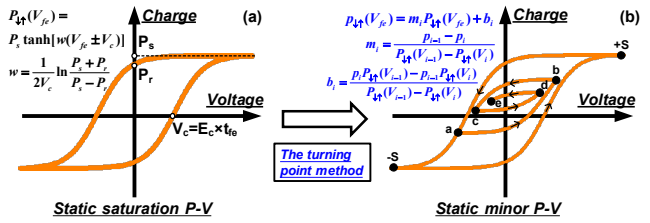

Fig. 2. (a) The static saturation P-V loop and (b) the static minor P-V loop of a ferroelectric capacitor.

Finally, polarization switching delay is introduced to simulate the dynamic behavior of ferroelectric [12,13]. The delay is determined by a first order differential equation (the equation in Fig. 3) where the switching delay (τ) is a constant. The equivalent circuits of a ferroelectric capacitor in both static and transient conditions are illustrated in Fig. 3. In transient conditions, the actual driving force of spontaneous polarization is the auxiliary voltage (V_{aux}). There is certain delay between V_{aux} and the actual voltage across ferroelectric (V_{fe}).

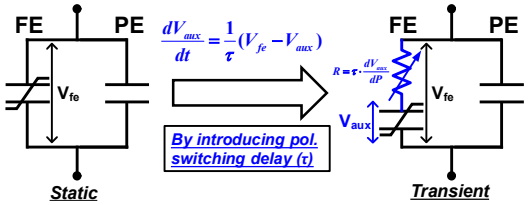

Fig. 3. Equivalent circuits of a ferroelectric capacitor in both static and transient conditions.

Fig. 4 (a) illustrates the simulated transistor structures and parameters. Both FeFET and reference MOSFET are simulated. The only difference between them is the additional $HfZrO_2$ (HZO) thin film in the gate stack of FeFET.

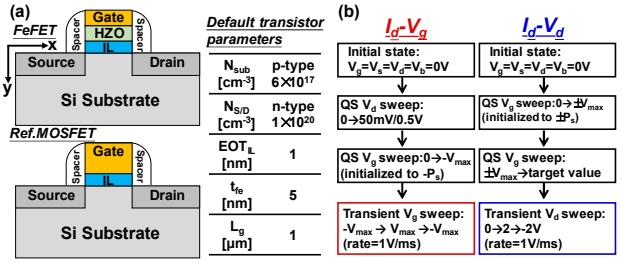

Fig. 4. (a) The simulated device structures and parameters. (b) The flow chart for both I_d-V_g and I_d-V_d simulation.

Fig. 4 (b) shows the flow chart for transistor simulation. Before transient I_d-V_g and I_d-V_d simulation, quasi-static (QS) sweep is applied to initialize certain polarization states and bias conditions [24]. After that, double V_g or V_d sweep is applied in transient condition. Note that the value of V_{max} in Fig. 4 (b) is large enough to initialize saturation polarization (P_s) in this study.

To extract the parameters and verify the abovementioned ferroelectric model, a ferroelectric capacitor in response to triangular waveforms is simulated and fitted to the measurement result [25].

III. Results and Discussions

A. TNC in capacitors

To verify this model and extract parameters of FE, quasi-static Q-V curve of a 10 nm FE capacitor is simulated and fitted to our previous experimental result of a FE-HfZrO (HZO) capacitor as shown in Fig. 5 (a) [25]. The extracted P_r, P_s, ε_r, and E_c (quasi-static parameters) are 20.1 μC/cm^2, 23 μC/cm^2, 35, and 1.16 MV/cm, respectively. Meanwhile, the experimental displacement current of the FE capacitor in response to a triangular waveform can be reproduced with the same fitting parameters shown in Fig. 5 (b).

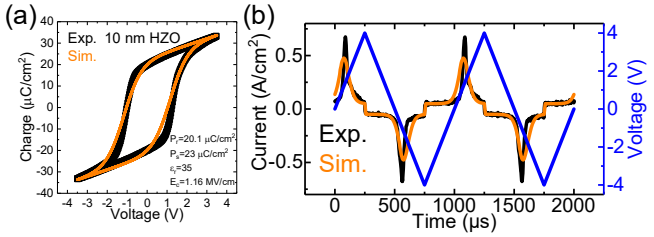

Fig. 5. (a) *Q-V* curve (100 Hz) with parameter fitting for 10 nm HZO. (b) Displacement current of FE capacitor in response to a triangular waveform with same parameter fitting [19].

In order to extract dynamic parameter, τ, resistor-metal/FE/metal (R-MFM) netlist which is the same as the experimental set-up in Ref. [25] is reconstructed in simulation. Fig. 6 (a)-(c) show transient responses of R-MFM netlist where R=20 kΩ (Fig. 6 (e)) and the input voltage pulse is from −4 V to 4 V. For the best fitting, τ=4 μs is obtained. Fig. 6 (d) shows reconstructed Q-V_{fe} curves for both measurement and simulation where TNC is directly observed as a voltage snapback [26].

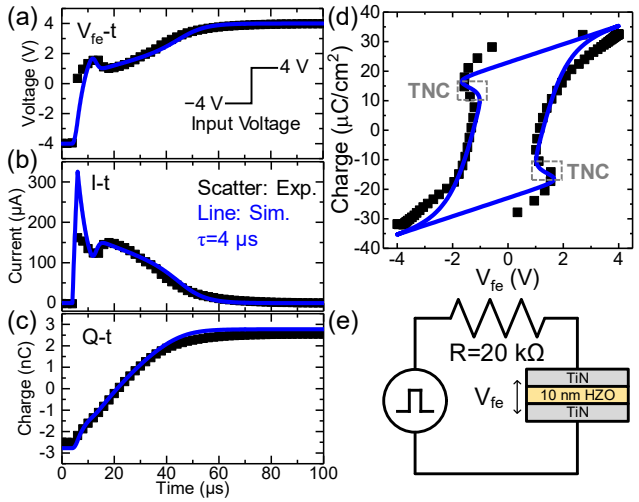

Fig. 6. (a)-(c) Measured and simulated transient responses of R-MFM. (d) Reconstructed *Q-*V_{fe} curves for both measurement and simulation. (e) Experiment and simulation set-up [19, 20]

By using the dynamic FE model and FE parameters extracted above, transient characteristics of a FE-DE series capacitor which is a simplified model of a FeFET gate capacitor is simulated in response to a triangular waveform (Fig. 7 (a) inset). Fig. 7 (a) and (b) plot the simulated internal voltage amplification (A_v) as function of gate voltage (V_g) and corresponding Q-V_{fe} curves, respectively. A_v is larger than 1 in certain V_g region and TNC is observed as a voltage snapback for τ=4 μs, while A_v is always smaller than 1 and no

TNC occurs for τ=0 (quasi-static condition). This means that finite polarization switching delay is responsible for TNC.

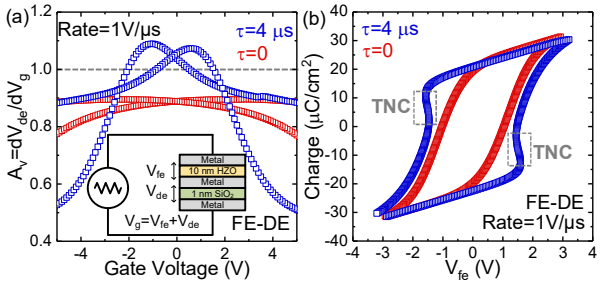

Fig. 7. (a) Simulated internal voltage amplification (A_v) as function of gate voltage (V_g) in FE-DE series capacitor. (b) Corresponding Q-V_{fe} curves. A_v is larger than 1 and TNC is observed as a voltage snapback for τ=4 μs, while A_v is always smaller than 1 and no TNC is observed for τ=0 (quasi-static condition).

To better understand the physical mechanism of TNC, Fig. 8 (a) shows the simulated polarization switching current (dP/dt), total free charge current (dQ/dt), and voltage drop across FE (V_{fe}) as function of time for τ=4 μs. TNC can be understood as the consequence of incomplete screening of spontaneous polarization charge (depolarization effect) [8, 23-25]. Fig. 8 (b) shows the schematic illustration of the physical mechanism for TNC in FE-DE series capacitor. Initially, as V_g is swept in forward direction from the maximum negative value, V_{fe} increases by charging the PE component. After a certain time period, dP/dt increases due to the response of spontaneous polarization. When the increased dP/dt is larger than dQ/dt, in order to satisfy the charge balance condition: $Q=\varepsilon_0\varepsilon_r E_{fe}+P$, V_{fe} has to drop, which is regarded as TNC. Meanwhile, there is a voltage gain in the internal node because of the reduced V_{fe} and more increased V_{de}. It should be noted that, in quasi-static condition, dP/dt is never larger than dQ/dt and TNC is not observed.

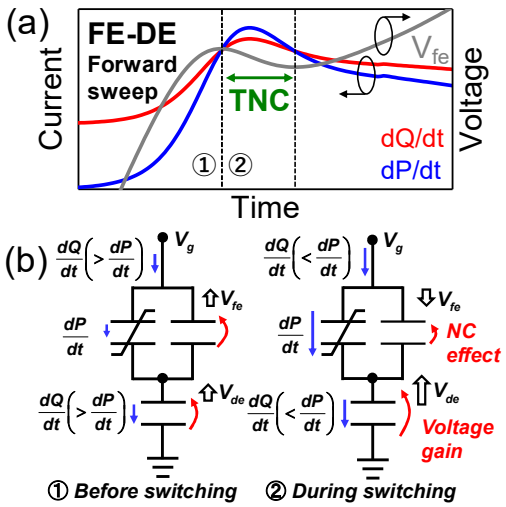

Fig. 8. (a) Simulated polarization switching current (dP/dt), total free charge current (dQ/dt), and voltage drop across FE (V_{fe}) as function of time for τ=4 μs in FE-DE series capacitor. (b) Schematic illustration of physical mechanism for TNC.

B. Steep SS, Reverse DIBL and NDR in FeFET

Fig. 9 (a)-(c) plot simulated I_d-V_g curves and SS in forward and reverse sweep, respectively. Sub-60 mV/dec SS is achieved more prominently in reverse sweep for the FeFET and counter-clockwise hysteresis is caused by polarization switching. FE-type hysteresis can be compensated by threshold voltage shift caused by charge trapping and detrapping [10, 17, 27], which can be a reasonable explanation for sub-60 mV/dec SS with negligible hysteresis observed in some experiments and revisited later. Note that SS is also lower than 60 at very low I_d level in forward sweep for both FeFET and reference MOSFET is due to the displacement current at the sweep rate.

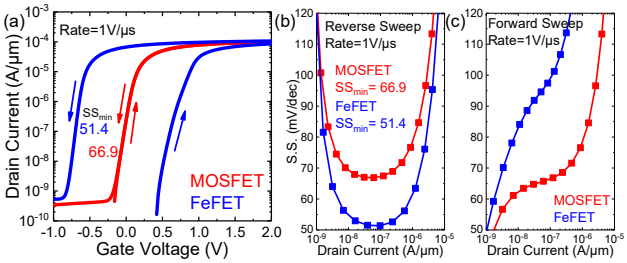

Fig. 9. (a) Simulated I_d-V_g curve for both FeFET and reference MOSFET with τ=4 μs and sweep rate of 1 V/μs. (b) SS in reverse sweep. (c) SS in forward sweep.

Similarly to the discussion for the FE-DE series capacitor, dP/dt and dQ/dt versus time are plotted in Fig. 10 (a) and (b) for further understanding the relationship between TNC and steep SS phenomenon. During forward/reverse sweep, two TNC region (|dP/dt|>|dQ/dt|) are observed. The first one is in accumulation/inversion region and the second one is in transition between accumulation and inversion. These two TNC region can be also observed as two negative slope regions with different slopes in Fig. 10 (b). In subthreshold region, small depletion layer capacitance suppresses both dQ/dt and dP/dt and causes strong depolarization effect with dP/dt > dQ/dt, thus steep SS. Sub-60 mV/dec is observed in wide I_d range only for reverse sweep, since the second TNC covers most of the weak inversion and depletion regions for reverse sweep (Fig. 10 (b)) but not forward sweep (Fig. 10 (a)). Fig. 10 (c) plots zoomed-in Q-V_{fe} curve around 0 charge corresponding to the subthreshold region in Fig 10 (a) and (b), which also indicates that NC is more prominent in wide I_d range in reverse sweep. With different FE parameters, it is possible to make TNC cover most of the weak inversion region in forward sweep as well, thus leading to sub-60 mV/dec SS near V_{th} bidirectionally (not shown, this time).

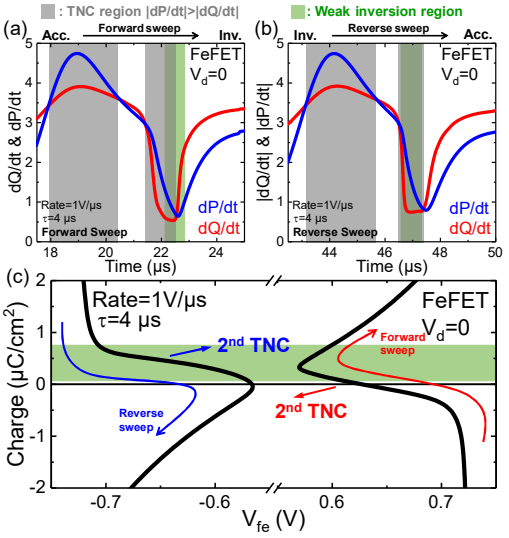

Fig. 10. Simulated polarization switching current (dP/dt) and total free charge current (dQ/dt) as a function of time for (a) forward and (b) reverse sweep. (c) Zoomed-in Q-V_{fe} curve around 0 charge.

Fig. 11 plots the simulated transient I_d-V_g characteristics and the calculated SS-I_d for FeFET. Prominent sub-60mV/dec SS and R-DIBL are observed in reverse sweep. R-DIBL can be also judged by the increased barrier height as shown in Fig. 12. To explore the mechanism of R-DIBL, we investigated the charge density in the channel (N_{ch}) and the voltage across the ferroelectric layer (V_{fe}) at different V_d (Fig. 13). For fixed V_g, higher V_d will lead to higher channel potential and thus lower N_{ch} and more depletion near the drain. This happens even for conventional MOSFET (Fig. 13 (a)). However, for FeFET, higher V_d (lower N_{ch} and more depletion) will result in higher V_{fe} (reduced $|V_{fe}|$) due to TNC (Fig. 13 (b)). The increased V_{fe} will further decrease N_{ch} (Fig. 13 (c)), raise the channel electron potential shown in Fig. 12, and thus I_d decreases [24]. This way, R-DIBL happens.

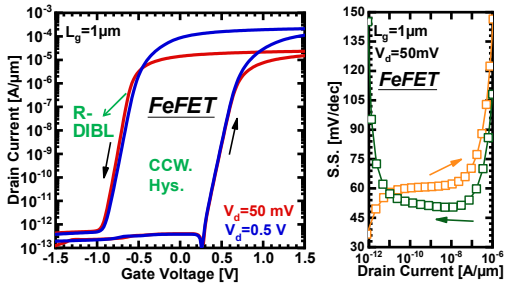

Fig. 11. The simulated transient I_d-V_g characteristics and the calculated *SS*-I_d for FeFET.

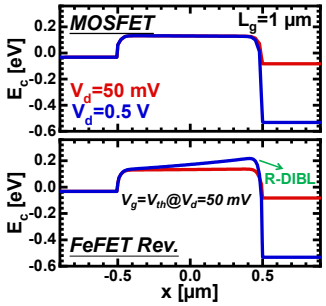

Fig. 12. Extracted conduction band-edge energies (E_c). R-DIBL can be judged by the increased barrier height at higher V_d.

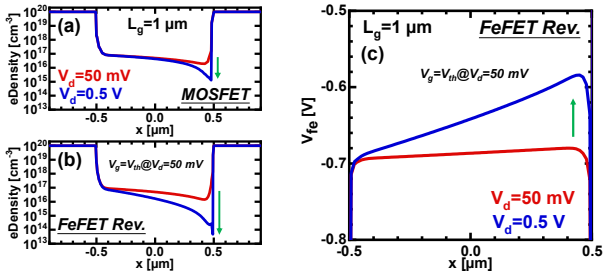

Fig. 13. Simulated charge density in the channel (N_{ch}) at different V_d for (a) reference MOSFET and (b) FeFET. (c) Voltage across ferroelectric (V_{fe}) at different V_d.

Fig. 14 (a) and (b) plot the simulated transient I_d-V_d characteristics for FeFET with $+P_s$ (low V_{th}) and $-P_s$ (high V_{th}) initialization, respectively. In the case of $+P_s$ initialization, I_d shows large hysteresis. Moreover, I_d decreases as V_d increases in forward V_d sweep, which is regarded as NDR. However, in the case of $-P_s$ initialization, I_d is nearly hysteresis-free and no NDR is observed. These results are consistent with experiments demonstrated in Ref. [17].

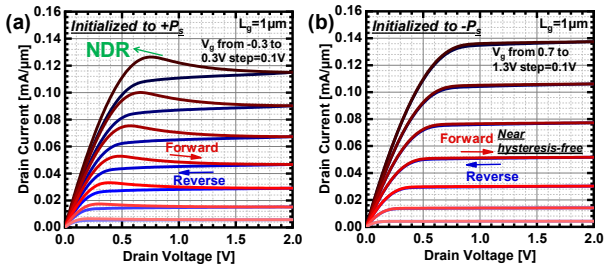

Fig. 14. The simulated transient I_d-V_d characteristics for FeFET with (a) $+P_s$ (low V_{th}) and (b) $-P_s$ (high V_{th}) initialization. NDR is observed only in forward V_d sweep with $+P_s$ initialization.

According to the simulated I_d-V_d characteristics (Fig. 14), ferroelectric history should play an important role in NDR. We investigated the Q-V trajectory of ferroelectric (Q_{fe}-V_{fe}) near the drain during the V_d sweep (Fig. 15). Note that TNC can be induced during V_d sweep instead of V_g sweep. In the case of $+P_s$ initialization, Q_{fe}-V_{fe} shows large hysteresis and TNC is observed only in forward sweep because there is a pathway where Q_{fe} decreases while V_{fe} increases as a part of major loop. Whereas, in the case of $-P_s$ initialization, Q_{fe}-V_{fe} is nearly hysteresis-free and no TNC is observed because there is no pathway where Q_{fe} increases while V_{fe} decreases in minor loop. The behaviors of Q_{fe}-V_{fe} are consistent with I_d-V_d (Fig. 14), which means TNC is responsible for NDR observed in forward sweep, if $+P_s$ is initialized.

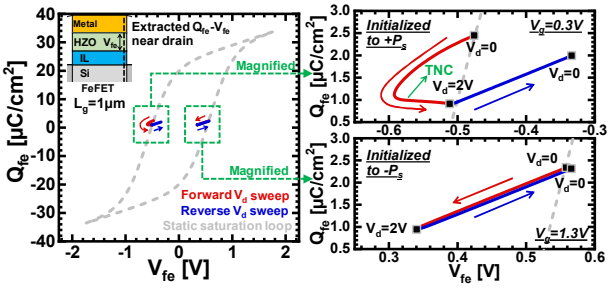

Fig. 15. Extracted Q-V trajectory of ferroelectric (Q_{fe}-V_{fe}) during the transient V_d sweep. The magnified plots are shown in the right side.

The mechanism of NDR is similar to R-DIBL and it can be illustrated as follows [24]. For fixed V_g, as V_d increases, N_{ch} decreases and the channel near the drain depletes more due to the increased channel potential near the drain. Then, in TNC region, V_{fe} increases according to the charge balance condition. This increased V_{fe} further reduces N_{ch} near the drain, the electron potential is raised, and I_d decreases. Therefore, NDR happens. This can be also interpreted as R-DIBL in that V_{th} increases and I_d decreases as V_d increases.

C. Charged defects in FeFET

As already mentioned in the earlier sections, TNC describes sub-60mV/dec steep SS but with hysteresis. This hysteresis is often not seen in experimental reports. Such hysteresis-free steep SS behavior can be due to the existence of charged defect such as charge trapping and fixed charge. We also incorporate charged defects in FeFET model as shown in Fig. 16 (a). Trap band of FE-HfO_2 such as HZO has been recently explored and identified [28]. We applied the similar defect profile for charge trap and fixed charge in our work. Fig. 16 (b) shows the example of FeFET with HZO gate insulator, where almost hysteresis-free operation with sub-60mV/dec has been obtained [29]. The interaction between

ferroelectric property and such charged defects are important to consider for understanding the device operation.

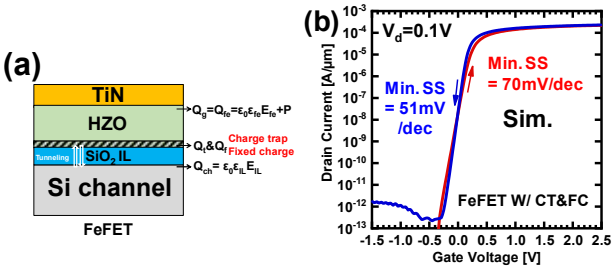

Fig. 16 (a) Schematic of FeFET with charged defects. (b) Simulated I_d-V_g characteristics with the defects.

IV. Summary

In this paper, we overviewed the framework of TNC in FeFET referring to our researches and other groups. TNC provides us physical understanding of steep subthreshold behavior, R-DIBL, NDR, hysteresis-free operation in FeFET. This framework was intended for understanding NCFET but now can be practically applied to FeFET memory application.

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