

Characteristics of Gate-All-Around Silicon Nanowire and Nanosheet MOSFETs with Various Spacers

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Abstract—We estimate DC characteristics and single-charge trap (SCT) induced random telegraph noise (RTN) of gate-all-around (GAA) silicon nanowire (NW) and nanosheet (NS) metal-oxide-semiconductor field effect transistor (MOSFETs) for sub-5-nm nodes. Devices with various dielectric spacers from low- to high- κ including asymmetric dual spacers (ADS) are considered. More than 31% boost on the normalized on-state currents is observed for the explored devices with high- κ and ADS spacers. Similarly, for the normalized off-state currents, more than 50% reduction is achieved. The largest magnitude of the RTN ($\Delta I_D/I_D \times 100\%$) is 6.7% for the nominal GAA Si NS MOSFET with an effective channel width of 40-nm.

Keywords—DC characteristics; SCT; RTN; Gate-all-around; Nanowire; Nanosheet; MOSFETs.

I. INTRODUCTION

Gate-all-around nanowire (NW) and nanosheet (NS) MOSFETs have been of great interest in futuristic technological nodes because of their ultimate channel controllability and high immune to short channel effects (SCEs) [1]–[5]. Ultimately, ultra-small devices suffer from various fluctuations including work function fluctuation, random dopant fluctuation and process variations, interface trap fluctuations, line edge roughness [3],[6]. Furthermore, random telegraph noise (RTN) is a low-frequency noise phenomenon observed in emerging CMOS devices; it changes as discrete jumps in the magnitude of drain current of MOSFETs, due to capture and emission of conduction carriers by single charge trap (SCT) specifically at the interface of channel/oxide [7]. In short-channel devices, the existence of SCT increases the device variability of random telegraph noise (RTN) [8]. Electrical characteristics of silicon GAA NW and NS MOSFETs including FinFETs have recently been reported [4]–[5], [9]–[11]. In GAA NW and NS MOSFETs, the wider cross-section simultaneously affects drive current, electrostatics, and parasitic capacitances. Notably, electrical characteristics MOSFETs can be boosted by using different topologies of spacers [3]. The structural and electrical characteristics differences among FinFETs, GAA NW and NS MOSFETs were reported [11], but the impacts of RTN and spacer technology on these devices have not been clearly discussed yet.

In this study, we explore DC characteristics and RTN induced by the acceptor-type SCT appearing in the middle of the interface between channel and oxide of the explored devices: GAA NW MOSFETs and GAA NS MOSFETs with various spacers. Compared with the conventional SiO_2 spacer ($\epsilon = 3.7\epsilon_0$), the studied device with asymmetric dual spacer (ADS) consisting of 50% SiO_2 and 50% HfO_2 ($\epsilon = 22\epsilon_0$) exhibit interesting DC characteristics and parameters of the short-channel effect (SCE).

TABLE I. THE DEVICE SETTINGS, ACHIEVED DC CHARACTERISTIC AND THE SCE PARAMETERS OF THE 16-NM-GATE GAA NS MOSFET WITH A 40-NM ECW CORRESPONDING TO SUB-5-NM NODES.

Parameters	Settings and Achieved Specification
Gate Length (L_G) (nm)	16
Channel Doping (cm^{-3})	5×10^{17}
Channel Width (W_{ch}) (nm)	5, 6, 10, 15
Channel Height (H_{ch}) (nm)	4, 5, 10
S_{ext}/D_{ext} Length (nm)	5
S/D Doping (cm^{-3})	1×10^{20}
S_{ext}/D_{ext} Doping (cm^{-3})	4.8×10^{18}
EOT (nm) ($T_{\text{SiO}_2} + T_{\text{HfO}_2} \times \epsilon_{\text{SiO}_2} / \epsilon_{\text{HfO}_2}$) ($0.6 + 2 \times 4 / 22$) = 0.9636	0.963
I_{ON} (A)	7.21×10^{-6}
I_{OFF} (A)	5.62×10^{-16}
Threshold Voltage (mV)	260
I_{ON}/I_{OFF} Ratio (A/A)	1.282×10^{10}
SS (mV/dec)	62.8
DIBL (mV/V)	25.9

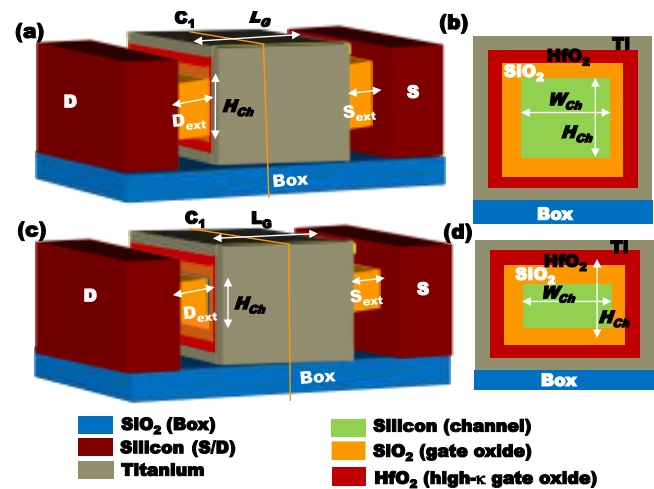


Fig. 1. (a) and (c) are simulated GAA NW MOSFET and GAA NS MOSFET. (b) and (d) are the cross sections of the channel which are 2D cuts (cut-C1) from (a) and (c), respectively.

II. COMPUTATIONAL DEVICES

A 3D quantum-mechanically correction device simulation is intensively performed by solving a set of density-gradient drift-diffusion equations. Physical parameters of the device simulation are firstly validated through the result of the nonequilibrium green function simulation [7],[12]. The thin layer mobility model engaged with mobility degradation at the interface of semiconductor-insulator [13] is also adopted. To provide the best accuracy of device simulation, calibration with measurement has been reported in our recent study [7]. Devices with 16-nm channel length are with a rectangular channel of 20- and 40-nm effective channel widths (ECWs)

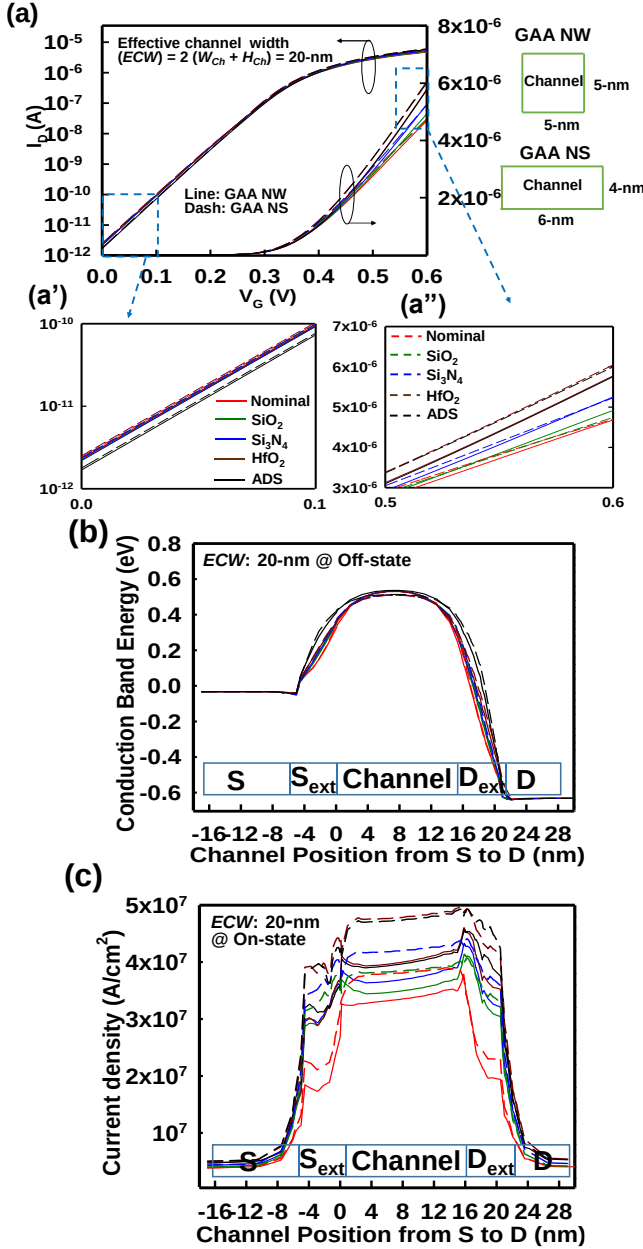


Fig. 2. For the same threshold voltage 260 mV without SCT, (a) simulated I_D - V_G curves of the GAA NW and GAA NS devices with various spacers and a 20-nm ECW. (a') and (a'') Zoom-in plots near the off- and on-state regions. (b) Without SCT, 1D cut views of the off-state ($V_D = 0.6$ V and $V_G = 0$ V) conduction band energy from S to D along the channel for the GAA NW and NS devices with various spacers and the 20-nm ECW. (c) The on-state ($V_D = 0.6$ V and $V_G = 0.6$ V) current density of the GAA NW and NS devices with various spacers and the 20-nm ECW.

are examined, by using the expression as stated in Eq. (1).

$$ECW = 2(W_{ch} + H_{ch}), \quad (1)$$

where W_{ch} and H_{ch} are the width and height of the channel of the explored GAA NW and NS devices. Notably, the 16-nm channel length is correspond to sub-5-nm technological nodes, according to projections of the International Technology Roadmap for Semiconductors [14]. Figs. 1(a)-(d) show the studied devices and cross-sectional views of the GAA NW and NS devices. The simulated structure consists of a titanium metal gate with low- κ (SiO_2) and high- κ (HfO_2) stack, and the effective oxide thickness (EOT) of 0.963 nm, calculated by

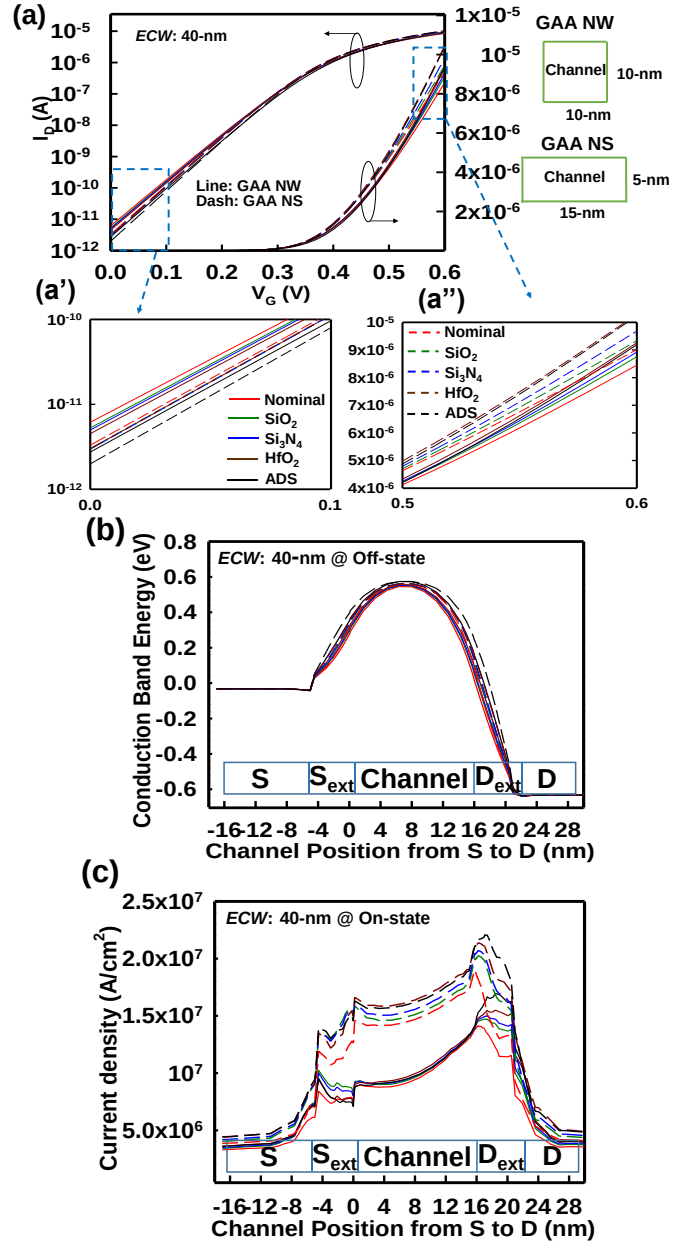


Fig. 3. (a) I_D - V_G curves of the GAA NW and NS devices with various spacers and a 40-nm ECW. (a') and (a'') Zoom-in plots near the off- and on-state regions. (b) Without SCT, 1D cut views of the off-state ($V_D = 0.6$ V and $V_G = 0$ V) conduction band energy from S to D along the channel for the GAA NW and NS devices with various spacers and the 40-nm ECW. (c) The on-state ($V_D = 0.6$ V and $V_G = 0.6$ V) current density of the GAA NW and NS devices with various spacers and the 40-nm ECW.

$$EOT = T_{\text{SiO}_2} + T_{\text{HfO}_2} \times \frac{\epsilon_{\text{SiO}_2}}{\epsilon_{\text{HfO}_2}}. \quad (2)$$

To assess the effect of spacers on device characteristics, we consider the nominal case (i.e., devices without any spacer), low- κ (SiO_2), Si_3N_4 , high- κ (HfO_2), and 50% SiO_2 + 50% HfO_2 for the case of ADS to cover the source (S) and drain (D) extensions [3].

The adopted device parameters and the achieved characteristics including SCE parameters are listed in Table I, for the nominal n-type device. According to our recent study [7], we assume that SCT has a rectangular shape with $(2 \text{ nm})^3$ at the middle of the interface between channel and oxide.

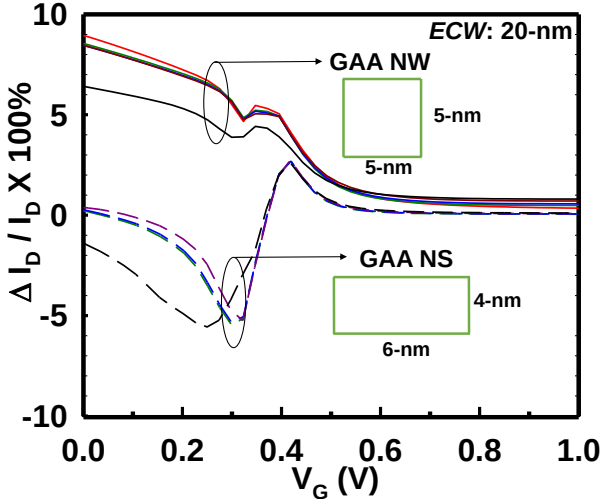


Fig. 4. (a) and (b) The statistically calculated magnitude of the RTN induced by the SCT locating at middle of the surface of the channel, under the biasing of $V_D = 0.01$ V and $V_G = 1$ V for both the GAA NW and NS MOSFETs with various spacers of the 20-nm ECW.

To explore the most severe impact of SCT on RTN, the density of interface trap (D_{it}) of $5.6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ is assumed for all stated devices [7].

III. RESULTS AND DISCUSSION

In order to investigate the difference stemming only from the different geometries of GAA NW and NS MOSFETs, it is necessary to impose similar threshold voltage for all devices. The transfer characteristics for all nominal devices are tuned to the same threshold voltage (V_{th}) at 260 mV by adjusting the metal work function. The I_D - V_G curves of the devices with the 20-nm ECW, as shown in Fig. 2(a), show the comparison among the aforementioned devices with various spacers. The comparison reveals that the impact of spacers on the enhancement of the on-state current and the reduction of the off-state current which are further examined via the zoom-in plots, as shown in Figs. 2(a')-(a''). It is not shown here, first we cut from the simulated 4D results to a 3D plot of the conduction band energies for the devices with the 20-nm ECW. Then, the 3D plot is further sliced into a 2D off-state conduction band energy. As shown in Fig. 2(b), the devices with all spacers are plotted together. Similarly, the on-state current densities of the 20-nm ECW are shown in Fig. 2(c). Furthermore, the I_D - V_G curves of the devices with the 40-nm ECW, as shown in Fig. 3(a), compare the devices with aforementioned various spacers. The comparison reveals that the impact of spacer on the enhancement of the on-state current and the reduction of the off-state current are further examined as zoom-in results shown in Figs. 3(a')-(a''). The off-state conduction band energy profiles of the devices with the 40 nm ECW are shown in Fig. 3(b). In addition, the on-state current densities of the devices with the 40-nm ECW are shown in Fig. 3(c). The majority of electron transport is controlled through large overlapped gate along the channel direction; therefore, the scattering of electrons can be effectively controlled in GAA NS MOSFETs that resemble low off-state current; thus, the conduction band energy is higher during the off-state in the GAA NS MOSFET compared to the NW one. For the GAA NS MOSFET with the ADS, the highest normalized on-state current is increased by 31.4%; similarly, a 65.4% reduction on the normalized off-state current is observed, as shown in Figs. 2(a) and 3(a). At high gate bias, the fringing electric field will penetrate from

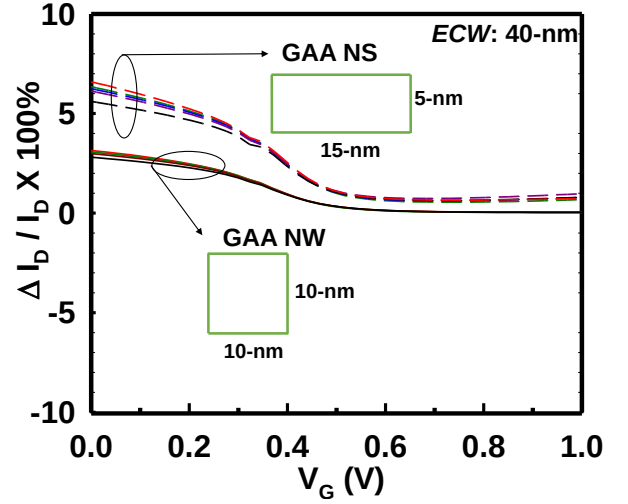


Fig. 5. (a) and (b) The statistically calculated magnitude of the RTN induced by the SCT locating at middle of the surface of the channel, under the biasing of $V_D = 0.01$ V and $V_G = 1$ V for both the GAA NW and NS MOSFETs with various spacers of the 40-nm ECW.

the S/D extension regions owing to heavy dopant; thus, the gate fringing electric field cannot change the resistance of S/D extensions. This leads to a relatively high on-state current and low off-state currents. We do study the relationship of the dielectric constant and characteristics are further examined by observing the off-state conduction band energy profiles of the 20- and 40-nm ECWs, as shown in Figs. 2(b) and 3(b), respectively. The higher conduction band energy at off-state leads to lower off-state current; therefore, the ADS spacer records high conduction band compared to other spacers. Similarly, for the on-state, due to the extension in the spacer region constitutes for a high fringing electric-field area that leads to high current density, thereby improving the on-state current, as shown in Figs. 2(c) and 3(c) for the 20- and 40-nm ECWs, respectively. Both the GAA NW and NS MOSFETs with the ADS spacer reports high electric field compared to other spacers; thus, the ADS records high on-state current for both devices in Figs. 2(c) and 3(c). The effect of spacers on SCEs for both the GAA NW and NS MOSFETs with the 20- and 40-nm ECWs are compared and listed in Table II. The comparison results reveal that the I_{ON}/I_{OFF} current ratio is increased for the GAA NS and NW MOSFETs from low- to high- κ spacers. The extracted parameters of SCE are suppressed for the GAA NS MOSFETs compared to the GAA NW MOSFET from low- to high- κ spacers.

It has been explored that the magnitudes of RTNs induced by SCT are significant in planar MOSFETs and bulk FinFETs [7]; however, the explored GAA NW and NS MOSFETs have improved immunity to the impact of SCT. Fig. 4 shows the magnitude of RTN induced by SCT of the devices with the 20-nm ECW. For the 20-nm-ECW, the channel height of the nominal GAA NS MOSFET is similar to the GAA NW device, owing to strong gate controllability which leads to higher immunity to SCT, as shown in Fig. 4. The magnitude of RTN induced by SCT of the devices with the 40-nm ECW is shown in Fig. 5. However, the largest magnitude of RTN is 6.7% (about 3% for the case of GAA NW device) in Fig. 5 for the GAA Si NS MOSFET with the 40-nm ECW. The off-state current of the GAA NS MOSFET is lower than that of the GAA NW one at small V_G . When V_G increases, the device starts to induce channel and conduct, vast conduction carriers are generated in the channel which enhances the SCT capture

TABLE II. WITHOUT SCT, COMPARISON OF THE SIMULATED AND EXTRACTED SCE PARAMETERS, STATISTICALLY CALCULATED MAGNITUDES OF RTN FOR THE GAA NW AND NS MOSFETs WITH A 20 AND 40-nm ECWs AND VARIOUS SPACERS. THE COMPARISON IS WITH THE SAME THRESHOLD VOLTAGE OF 260 mV. THE CASES OF THE NOMINAL SPACER ARE THE DEVICES WITHOUT SPACERS. NOTABLY, FOR THE CASES FROM LOW- TO HIGH-k, THE SIMULATED SCE OF ALL DEVICES ARE IMPROVED.

Device		20-nm ECW		40-nm ECW	
Spacer	Parameter	GAA NW MOSFET	GAA NS MOSFET	GAA NW MOSFET	GAA NS MOSFET
Nominal	I_{ON}/I_{OFF} Ratio	3.5×10^9	3.4×10^9	1.32×10^9	3.7×10^9
	SS (mV/dec)	61.3	61	66.8	63.4
	DIBL (mV/V)	11	10.2	44	25
	Max. RTN ($\Delta I_D/I_D \times 100\%$)	8.9	0.3	3.1	6.7
SiO ₂	I_{ON}/I_{OFF} Ratio	4×10^9	3.6×10^9	1.7×10^9	4.4×10^9
	SS	61.4	61.2	66.2	63.2
	DIBL	10.8	9.6	41	22
	Max. RTN	8.8	0.26	2.7	6.12
Si ₃ N ₄	I_{ON}/I_{OFF} Ratio	4.2×10^9	3.95×10^9	1.9×10^9	4.6×10^9
	SS	61.2	61.3	66.1	63.3
	DIBL	10.8	9.5	40	22
	Max. RTN	8.4	-0.8	2.8	6.05
HfO ₂	I_{ON}/I_{OFF} Ratio	5.7×10^9	4.22×10^9	2.24×10^9	4.9×10^9
	SS	61.2	61	65.4	63.2
	DIBL	12	9.2	39.6	23
	Max. RTN	8.2	-1.2	2.72	6
ADS	I_{ON}/I_{OFF} Ratio	6.5×10^9	6.2×10^9	4.23×10^9	8.3×10^9
	SS	60.9	60.9	64.3	62
	DIBL	9.4	9	32.7	19
	Max. RTN	6.4	-1.9	2.48	5.5

and emission of carriers; consequently, it leads to large magnitude of RTN. It is because of that the magnitude of RTN is essentially dependent on the conducting carriers in the channel. It is also inferred that for all spacer devices, the increase in spacer dielectric further reduces the tunneling gate leakage there by a reduction in the magnitude of RTN.

IV. CONCLUSIONS

In summary, the reported rectangular shape channel GAA NW and NS MOSFETs has been studied for the DC and RTN induced by SCT with various spacers materials. The ADS has wonderful characteristics compared to other spacer materials; in particular, for the off-state current, it is about 65.4% reduction and the boost of on-state current is up to 31.4% for the GAA NS MOSFET of 40-nm ECW. We have explored the impacts of the SCT on the RTN for the GAA NW and NS MOSFETs. Thus, the influence of RTN (at low gate bias) is more significant in GAA NW MOSFETs compared to GAA NW MOSFETs at scaled ECWs.

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