High-sigma analysis of DRAM write and retention performance: a TCAD-to-SPICE approach

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***Abstract*—This paper presents a TCAD-to-SPICE high-sigma analysis of DRAM write and retention performance. Both statistical and process-induced variability are taken into-account. We highlight that the interplay between discrete traps and discrete dopants is ruling the leakage statistical tails and therefore can play a fundamental role in determining yield and reliability of ultra-scaled DRAMs.**

Keywords—DRAM, leakage, retention time, DTCO, TCAD.

I. Introduction

Continuing efforts in advancing DRAM process technology have enabled dramatic feature-size reduction and unprecedented levels of integration [1-4]. However, the resulting increase in memory density per chip comes at the expense of increased severity of parasitic effects [5]. In particular, during the design cycle, attention has to be put on the DRAM cell transistor leakage current, which dictates DRAM refresh time (tREF) and, in turn, affects manufacturing yields. It is of utmost importance to highlight that the ultimate failure in the tREF performance is not governed by the average cell behaviour, but by the leakage current of extreme-tail cells ($<10^{-6}$ probability). These cells may exhibit a few orders of magnitude higher leakage than the nominal cell, with a statistical distribution that is influenced by both process (e.g. geometry, doping profiles) and intrinsic statistical variability (e.g. random discrete dopants, random traps). Innovative characterization techniques have been proposed to experimentally evaluate the DRAM cell transistor leakage current distributions [6]. Of equal importance becomes the availability and timely deployment of modelling platforms that enable the Design-Technology Co-Optimization (DTCO) of DRAM circuits to evaluate and optimize tREF in the presence of process and statistical variability with reduced requirements on costly and slow silicon manufacturing cycles.

II. Simulation Methodology

In this paper we present a TCAD-to-SPICE modelling approach enabling the early injection of statistical metrics into the design/optimization cycle. The flow, which allows accurate and extensive exploration of the design space by taking into account both leakage (tREF) and writing (tWR) statistical behaviour and their correlation, consists of the following steps (Fig.1): (i) accurate process structure generation by means of Process Explorer (layout to 3D structure) and Sentaurus Process (doping profiles) [7-8] to capture process and doping profile variations, (ii) accurate device simulation of the nominal transistors by means of Sentaurus Device [9], (iii) Garand VE [10] for the physics-based variability simulation of trap-assisted leakage current in presence of random discrete dopants (RDD), (iv) Mystic [11] to extract statistical compact models, and (v) RandomSpice [12] for generation of models at arbitrary trap densities in statistical SPICE simulations.

It has been previously shown that discrete doping can play a fundamental role in determining the stochastic dispersion of band-to-band tunnelling in transistors [13]. Here, we also take into account the trap-assisted band-to-band tunnelling (TAT), as the measurements clearly show that the transistor leakage current is a function of the number of defects in silicon, their energy level in the bandgap, and the electric field [6]. The trap-assisted contribution is modelled through an enhancement of the trap capture cross-section in the conventional Shockley-Read-Hall (SRH) generation term. The enhancement can either be computed by Hurkx-like local models or by non-local tunnelling path approaches. Garand VE simulates hundreds of statistical RDD instances for each process condition under consideration. For each RDD configuration, thousands of single-trap positions are evaluated to gather the TAT leakage statistics. Arbitrary trap density statistics can then be obtained later in RandomSpice by convolution of the single-trap cumulative distribution functions (this assumes single traps to act as independent entities).

III. TCAD Simulation Results

The DRAM test structure used for this study (Fig.2) is representative of a $6F^2$ cell with features reported in the side table.

The 3D structures are generated, for different process conditions, by using Process Explorer, which allows for fast, yet accurate, structure generation. The parameters *WLetch* and *Dose* (roll-off) are varied to generate a range of structures corresponding to different process conditions, or process variations.

A. RDD simulation results

Initial Garand VE analysis was performed to evaluate the impact of RDD on the on-current for the DRAM cell, across the *WLetch* and *Dose* process variations space, showing a 10% variation in the mean on-current (Fig.3). Furthermore, the on-current standard deviation also shows a consistent process-dependence, varying from 3% to 6% of the nominal on-current value and, hence, highlighting the interplay

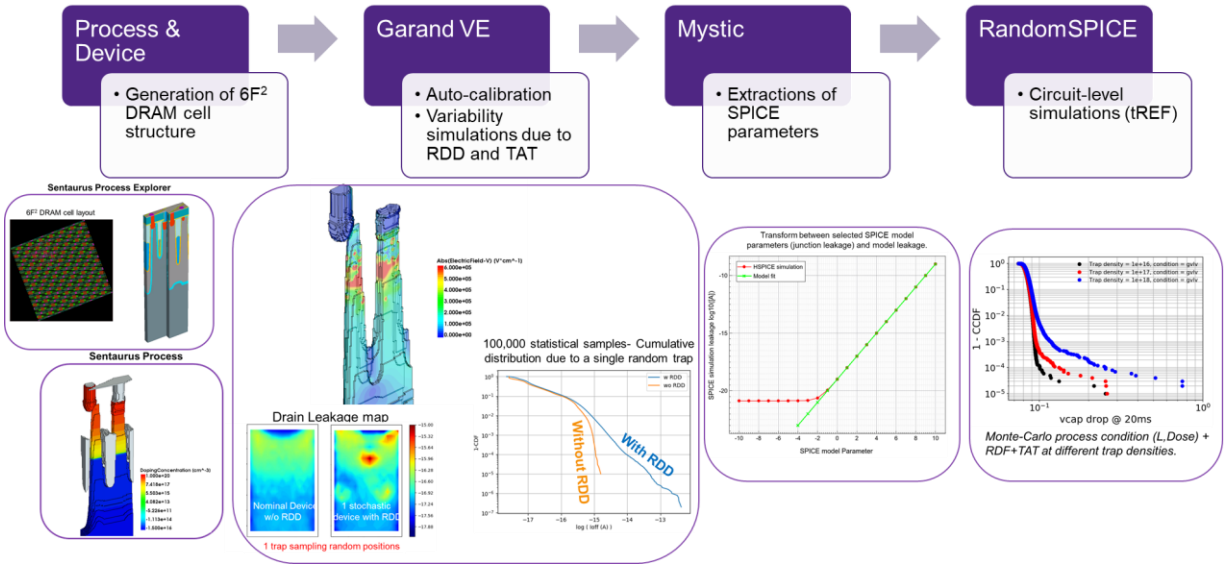
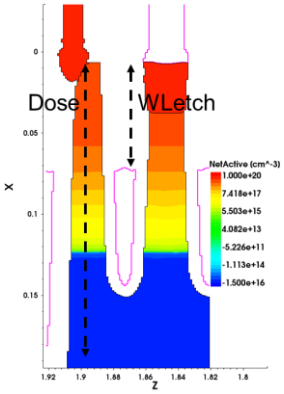


Figure 1:TCAD-to-SPICE flow for the high-sigma analysis of DRAM write and retention performance, consisting of: (i) layout-based structure generation and process emulation, (ii) device simulation of the nominal transistors, (iii) physics-based variability simulation of trap-assisted leakage current in the presence of random discrete dopants, (iv) statistical compact model extraction, and (v) model card generation at arbitrary trap densities in statistical SPICE simulation.



Critical Dimensions

WLetch	60nm
Peak Dose	2e19cm^{-3}
Technology node	2z nm

Electrical Parameters

V(core)	1V
V(bulk)	-0.8V
V(wl,low)	-0.2V
V(wl,high)	3.0V
tREF	64ms

Figure 2: (left) cross-section of generated DRAM cell structure, corresponding to a 6F^2 technology. (right) table of critical dimensions and electrical parameters for the DRAM structure under test.

between process and statistical variability. The results of the analysis can be understood by considering that the combination of *WLetch* and *Dose* define the gate to source/drain overlap. With a high *WLetch*, there is significant underlap, leading to low on-current and high variability.

B. Single trap analysis

We consider 200 RDD configurations. For each of them we sweep a single trap position across the silicon area under investigation (the drain pillar region) with a 0.5nm spacing, leading to ~70,000 trap evaluations per each RDD configuration (14,000,000 trap configurations for each simulated process condition). Results in Fig.4 highlight that the interaction between traps and random dopants can enhance the leakage. In this case we see a greater than 10x increase in leakage at 10^{-5} probability level and, moreover, the tail of the distribution is now unbounded. Fig.5 shows the map of leakage as a function of the trap vertical position, highlighting that the peak of the leakage is determined by the

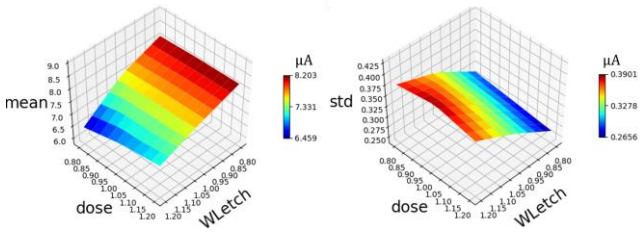


Figure 3: Mean ON-current (left) and its standard deviation (right) across the space of process variation. The plot on the right highlights the clear interplay between statistical and process variability.

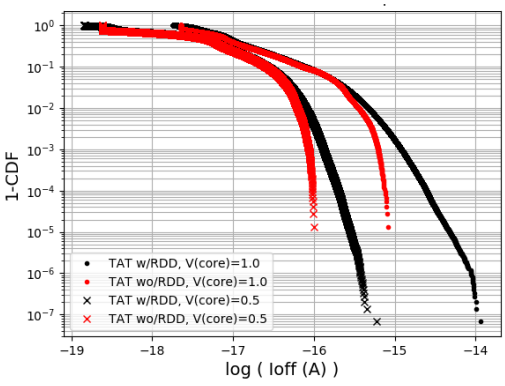


Figure 4: Complementary CDF of single trap leakage. The "w/RDD" plot represents 200 RDD configurations with ~70,000 trap evaluations per RDD configuration. The "wo/RDD" is instead obtained for a device featuring a continuous doping profile.

p-n junction and, therefore, by the process conditions (Fig.6). The leakage tail is also strongly influenced by process conditions, with *WLetch* and *Dose* having a reverse impact on leakage compared to I_{on}, with worst case leakages encountered when *WLetch* is small (i.e. the metal gate gets closer to the storage capacitor).

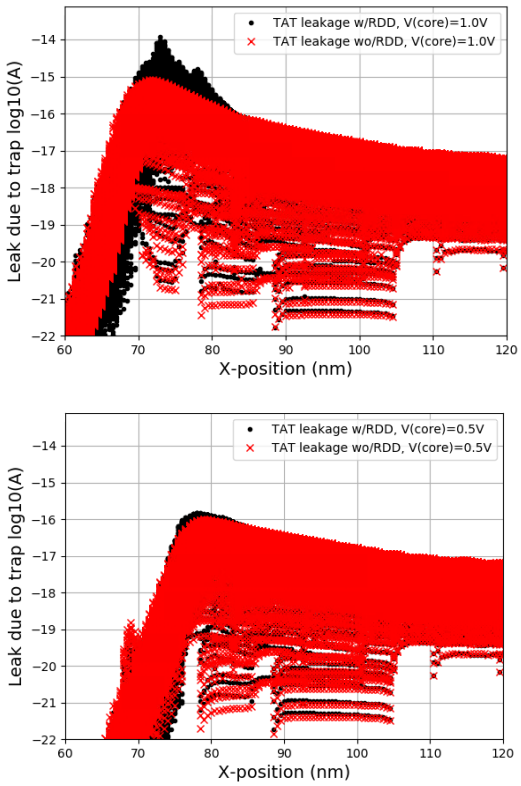


Figure 5: (top) Map of trap-related leakage against vertical position along the source/drain pillar connected to the storage capacitor, at V(core)=1.0V. (bottom) The same picture, at V(core)=0.5V.

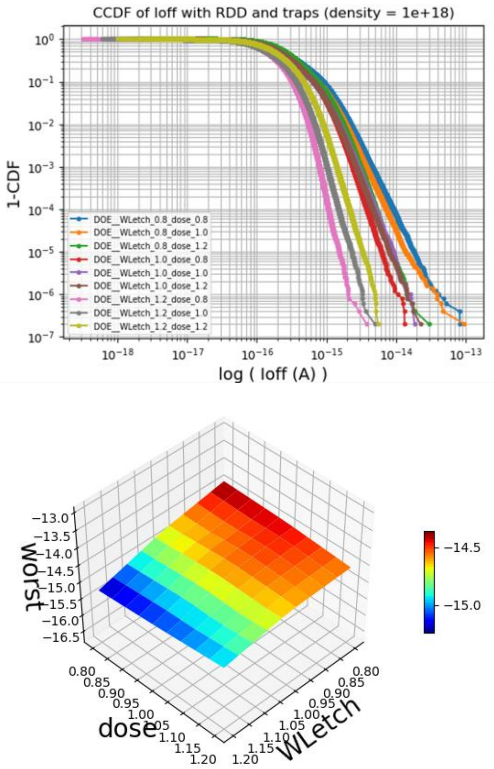


Figure 6: (top) Leakage distributions for each process condition showing ~2 orders of magnitude difference in tail leakage for this set of experiments. (bottom) tail leakage values across different process conditions, highlighting a clear interplay between process and statistical variability also for the leakage behaviour.

C. *Arbitrary trap density*

The results for many traps can be obtained analytically by self-convolution of the single-trap statistics. Fig.7 confirms the validity of the approach, by comparing analytical results with full TCAD simulation.

IV. SPICE Simulation Results

The simulated TCAD data is then propagated into a SPICE model. For each Monte-Carlo instance of the DRAM cell, a unique leakage current is generated using the fitted TCAD data distributions. These randomised leakage values are then converted to BSIM4 junction leakage parameters. To verify the SPICE model is reproducing the TCAD data, Fig.8 shows the leakage complementary cumulative distributions from the TCAD fitting and leakage values extracted from the SPICE model. Because leakage values are directly generated, it becomes simple to skip any SPICE simulation where leakage current is not high enough to cause cell failures. In Fig.8, SPICE simulations are only enabled for circuits where the DRAM cell leakage current at nominal bias >1 fA. As a result, only ~400k of 10M (representing roughly 10Mbit) SPICE tWR+tREF simulations were run – enabling high-sigma analysis. Finally, SPICE simulations were run combining on-current and leakage variability where a write-then-hold operation was performed. The results of these simulations are shown in Fig.9, where the left figure shows (target - final storage voltage), and the right figure shows storage voltage after a 64ms hold. The simulations are performed at 3 process conditions, which are described in Table 1.

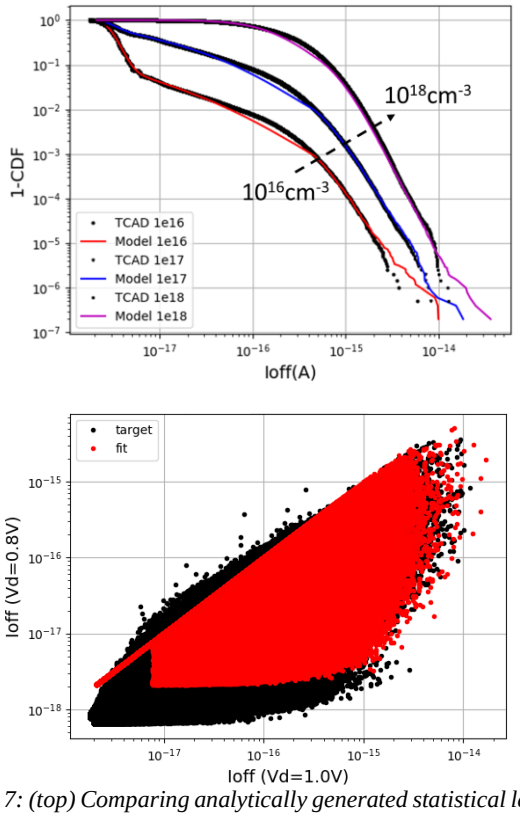


Figure 7: (top) Comparing analytically generated statistical leakage (obtained by convolution of the single trap distribution) vs TCAD-generated data for different trap densities. (bottom) The analytical generation is also able to maintain good agreement with TCAD data with respect to drain bias dependence (here shown for the case of single trap).

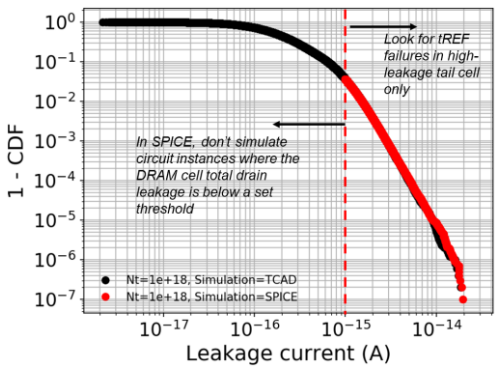


Figure 8: CCDF of leakage current in the DRAM cell: TCAD vs SPICE simulation. The SPICE tail methodology allows fast and reliable high-sigma analysis.

Process Conditions Definitions			
	lv	lv + worst_gv	lv + best_gv
WLetch	1.0	0.8	1.2
Dose	1.0	0.8	0.8
4.5σ voltage underwrite	29mV	22mV	50mV
4.5σ hold voltage drop	70mV	110mV	24mV

Table 1 Process conditions for the statistical circuit simulation analysis reported in Figure 10.

Finally, the results shown in Fig.10 provide a quantitative analysis of the trade-offs between better write behaviour (tWR), and better leakage (tREF).

V. Conclusions

We have presented a TCAD-to-SPICE methodology for the high-sigma analysis of DRAM write and retention performance. This modelling platform can enable the Design-Technology Co-Optimization (DTCO) of DRAM circuits to evaluate and optimize tREF in the presence of process and statistical variability.

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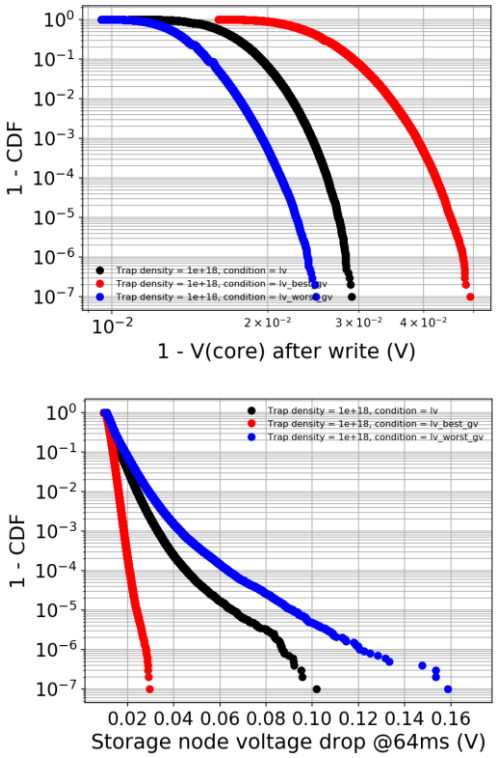

Figure 9: (top) Delta V(core) distribution after a write operation, representing variability in on-current due to random dopant fluctuations. (bottom) Distribution of storage capacitor voltage drop (relative to final storage node voltage value), after 65ms hold time.

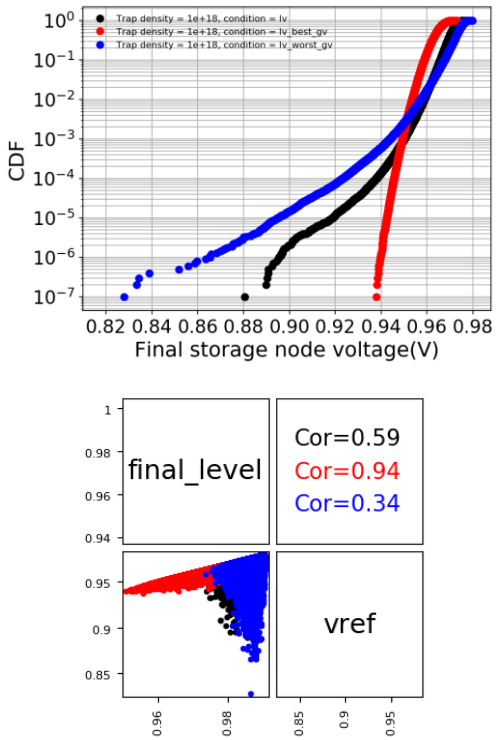

Figure 10: (top) Final storage capacitor voltage after a write and 64ms hold operation. (bottom) scatter plot of final storage node voltage after write (final level) vs. final storage node voltage after write and 64ms hold. The red data points represent worst tWR/best tREF process conditions, the blue represents best tWR/worst tREF conditions, and black the "typical" case.