High-Performance Metal-Ferroeletric-Semiconductor Nanosheet Line Tunneling Field Effect Transistors with Strained SiGe

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***Abstract*—Nanosheet line tunnel-field effect transistors (NLTFETs) are for the first time proposed by utilizing the advantages of ferroelectricity through HZO materials. Three ferroelectric line TFETs have been proposed and investigated. Among these, the metal-ferroelectric-semiconductor (MFS) structure has shown superior performance than the other two variants. The factors of electric field and electron barrier tunneling have been addressed to govern the performance of these structures. In addition, the effects of the ferroelectric ($Hf_{0.5}Zr_{0.5}O_2$) thickness (t_{FE}) and the dielectric constant have been discussed. The MFS NLTFETs can effectively utilize the advantages of ferroelectric than the other variants. High on-current of 175.6 μA/μm and low off-current of 38.4 aA/μm are achieved at t_{FE} of 4 nm through proper utilization of gate-overlap on to the drain side. Furthermore, the proposed MFS structure successfully delivers low average and minimum subthreshold swings even at very thin t_{FE}.**

***Keywords—Nanosheet line TFETs*, *MFS*, $Hf_{0.5}Zr_{0.5}O_2$, and *SiGe*.**

I. Introduction

The tunnel-field effect transistors (TFETs) are promising aspirants for future energy-efficient electronics. In this prospective, band-to-band tunneling (BTBT) is the principal mechanism that governs DC characteristics of TFETs. Nevertheless, TFETs suffer from low tunneling probability due to its limitations in tunneling length or width (λ) and barrier height ($\Delta\Phi$). Hence, major investigation is carried out by considering various semiconductors (e.g., direct bandgap and 2D materials) to increase the tunneling probability [1]–[3]. Alternatively, this limitation is also overwhelmed to some extent through the excess field generations with the concept of line tunneling [4]. Even though various options of using line tunneling concepts have been proposed [5]–[8] the completely scaled n-epitaxial layer geometry has shown most promising choice in improving the tunneling probability [9], [10].

The ferroelectric utilization on TFETs is proved to be an alternative and a proficient option in further improving the limitations [11]–[14]. This is mainly due to the enhancement of internal voltage at source-channel junction that provides excess source to enhance the tunneling probability at low applied potentials. Thus, ferroelectric not only improves the on-current (I_{on}) but also enhances the steepness of the slope under sub-thermionic emission. Hence, the line TFETs (efficient than point-TFETs) with utilization of ferroelectric is the effective choice and need to be addressed [14].

TABLE I. Device Specifications and Materials Used

Parameter	Material	Value
Gate length (L_G)	TiN	15 nm
Channel length (L_{ch})	Silicon	10 nm
Channel thickness (t_{Ch})	Silicon	5 nm
Channel width (W)	Silicon	10 nm
Source-overlap length (S_{OV})	$Si_{1-x}Ge_x$	5 nm
Gate-overlap on drain (D_{OV})	Silicon	5 nm
Gate oxide thickness (t_{ox})	HfO_2	3 nm
Ferroelectric layer thickness (t_{FE})	$Hf_{0.5}Zr_{0.5}O_2$	4 nm
Gate-metal thickness (t_G)	TiN	3 nm
Gate-electrode work-function	TiN	4.4 eV
Source doping concentration (p^{++})	Boron	5×10^{20}
Channel doping concentration (p)	Boron	1×10^{16}
Drain doping concentration (n^+)	Arsenic	1×10^{19}
Epitaxial doping concentration (n)	Arsenic	5×10^{18}

The metal-ferroelectric-insulator-semiconductor (MFIS) metal-ferroelectric-metal-insulator-semiconductor (MFMIS), and the metal-ferroelectric-semiconductor (MFS) are the possible options that have been realized as negative capacitance (NC) FETs [15]–[17]. The basic advantage of the MFMIS is eliminating the leakage current by controlling the equipotential surface through the extra metal layer. However, the MFMIS structures are experimentally failed in utilization of polarization effect. Considering MFIS structures that utilizes the benefits of NC but not fully by the semiconducting channel due to the existence of dielectric layer. Apart from MFIS and MFMIS, the MFS structures have been shown exceptionally well in utilizing the benefits of ferroelectricity to improve the device characteristics by the use of 2D materials in delivering ultra-low power consumptions and reducing the switching time of various applications [17].

On the other hand, FETs with nanosheet structures are promising in emerging devices owing to their controllability in sinking scattering of electrons/holes and in generating sufficient fields for TFETs. In addition, nanosheet devices can be more beneficial for high-packed density with its reduced effective width of the device [18]. Notably, devices with nanosheet structures are also considered as effective choices in ultrascaled technology nodes, such as sub-5-nm [19]–[21]. Thus, we first demonstrate the nanosheet line TFET (NLTFET) with a MFS structure and compare with other variants of MFMIS and MFIS. The rest of the paper is organized as follows: design and simulation of the explored NLTFET are shown in Sec. II. Results and discussion on the specified structures are shown in Sec. III. Conclusions are listed in Section IV.

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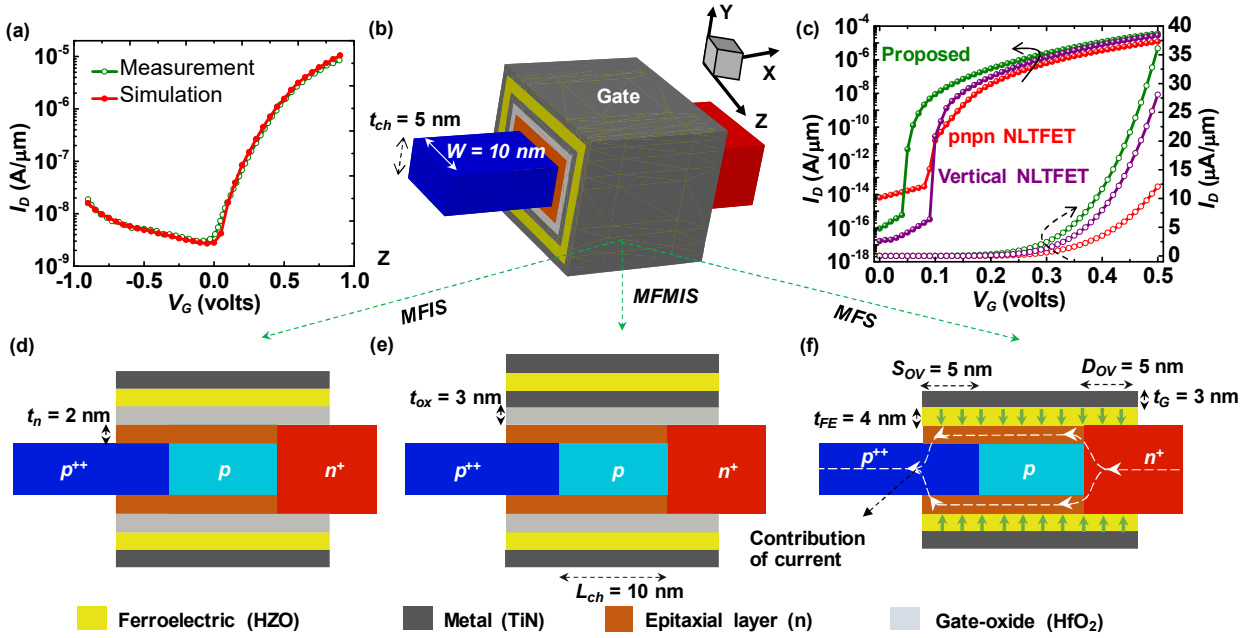

Fig. 1. (a) Validation of simulated data with experimental data [24]. (b) Proposed structures of NLTFETs with (d), (e) and (f) as MFIS, MFMIS, and MFS (with internal line TFET specifications), respectively. The doping concentrations of regions source (p^{++}), channel (p), epitaxial layer (n), and drain (n^+) are considered as 5×10^{20}, 1×10^{16}, 5×10^{18}, and 1×10^{19} cm^{-3}, along with the work-function as 4.4 eV. (c) Comparative analyses on the proposed structure (MFIS) with existed simulations [22], [28]. Note that the ferroelectric pnpn NLTFET and Vertical NLTFET in are designed and modelled as MFIS NLTFETs, based on the internal structure shown in [22], [28].

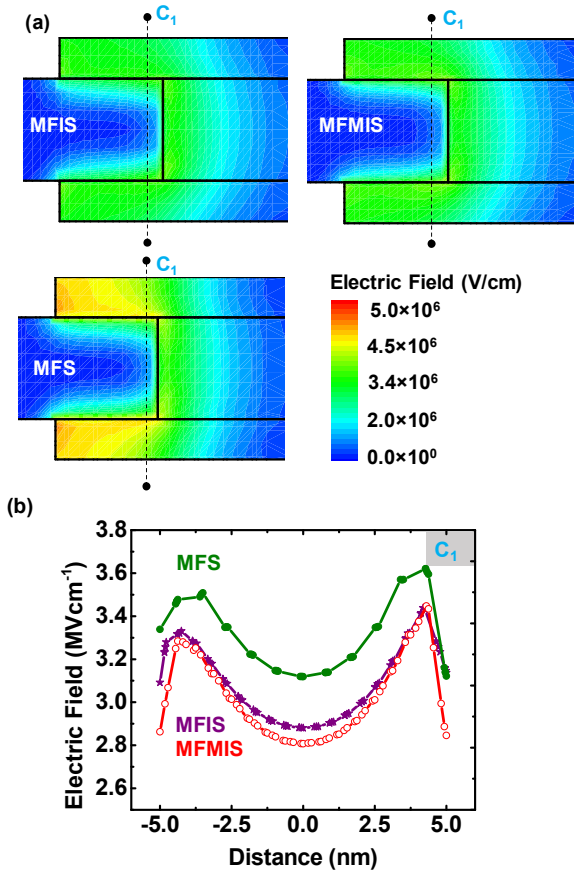

Fig. 2. (a) The electric field profile distributions and (b) its variation through n-epitaxy-source regions (along the cut-line C_1) for the proposed structures of MFIS, MFMIS, and MFS based NLTFETs.

II. Device Modelling and Simulation

To design and analyze the TFETs, 3D device simulations are performed, where the band-to-band tunneling models as dynamic nonlocal tunneling and Hurkx trap-assisted tunneling (TAT) are calibrated with respect to the material considerations ($Si_{1-x}Ge_x$, where x as the Ge fraction and HfO_2 as dielectric) [9]. The simulations are experimentally validated for ferroelectric TFET, as depicted in Fig. 1a [24]. In addition, the proposed device performance is estimated through reasonable comparison with recently explored architecture, can be found in Fig. 1c [22]. The material properties of $Hf_{1-x}Zr_xO_2$ with Zr fraction (x) of 0.5 is a suitable option in delivering the significant polarization and electric fields [23], [24]. Furthermore, $Hf_{0.5}Zr_{0.5}O_2$ has the superior band alignment with Si and $Si_{0.6}Ge_{0.4}$ respectively, therefore the devices with these material choices can be able to achieve low leakage currents even at highly scaled ferroelectric thickness (t_{FE}) [25]. The designed and simulated structures naming ferroelectric NLTFETs as MFIS, MFMIS and MFS are illustrated in Figs. 1b, d-f based on the specifications as listed in Table I.

III. Results and Discussions

Distributions of the electric field in the proposed structures along the cut-lines C_1 are depicted in Fig. 2. It can be observed that the MFS NLTFETs can able to utilize the ferroelectric polarization effectively and there by producing significant field compared to MFIS and MFMIS structures. In addition, the surface potential can be further improved through the reduction of oxide capacitance (C_{ox}), thus achieving more internal voltage (V_{int}) through ferroelectric capacitance (C_{FE}) [26]. Hence, the expression for internal voltage generated through MFS structure can be modified to (by neglecting C_{ox})

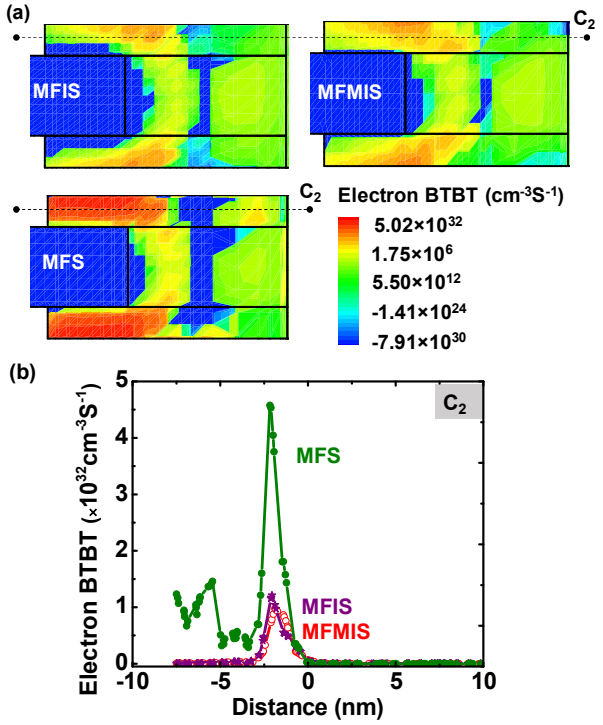

Fig. 3. (a) The distributions of electron BTBT on the proposed structures (MFIS, MFMIS, and MFS), (b) including their tunneling rate along the cut-line C_2 (contributor of line tunneling).

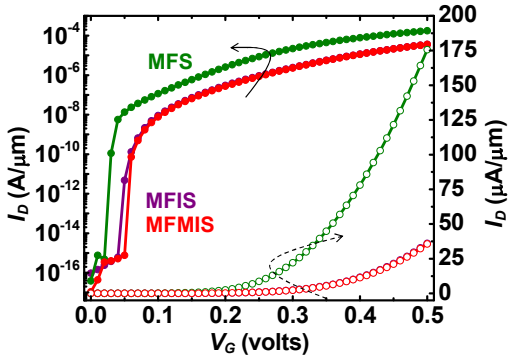

Fig. 4. The I_D-V_G characteristics of MFS, MFIS and MFMIS structures at the bias level of $V_D = V_G = 0.5$ V and at t_{FE} of 4 nm.

$$V_{\text{int}} = \frac{V_{gate}}{1+\frac{C_{NS}}{C_{NS}}\left(\frac{1}{C_{FE}}\right)}, \quad (1)$$

where, V_{gate} as the applied voltage and C_{NS} as the nanosheet capacitance. Therefore, it is understood that the negative capacitance effect is fully utilized by reducing the series capacitance (or C_{ox}) [17]. Eventually, the electron BTBT can be replicated as stronger (line/vertical tunneling) for MFS structure than other structures. This is because the reduction in oxide thickness reduces the screening tunneling length as well, based on the expression

$$\lambda = \sqrt{\frac{\varepsilon_{NS}}{\varepsilon_{ox}} t_{ox} t_{NS}}, \quad (2)$$

TABLE II. EXTRACTED DC RESULTS OF MFS AND MFIS NLTFETS

Structure	t_{FE} (nm)	I_{off} (aA)	I_{on} (μA)	V_t (V)
MFS FeLTFET	5	34.63	211.46	0.215
	4	38.36	175.6	0.210
	3	38.96	211.56	0.209
	2	36.01	188.56	0.210
	1	34.06	187.7	0.213
MFIS FeLTFET	5	91.6	37.3	0.315
	4	94.3	36.1	0.318
	3	94.5	35.5	0.321
	2	127.23	32.6	0.327
	1	138.1	34.2	0.321

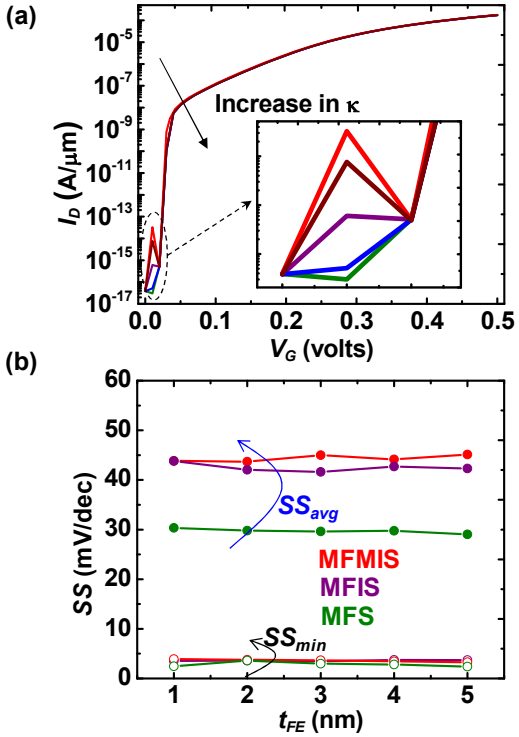

Fig. 5. (a) The extracted I_D-V_G for variation in dielectric constant (κ) of the $Hf_{0.5}Zr_{0.5}O_2$ on MFS NLTFET structure. Inset shows the off-state current fluctuation for increased κ (red to green) at t_{FE} of 4 nm. (b) The observed SS_{min}, SS_{avg} for the proposed structures by scaling t_{FE}.

where ε_{NS}, ε_{ox}, t_{NS}, and t_{ox} are the dielectric constant and thicknesses of the nanosheet (semiconductor) and oxide materials. Hence, the tunneling probability as specified in Fig. 3 can be significantly improved to two orders of electron BTBT rate for the MFS NLTFETs. Since, the coercive field (E_c) strongly correlated on tunneling mechanism and thus corresponds to an increased the tunneling rate. The performance of proposed structures (three variants) at t_{FE} of 4 nm is depicted in Fig. 4. It is understood that the on-current boost is approximately 5 times higher than the MFIS structure (understood from Table II). Interestingly, good agreement with I_{off} is achieved, even for reduced t_{FE} due to wrapped around gate and gate-overlap on to drain (D_{OV}). However, the controllability of negative-capacitance regime in MFS structure's is difficult than the MFIS/MFMIS structures [17]. Thus the I_{off} at low bias levels is observed to be fluctuated upon scaled t_{FE} (can be seen from Fig. 4). The extracted I_{on}

state that the controllability of negative capacitance is the crucial factor in the absence of dielectric. Thus, the fluctuated I_{on} can be seen for the scaled t_{FE} as listed in Table II. In addition, based on the matched C_{FE} with that of C_{NW}, the high I_{on} can be seen at the t_{FE} of 3 nm with reasonable I_{off}. However, the fluctuation in threshold voltage is insignificant. It means, the higher gate-bias and very low bias levels are critical in controlling the MFS structures. Furthermore, the scalability of dielectric constant (κ) in $Hf_{0.5}Zr_{0.5}O_2$ is analyzed in MFS structures and is depicted in Fig. 5a. As like MFIS structures, the MFS structures are also invariant for variation in κ values, except at the off-state condition, can be seen in Fig. 5a. Because, the variation in capacitance is crucial for varied dielectric thickness and which is negotiate at high potential levels [27]. The performance of average and min subthreshold swing swings (SS_{min} and SS_{avg}) are extracted and depicted in Fig. 5b. The results state that the factor of average subthreshold swing is greatly improved through major impact of ferroelectric polarization below the subthreshold regime. This is due to enhanced transport mechanism MFS structures is made steeper SS_{avg} than either MFIS or MFMIS structures. In addition, the results state that these values are consistent upon highly scaled t_{FE} values (viewed from Fig. 5b). Therefore, we state that the MFS based NLTFETs are delivering superior performance, provided that the controllability should be properly maintained. Nevertheless, the proposed structure has been made for the needs of high-drive current and low I_{off} with very good average and minimum subthreshold swings.

IV. Conclusions

We have designed and studied three types of ferroelectric NLTFETs with $Si_{0.6}Ge_{0.4}$ as source. The relevant discussions on the device performance has been addressed with physical constraints of electric field and BTBT on the proposed structures (MFS, MFIS, and MFMIS). Among all, the MFS based NLTFETs has been delivering superior performance in terms of I_{on}, I_{off} and well maintained V_t. Furthermore, the low and steeper subthreshold swings have been achieved on the proposed MFS structure. Thus, we conclude that the proposed structure has been made in delivering superior DC performance with the needs of high-drive current and low I_{off} with very good average and minimum subthreshold swings.

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