# Automatic Device Model Parameter Extractions via Hybrid Intelligent Methodology

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***Abstract*—We report an advanced hybrid intelligent methodology for device model parameter extractions combining multiobjective evolutionary algorithms, numerical optimization methods, and unsupervised learning neural networks on a unified optimization framework. The results between experimentally measured data and the calculation from industrial standard compact models are accurate, stable and convergent rapidly for all I-V curves. Verifications from diodes, bipolar transistors, MOSFETs, FinFETs, to nanowire MOSFETs confirm the robustness of the developed prototype, where the extraction is within 5% of accuracy.**

***Keywords—Automatic model parameter extraction*; *Hybrid intelligent methodology*; *Multiobjective evolutionary algorithms*.**

## I. Introduction

Compact models for various semiconductor devices have been indispensable bridges between foundries and integrated circuit (IC) design companies [1-3]. For a specified compact mode, IC design companies design products according to model cards that characterize the electrical behaviors of transistors fabricated by foundries. The CMOS scaling have reached nanometer sizes following the Moore's law [4]. The conventional planner MOSFETs face physical challenges to further reducing channel length. The multiple-gate MOSFETs, bulk FinFETs and nanowire MOSFETs, are able to suppress short-channel effects enabling further device scaling [5]. Nowadays, commercial available extraction tools BSIMpro+® and MBP® are empirically relying on manual adjustment. The device-engineers-intensive work is very time consuming. We had proposed a single-objective genetic algorithm (GA)-based [6-7] hybrid intelligent methodology for MOSFETs model parameter extraction running on a unified optimization framework (UOF) [8]. However, model parameter extraction considers many sets of I-V and C-V curves simultaneously; thus, it is a multiobjective optimization problem (MOP) in nature. It will be more efficient and useful in semiconductor industry if we can advance the hybrid intelligent methodology combining with a multiobjective evolutionary algorithm (MOEA) [9-12] to improve the extraction efficiency for bulk FinFETs and nanowire MOSFETs.

In this work, we advance the aforementioned hybrid intelligent methodology for automatic model parameter extraction of bulk FinFETs and nanowire MOSFETs. The new approach combines the MOEA with an objective-function-decomposition technique, numerically robust Levenberg-Marquardt (LM) method, and unsupervised learning neural network (NN). We have successfully implemented a prototype of the extraction on UOF.

## II. The Hybrid Intelligent Methodology

Figure 1 shows the newly MOEA-based hybrid intelligent methodology and the implemented prototype. The system has modules: file, solver, calculator, and problem. First, we through file class to read the mask, input, parameter, and output files required by UOF. Second, the imported data from the file class will be sent to the solver class, which controls the problem and calculator classes. Third, the problem class defines various optimization problems and return to the solver class. Final, we use different model calculators to calculate I-V curves of devices. Notably, curves of devices can be calculated via external circuit simulators (e.g. HSPICE® or PSPICE®) or from the built-in analytical equations of compact models.

We apply a nonlinear least square technique to formulate the optimization problem of parameter extractions, as listed in Eq. (1), where a penalty-boundary intersection method is used to decompose the dimension of MOP. Both the MOEA and LM are applied to optimize all parameters. The NN traces the trend of errors of original curves and their first derivatives. To minimize errors between measurement and model, the MOEA will compute the corresponding score of fitness. When the MOEA obtains an updated solution, the LM is activated to search the nearby local optima, and, simultaneously, the NN suggests proper searching directions based on an overall fitness. The prototype automatically extracts improved solutions via the evolutionary process which will terminate when a given root-means-square error reaches for all curves.

## III. Results and Discussion

We implement a prototype of model parameter extraction to verify the automatic extraction for various devices, such as *p-n* diodes, BJTs, MOSFETs, bulk FinFETs, and nanowire MOSFETs, respectively; Fig. 2 shows a system architecture and the logo of the implemented tool. Figure 3(a) shows the extracted (lines) and measured (dots) I-V and transconductance ($g_m$) curves of a *p-n* diode. Figure 3(b) shows the Gummel plot of the extracted Gummel-Poon model of a *npn* BJT. All errors between measured data and extracted current are within 5%. Adopted compact models and final extracted parameters are partially listed in Table 1.

For MOSFETs, we extract model parameters 10 times independently for 130, 85, and 75 nm, respectively, where all devices have the same width of 10 μm, oxide thickness of 3.3 nm, and doping concentration of $3\times10^{18}$ $cm^{-3}$ at 300 K. Figures 4(a)-(d) and (e)-(h) show the extracted $I_D$-$V_{GS}$, $g_m$, $I_D$-$V_{DS}$, and outputconductance ($g_d$) curves of the 130 and 85 nm n-MOSFET, respectively. The results between the model and measured show the accuracy of the extraction and the extracted 10-times curves show its robustness. Figures 5(a)-(d) show the extracted $I_D$-$V_{GS}$, $g_m$, $I_D$-$V_{DS}$, and $g_d$ curves of the 75 nm n-MOSFET, respectively. Figures 6(a)-(b) show 10-time plots of the CPU time verse the number of evolution for 85- and 75-nm n-MOSFET, respectively. It costs about 10 minutes to complete an extraction within 5% error when the BSIM 4.21 model is applied. The average errors of $I_D$-$V_{GS}$, $g_m$, $I_D$-$V_{DS}$, and $g_d$ for various dimensions n-MOSFET are listed in Table 2. Partially extracted parameters for an n-MOSFET with W/L = 10 μm/75 nm are listed in Table 3. The 10-time extracted threshold voltage $V_{th}$ and $g_{m,\ max}$ for various dimensions are listed in Table 4. Above tests clearly confirm the accuracy and robustness of the automatic extraction.

We do further apply the tool to extract bulk FinFETs and n-/p-type nanowire MOSFETs, as shown in Figs. 7 and 8. For the 26-nm drawn gate length bulk n-type bulk FinFET with a

7-nm channel thickness and a 42-nm channel height, at least five objectives are considered simultaneously to extract a set of BSIM-CMG model. Figures 7(a)-(d) show the extracted $I_D$-$V_{GS}$, $g_m$, $I_D$-$V_{DS}$, and $g_d$ curves, respectively. The average errors of five curves and times of bulk n-FinFET are listed in Table 5. The extracted threshold voltage $g_{m,\,max}$, $V_{t,\,lin}$, $V_{t,\,sat}$, *DIBL*, $I_{off}$, $I_{on}$, and *SS* are listed in Tables 6 and 7. Partially extracted parameters are listed in Table 8. Figures 8(a)-(h) show the extracted $I_D$-$V_{GS}$, $g_m$, $I_D$-$V_{DS}$, and $g_d$ curves, respectively, of 10-nm n-/p-type nanowire MOSFETs with a 31-nm channel width. Not shown here, we have also applied the work to extract C-V curves for various devices before model parameter extractions from I-V curves.

## IV. Conclusions

In summary, we have successfully advanced a hybrid intelligent methodology for model parameter extraction. It bases on (i) the multi-objective evolutionary algorithm with a decomposition technique; (ii) the Levenberg–Marquardt method; and (iii) unsupervised learning neural network on the unified optimization framework. Various extractions have been tested which imply its practicality in automatic model parameter extraction. This work can benefit device engineers to perform parameter extraction with engineering acceptable model accuracy for emerging CMOS devices.

## Acknowledgment

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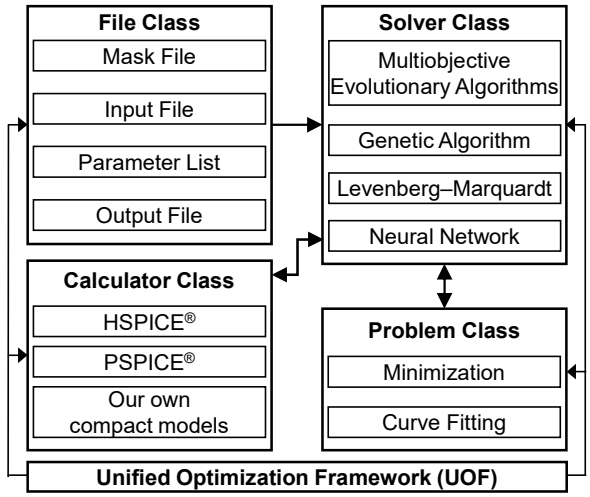


Fig. 1. The unified optimization framework (UOF) of the hybrid intelligent methodology.

$$Minimize \quad \left\{ \frac{1}{N} \sum_{j=1}^{N} \frac{\sqrt{\left(G_{i,j} - M_{i,j}\left(\vec{V}_{i,j}, \vec{P}_{i,j}\right)\right)^2}}{\left|Max\left(G_{i,j}\right)\right|} \right\} \quad for\ each\ i, \qquad (1)$$

where for each set of I-V or C-V curves (i.e., for each *i*), the model of MOP to be solved, where *G*, *M*, *N*, *V*, *P* are measured data, calculated results, number of total points, applied voltage, and model parameters, respectively.

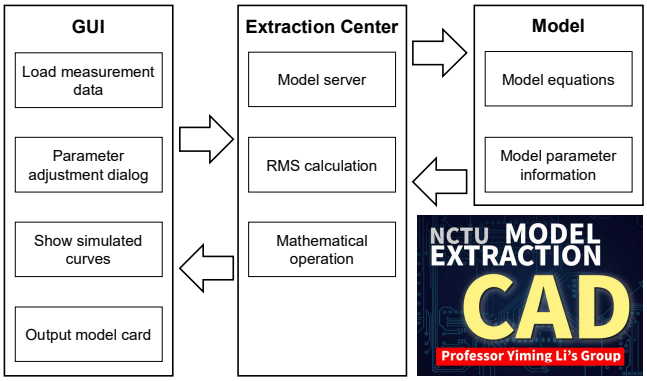


Fig. 2. A system architecture and the logo of the implemented tool.

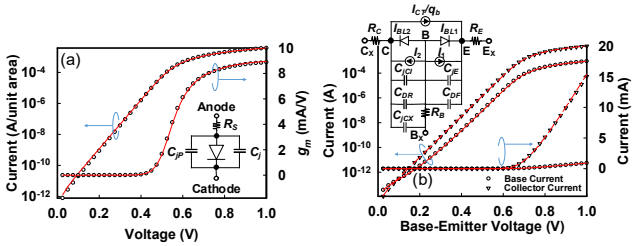


Fig. 3. For a *p-n* diode, (a) the extracted (lines) and measured (dots) of the normalized I-V curves in both the linear and log scales. For an *npn* BJT, (b) the extracted (lines) and measured (dots) Gummel plot. The inset in (a) and (b) are the equivalent circuit model of the *p-n* diode and Gummel-Poon model of *npn* BJT.

Table 1. List of the extracted parameter of the *p-n* diode and *npn* BJT.

| List of the extracted parameter of diode | | |
|---|---|---|
| Parameter Names | Initial Settings | Extracted Results |
| $I_S$ (A/unit area) | $1.0\times10^{-14}$ | $8.196\times10^{-13}$ |
| $N$ | 1.0 | 1.07107 |
| $R_S$ (Ω) | 0.0 | 104.053 |
| List of the extracted parameter of BJT | | |
| $I_S$ (A) | $1.0\times10^{-16}$ | $3.32\times10^{-15}$ |
| $N_F$ | 1.0 | 0.98 |
| $R_E$ (Ω) | 0.0 | 16.53 |
| $R_C$ (Ω) | 0.0 | 32.49 |
| $I_{SE}$ (A) | 0.0 | $1.216\times10^{-14}$ |

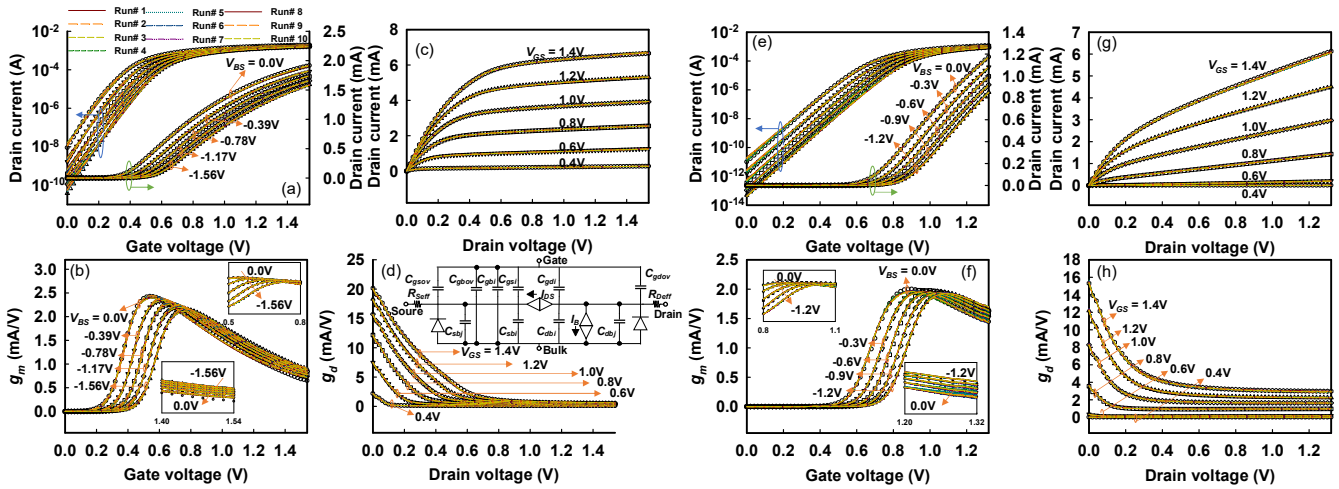


Fig. 4. Width/Length (W/L; μm/nm) = (a)-(d) 10 /130 and (e)-(h) 10/85 n-type MOSFETs; 10-times extracted (lines with colors) and measured (dots) data for (a) and (e) $I_D$-$V_{GS}$, (b) and (f) $g_m$, (c) and (g) $I_D$-$V_{DS}$, and (d) and (h) $g_d$ curves, respectively. The inset in (d) is the equivalent circuit model of the MOSFET.

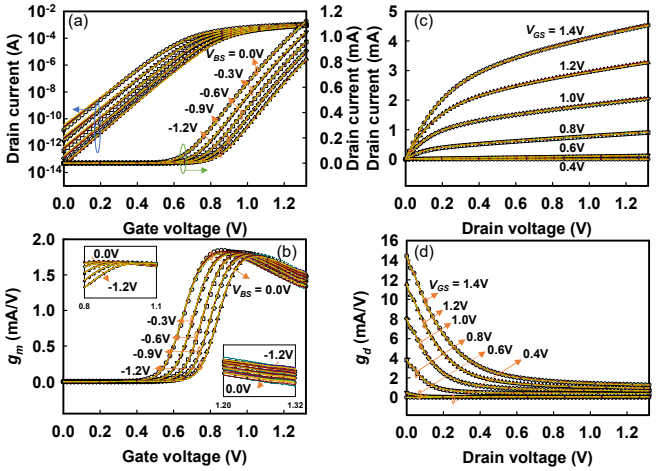


Fig. 5. The extracted (lines) and measured (dots) data for (a) $I_D$-$V_{GS}$, (b) $g_m$, (c) $I_D$-$V_{DS}$, and (d) $g_d$ curves for an n-MOSFET with W/L = 10 μm/75 nm.

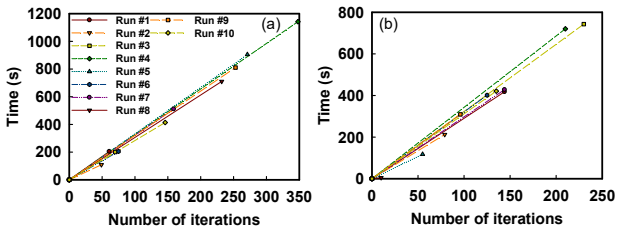


Fig. 6. 10-time plots of the CPU time verse the number of evolutions of n-MOSFETs with (a) L = 85 nm and (b) L = 75 nm, respectively.

Table. 2. List of the average errors among I-V sets of the extracted devices.

| Average Errors (%) | | | |
|---|---|---|---|
| Length | 130 nm | 85 nm | 75 nm |
| log($I_D$)-$V_{GS}$ (%) | 2.876922 | 2.935092 | 3.160965 |
| $I_D$-$V_{GS}$ (%) | 1.487478 | 1.116974 | 1.172822 |
| $g_m$ (%) | 4.969339 | 4.801862 | 4.821634 |
| $I_D$-$V_{DS}$ (%) | 2.638325 | 3.797678 | 3.199965 |
| $g_d$ (%) | 2.200646 | 3.778339 | 1.989134 |

Table 3. Partial list of the extracted parameters for an n-MOSFET with width/length = 10 μm/75 nm at one time.

| Parameter Names | Initial Settings | Extracted Results | Parameter Names | Initial Settings | Extracted Results |
|---|---|---|---|---|---|
| $V_{TH0}$ (V) | 0.7 | 0.359248 | $N_{factor}$ | 1.0 | 1.06441 |
| $K_1$ ($V^{1/2}$) | 0.5 | 0.858372 | $U_0$ ($m^2$/(Vs)) | 0.067 | 0.0216208 |
| $K_2$ | 0.0 | -0.146184 | $U_A$ (m/V) | $1.0\times10^{-9}$ | $-5.07149\times10^{-10}$ |
| $D_{VT0}$ | 2.2 | 2.69279 | $U_B$ ($m^2/V^2$) | $1.0\times10^{-19}$ | $3.1358\times10^{-19}$ |
| $D_{VT1}$ | 0.53 | 1.08794 | $V_{SAT}$ (m/s) | 80000 | 56119.9 |
| $C_{IT}$ ($F/m^2$) | 0.0 | 0.000410095 | $P_{CLM}$ | 1.3 | 0.584354 |
| $V_{OFF}$ (V) | -0.08 | -0.0797791 | $D_{ROUT}$ | 0.56 | 1.46222 |

Table 4. List of the 10-time extracted physical quantities $V_{th}$ and $g_{m,\,max}$ for the devices with three different channel length = 130, 85, and 75 nm, respectively.

| Length | 130 nm | | | | 85 nm | | | | 75 nm | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Measured | $V_t$ (V) | | $g_{m,\,max}$ (mA/V) | | $V_t$ (V) | | $g_{m,\,max}$ (mA/V) | | $V_t$ (V) | | $g_{m,\,max}$ (mA/V) | |
| $V_t$, $g_{m,\,max}$ | 0.243689 | | 2.4265 | | 0.565841 | | 2.00023 | | 0.557628 | | 1.84322 | |
| Run # | $V_t$ | Error (%) | $g_{m,\,max}$ | Error (%) | $V_t$ | Error (%) | $g_{m,\,max}$ | Error (%) | $V_t$ | Error (%) | $g_{m,\,max}$ | Error (%) |
| 1 | 0.2418 | 0.7645 | 2.442 | 0.6429 | 0.5711 | 0.9400 | 1.9672 | 1.7529 | 0.5619 | 0.7726 | 1.8118 | 1.7046 |
| 2 | 0.2417 | 0.7796 | 2.4429 | 0.6758 | 0.5693 | 0.6123 | 1.9612 | 1.9512 | 0.5607 | 0.5555 | 1.8100 | 1.8022 |
| 3 | 0.2406 | 1.2331 | 2.4486 | 0.9107 | 0.5687 | 0.5176 | 1.9609 | 1.9662 | 0.5606 | 0.5329 | 1.8049 | 2.0789 |
| 4 | 0.2548 | 4.5858 | 2.4020 | 1.0063 | 0.5702 | 0.7732 | 1.9634 | 1.8412 | 0.5606 | 0.5472 | 1.8084 | 1.8890 |
| 5 | 0.2485 | 0.8662 | 2.4432 | 0.6882 | 0.5688 | 0.5396 | 1.9695 | 1.5363 | 0.5603 | 0.4841 | 1.8111 | 1.7420 |
| 6 | 0.2466 | 1.2337 | 2.4469 | 0.8407 | 0.5690 | 0.5669 | 1.9764 | 1.1913 | 0.5607 | 0.5583 | 1.8005 | 2.3177 |
| 7 | 0.2543 | 4.3800 | 2.3949 | 1.3022 | 0.5704 | 0.8177 | 1.9665 | 1.6863 | 0.5610 | 0.6186 | 1.8026 | 2.2037 |
| 8 | 0.2562 | 5.1584 | 2.4081 | 0.7582 | 0.5690 | 0.5595 | 1.9681 | 1.6063 | 0.5600 | 0.4336 | 1.8326 | 0.5761 |
| 9 | 0.2414 | 0.9355 | 2.4432 | 0.6882 | 0.5700 | 0.7511 | 1.9597 | 2.0262 | 0.561 | 0.6047 | 1.8065 | 1.9921 |
| 10 | 0.2541 | 4.2764 | 2.3940 | 1.3393 | 0.5681 | 0.4132 | 1.9582 | 2.1012 | 0.5607 | 0.5611 | 1.8034 | 2.1603 |

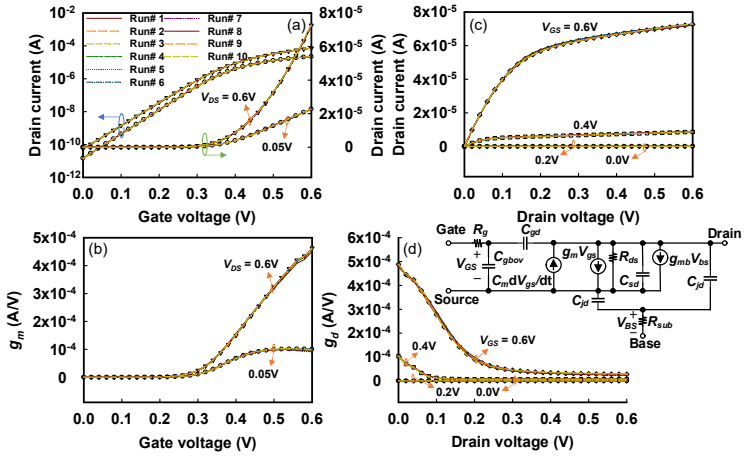


Fig. 7. For the 26 nm n-type bulk-FinFET with a 7-nm channel width and a 42-nm channel height, the extracted (lines) results from the BSIM-CMG model and the measured (dots) data are shown for (a) $I_D$-$V_{GS}$, (b) $g_m$, (c) $I_D$-$V_{DS}$, and (d) $g_d$. The inset in (d) is the equivalent circuit model of the bulk FinFET. Notably, at least 51 parameters are optimized in the BSIM-CMG model with the 108 version.

Table 5. List of average errors and CPU time of the extracted device.

| | | | |
|---|---|---|---|
| log($I_D$)-$V_{GS}$ (%) | 0.1919993 | $I_D$-$V_{DS}$ (%) | 4.767431 |
| $I_D$-$V_{GS}$ (%) | 0.499764 | $g_d$ (%) | 3.57325 |
| $g_m$ (%) | 1.603667 | CPU Time (s) | 582.726 |

Table 6. List of the 10-time extracted physical quantities $g_{m,\,max}$.

| Measured | $g_{m,\,max}$ ($10^{-4}$A/V) | |
|---|---|---|
| | 4.6281 | |
| Run # | $g_{m,\,max}$ | Error (%) |
| 1 | 4.6252 | 0.0626 |
| 2 | 4.6359 | 0.1685 |
| 3 | 4.5879 | 0.8686 |
| 4 | 4.5714 | 1.2251 |
| 5 | 4.6432 | 0.3262 |
| 6 | 4.6066 | 0.4645 |
| 7 | 4.6162 | 0.2571 |
| 8 | 4.5062 | 2.6339 |
| 9 | 4.6458 | 0.3824 |
| 10 | 4.6121 | 0.3457 |

Table 7. List of the 10-time extracted physical quantities $V_{t,\,lin}$, $V_{t,\,sat}$, $DIBL$, $I_{off}$, $I_{on}$, and $SS$, respectively.

| Measured | $V_{t,\,lin}$ (V) | | $V_{t,\,sat}$ (V) | | $DIBL$ | | $I_{off}$ ($10^{-11}$A) | | $I_{on}$ ($10^{-5}$A) | | $SS$ (mV/dec) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0.282628 | | 0.252134 | | 0.0554436 | | 5.4031 | | 7.2658 | | 70.4044 | |
| Run # | $V_{t,\,lin}$ | Error (%) | $V_{t,\,sat}$ | Error (%) | $DIBL$ | Error (%) | $I_{off}$ | Error (%) | $I_{on}$ | Error (%) | $SS$ | Error (%) |
| 1 | 0.2827 | 0.0536 | 0.2546 | 0.9822 | 0.0512 | 7.6243 | 5.4690 | 1.2209 | 7.2838 | 0.2478 | 71.2009 | 1.13127 |
| 2 | 0.2823 | 0.0872 | 0.2538 | 0.6788 | 0.0518 | 6.4241 | 5.5807 | 3.2883 | 7.2865 | 0.2859 | 71.1617 | 1.0756 |
| 3 | 0.2832 | 0.2335 | 0.2472 | 1.9230 | 0.0654 | 18.065 | 5.5085 | 1.9518 | 7.2707 | 0.0686 | 69.2127 | 1.69271 |
| 4 | 0.2829 | 0.1011 | 0.2543 | 0.8615 | 0.0520 | 6.1847 | 5.4632 | 1.1138 | 7.2758 | 0.1376 | 71.1064 | 0.99713 |
| 5 | 0.2817 | 0.3256 | 0.2533 | 0.4775 | 0.0515 | 6.9652 | 5.5788 | 3.2531 | 7.2555 | 0.1412 | 71.0163 | 0.86914 |
| 6 | 0.2819 | 0.2403 | 0.2552 | 1.2385 | 0.0485 | 12.468 | 5.4814 | 1.4502 | 7.2945 | 0.3959 | 71.4011 | 1.41573 |
| 7 | 0.2832 | 0.231 | 0.2545 | 0.9576 | 0.0522 | 5.7781 | 5.5410 | 2.5537 | 7.2798 | 0.1937 | 71.2968 | 1.26752 |
| 8 | 0.2817 | 0.3172 | 0.2533 | 0.4872 | 0.0515 | 6.9685 | 5.4317 | 0.5302 | 7.2102 | 0.7639 | 70.7927 | 0.55155 |
| 9 | 0.2811 | 0.5183 | 0.2539 | 0.7010 | 0.0495 | 10.602 | 5.5430 | 2.5909 | 7.2757 | 0.1365 | 71.1187 | 1.01458 |
| 10 | 0.2833 | 0.2620 | 0.2536 | 0.5953 | 0.0540 | 2.4922 | 5.4956 | 1.7121 | 7.3131 | 0.6518 | 70.9697 | 0.80287 |

Table 8. Partial list of the extracted parameters for the 26-nm n-type bulk FinFET.

| Parameter Names | Initial Settings | Extracted Results | Parameter Names | Initial Settings | Extracted Results |
|---|---|---|---|---|---|
| $C_{IT}$ (F/m$^2$) | 0.0 | $5.146\times10^{-7}$ | $V_{SAT}$ (m/s) | 85000 | 99998.7 |
| $C_{DSC}$ (F/m$^2$) | 0.007 | 0.0219993 | $U_0$ (m$^2$/Vs) | 0.03 | 0.0650832 |
| $C_{DSCD}$ (F/m$^2$) | 0.007 | 0.0142987 | $U_{CS}$ | 1.0 | $8.403\times10^{-5}$ |
| $D_{VT0}$ | 0.0 | 0.99285 | $P_{DIBL1}$ | 1.30 | 0.199277 |
| $D_{VT1}$ | 0.6 | 0.376897 | $D_{ROUT}$ | 1.06 | 0.271762 |
| $K_1$ (V$^{1/2}$) | 0.0 | $3.249\times10^{-7}$ | $P_{VAG}$ | 1.0 | 0.599929 |
| $E_{TA0}$ | 0.6 | $4.917\times10^{-6}$ | $P_{CLM}$ | 0.013 | $1.211\times10^{-6}$ |
| $D_{SUB}$ | 1.06 | 0.977978 | $P_{CLMG}$ | 0.0 | 0.522503 |

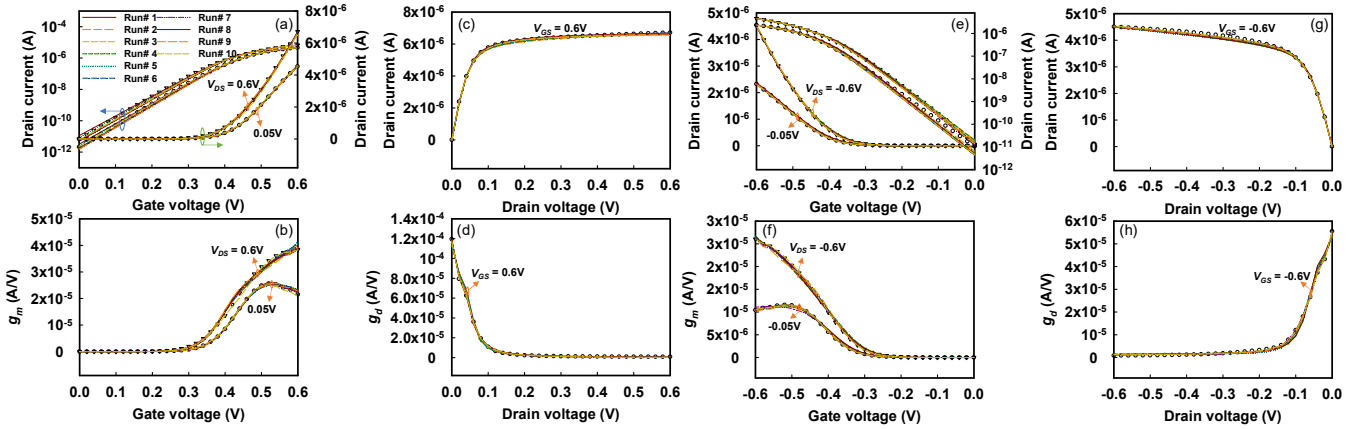


Fig. 8. For 10 nm (a)-(d) n- and (e)-(h) p-type nanowire MOSFETs with a 31-nm channel width, the extracted (lines) and measured (dots) data are shown for (a) and (e) $I_D$-$V_{GS}$, (b) and (f) $g_m$, (c) and (g) $I_D$-$V_{DS}$, and (d) and (h) $g_d$ curves, respectively. Similar to the bulk FinFET, the BSIM-CMG model with the 108 version has been adopted for parameters are optimized among the five objectives, where errors are within 5% for all sets of I-V curves.