Novel Optimization Method using Machine-learning for Device and Process Competitiveness of BCD Process

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***Abstract*— The novel optimization method for BCD(Bipolar-CMOS-DMOS) process development based on Machine Learning(ML) and statistical process modeling considering the entire wafer variation is proposed to improve the device and process competitiveness. The self-align PBODY process is used for high-performance N-type Lateral Diffused Metal Oxide Semiconductor(NLDMOS) in BCD process and it also is related to stability in PMIC operation. The process modeling embracing the performance and the stability of LDMOS is performed with TCAD using inline data. For the development of BCD process, the PBODY process parameters are optimized through the ML algorithms and the condition is verified with TCAD and silicon test. Finally, we can secure new low voltage NLDMOS with the improved performance and stability respectively for without any degradation in the new 0.13µm BCD process.**

Keywords—BCD process, optimization, machine-learning, LDMOS, statistical modelling

I. INTRODUCTION

Recently, the PMIC becomes more important as the market of portable electronic products growing up and expanding. PMIC performs a role of supplying stable power to a number of blocks and converting an input voltage to fit each block. The BCD process providing various LDMOS for 8V to 40V applications is well-known for a suitable process for PMIC [1,2]. However, the BCD process has some underlying difficulties owing to the limited number of layers relating to the cost of production [3]. Diverse types of LDMOS and hundreds of devices are manufactured simultaneously with the same IIP layer and different pattern sizes in BCD process, which is a root cause of increased process instability. Therefore, the simulation of not only the performance of the device but also the variation of the process is requested to develop the BCD process.

In this paper, the novel simulation flow using machine-learning and statistical process modelling that suggested in Fig.1 is proposed to improving both performance and process stability of new low voltage NLDMOS with 0.13µm BCD process, which is a suitable of a device for mobile application using 3.3 ~5V battery in Fig. 2 [4].

II. METHOD

A. Statistical process modeling

LDMOS is made with the Self-align BODY IIP process that creates the stable short channel regions and forms the gate poly pattern simultaneously shown in Fig. 3(a) [5]. In order to decrease the substrate resistance (Rsub) for the reliability of LDMOS, higher energy and more dosage are used in self-align BODY accompanied with the thicker photoresist (PR) [6,7]. However, the excessive PR etching is inevitable to form the precise pattern with thick PR and it causes the PR slope variation across the entire wafer. Therefore, the shapes of PR patterns are bound to be different depending on the location for the reason that a variety type of LDMOS are formed at the same process step. Particularly, the difference between inner and outer PR shapes of PBODY process is the outstanding issue of LDMOS, mainly used as a form of multi-finger structure. Figure 3(b) shows the Vtgm/Idsat distribution by such variation, especially between inner-outer transistors due to PR pattern density [8].

The relation between the different PR slopes and the Vtgm/Idsat distribution is verified with TCAD simulation. The channel doping profile determining Vtgm of LDMOS varies with PR slope, due to the difference of boron concentration penetrated through PR shown in Fig. 4 and 5.

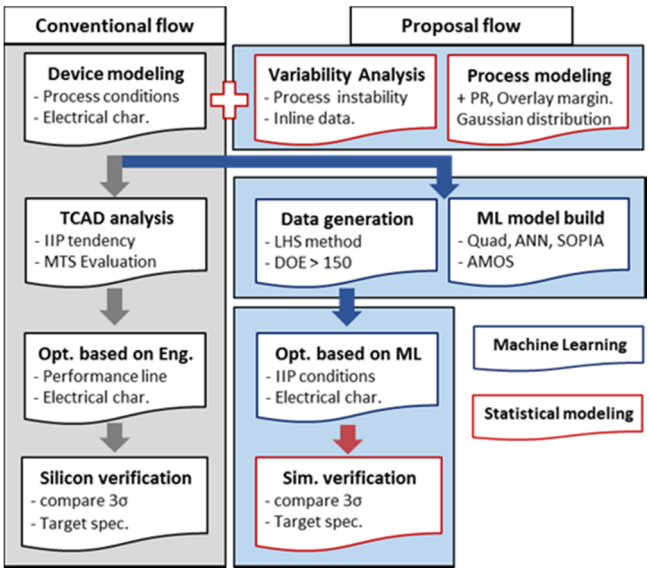

Fig. 1. New simulation methodology using machine learning and statistical process modeling

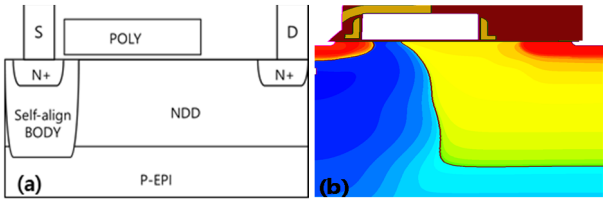

Fig. 2. NLDMOS: cross-section (a) and simulation structure (b).

For co-optimization of process variation and performance, the statistical process modeling for the variation of PR slope is implemented based on inline Scanning Electron Microscope (SEM) image and Critical Dimension(CD) data. The angles of PR slope are calculated from the difference between the Top CD and the bottom CD of PR. The mean value and the standard deviation of PR slope are obtained built on the inline data, as shown in Fig. 6. The PR slope distribution is assumed that comes from Gaussian distribution. Then, Vtgm/Idsat distribution of LDMOS is calibrated with the PR distribution on TCAD. The other variation factors like the overlay and the open area of IIP mask are ignored because the self-align scheme has the advantage that makes such variations smaller.

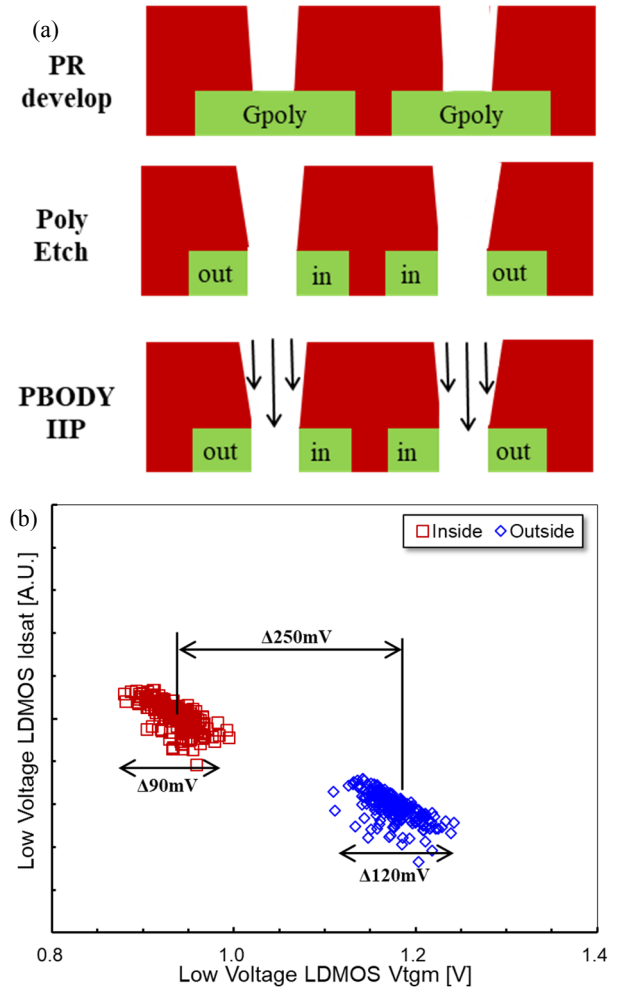

Fig. 3. PR variation of self-align BODY after etch in inner-outer pattern (a) and Vtgm/Idsat distribution including layout effect of LDMOS (b).

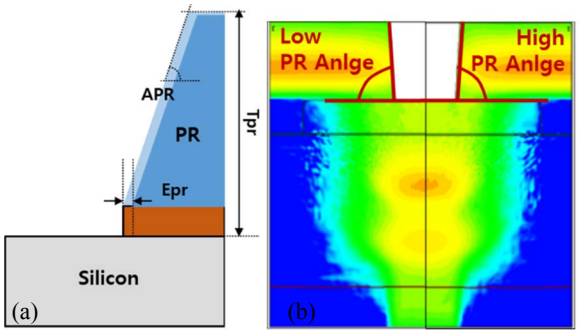

Fig. 4. Self-align BODY PR half-structure (a) and TCAD modeling IIP profile including PR variation (b).

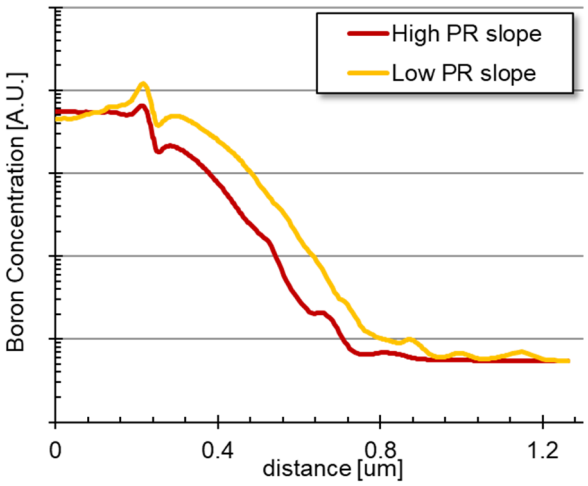

Fig. 5. Lateral Boron Concentration after anneal from TCAD simulation form the channel of the low voltage LDMOS

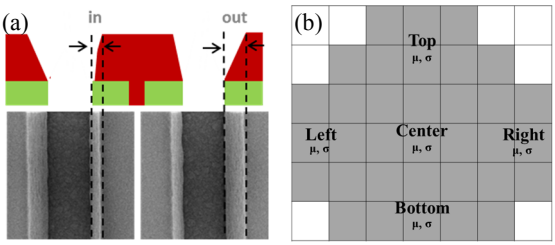

Fig. 6. Top view of self-align BODY PR after implant (a) and entire wafer CD data map example after PR developing (b)

B. *Machine learning*

In optimization for the electrical characteristics and robustness of the process, Automatic Multi-objective Optimization solution(AMOS) is used with PBODY IIP parameters for the new NLDMOS, because PBODY IIP dosage not affect other devices' characteristics. AMOS is an in-house tool that performs automatically data generations, data model learning, and optimization at once, based on ML.

Firstly, 150 conditions that consist of IIP parameters were selected for Latin Hypercube Sampling (LHS) method [9]. And, 5 electrical parameters of both types of low and high voltage LDMOS related to performance and reliability are trained through AMOS with TCAD data shown in Fig. 7. Then, several regression models like quadratic, Artificial neural network (ANN), Samsung open platform for Intelligence Application auto regression model (SOPIA) were evaluated. Finally, SOPIA model which totally records the high test R^2 was chosen among those for development for new NLDMOS [10]. As shown in Fig. 8, the regression result is attained R^2 more than 0.98 and has a good match with the TCAD data.

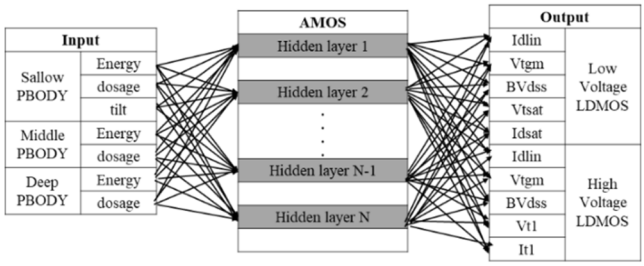

Fig. 7. AMOS regression diagram between PBODY IIP parameters and electric parmaters of two types of LDMOS.

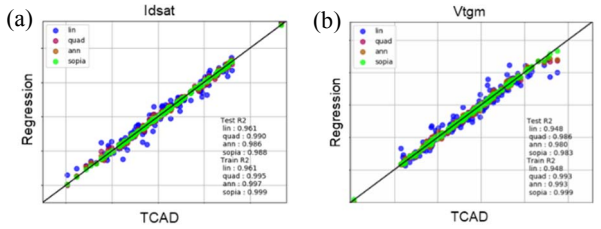

Fig. 8. AMOS regression consistency: Idsat (a) and Vtgm (b) of LDMOS

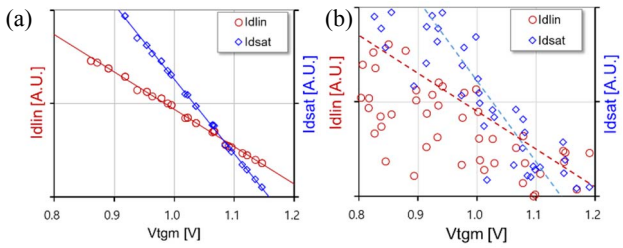

Fig. 9. The simulated data extracted from conventional DOE (a) and the simulated data obtained through LHS method (b).

III. Simulation

The new simulated data obtained through our method shows the improved conditions compare to the current performance line while the new simulated data obtained through our method shows the simulated data extracted from conventional DOE is placed on the same performance line with the current silicon data shown in Fig 9. It means there is a key to develop the device under conditions that changed the existing our perspective. The condition optimized with ML indicated that lower energy of deep PBODY is enough to satisfy reliability spec. Also, Shallow PBODY dosage increases to compensate for lowered deep PBODY IIP in the view of PBODY Vtgm. Through the machine learning model, the shallower and stronger IIP conditions are selected in terms of reliability and performance.

And the ΔVtgm distribution was evaluated simultaneously with the performance of the condition using the statistical process modeling. ΔVtgm is compared correspondingly with standard deviations of Vtgm distribution derived from PR slope variation. It is founded that ΔVtgm of low voltage LDMOS is more affected by weakening deep PBODY IIP than increasing shallow PBODY IIP dosage. Because NDD IIP dosage is much lower than PBODY IIP, a small portion of deep PBODY IIP penetrated PR change the length of the channel, causing a variation in Vtgm.

Finally, the proposal condition shows the performance is improved 5% and ΔVtgm decreases 30% compared to current NLDMOS shown in Fig. 10 and 11. Using the new simulation method, the optimized condition that enhances the stability and the performance is obtained at once, whereas the conventional method might need a few steps of iteration to optimize both of them.

IV. Experimnet Result

Figure 12 and Figure 13 show the silicon data for two test conditions of new low voltage NLDMOS, slightly changed from the proposal condition in the light of productivity. These results also show a similar trend with the simulated one, although there is a little difference.

The difference between inner and outer transistor's Vtgm is reduced a level lower than 1/5 to existing silicon data in both of two cases as shown in Fig. 12. In the view of performance,

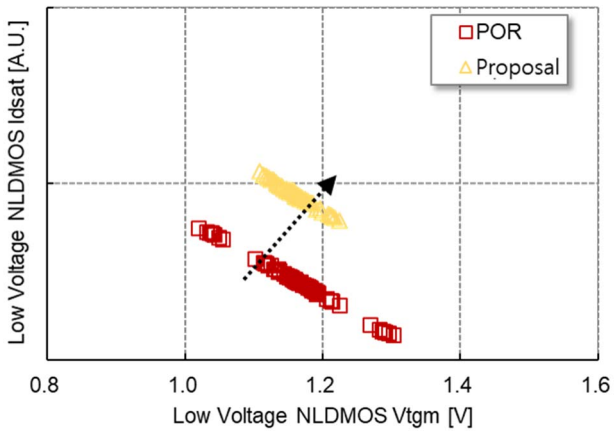

Fig. 10. ML optimization results of NLDMOS performance .

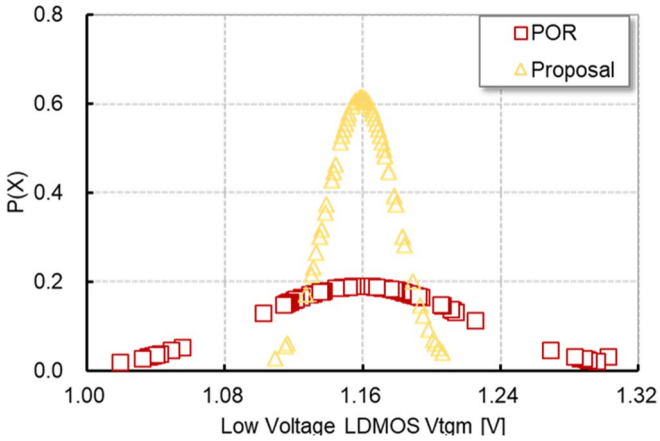

Fig. 11. ML optimization results of NLDMOS Vtgm distribution.

Idsat of case #2 is higher than POR and case #1 at the same Vtgm as shown in Fig. 13. Because the low voltage LDMOS operates at high gate bias, Idsat characteristic is also important not only Ron.sp, representing the operation at a low gate bias.

From this work, the new low voltage NLDMOS has improved the performance of 5% and process stability (ΔVtgm) from 270mV to 44mV.

V. Conclusion

The new optimization method that can be satisfied with the device performance and the process stability is proposed. The PBODY process, which is the key process in manufacturing LDMOS, cause dispersion of device electrical characteristic, and it is statically modeled with TCAD simulation.

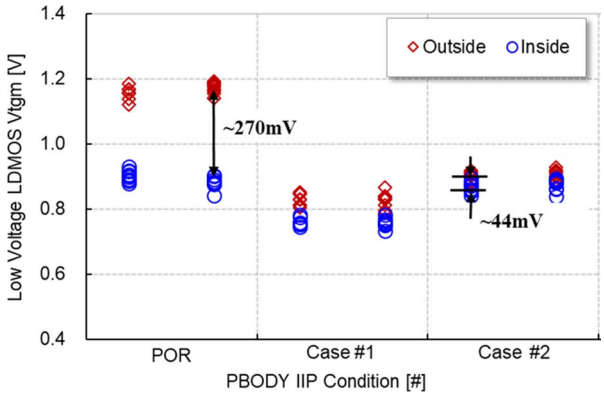

Fig. 12. Vtgm distribution of ML optimized LDMOS IIP condition

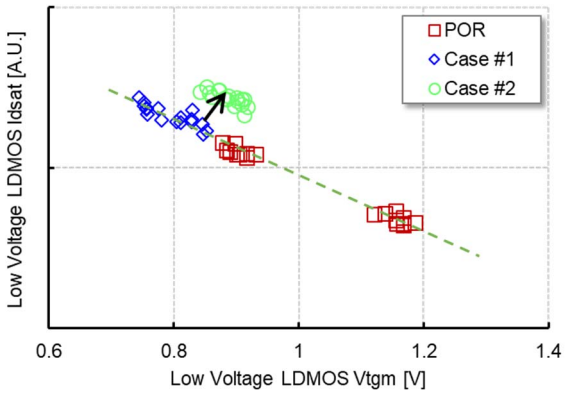

Fig. 13. Vtgm and Idsat graph of ML optimized LDMOS IIP condition related to performanc.

Especially, the relation between PR slope variation and Vtgm distribution is verified using the entire wafer's in-line data and TCAD analysis. For development of LDMOS in BCD process, PBODY IIP parameters are trained and optimized with AMOS, which is an in-house tool for ML. Also, the condition selected by Machine-learning is tested in BCD process and shows a good match with simulation data.

Machine-leaning and statistical process modeling are applied to the new method and the effectiveness of the method is verified through TCAD and silicon analysis. Finally, we obtain the improved result for performance and ΔVtgm of new LDMOS and enhanced the competitiveness of the BCD process.

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