Via Size Optimization for Optimum Circuit Performance at 3 nm node

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***Abstract*— Via size and placement for layer-to-layer connection needs careful assessment. Small via size offers compact pitch and denser connections between metal layers, while larger via size offers reduced resistance for better performance. In this paper, an optimization scheme for via size is presented, without changing the density of via allocation. We show that increasing via CD reduces resistance, resulting in enhanced performance. However, this also results in increased capacitance between different circuit nodes, which causes degradation in performance. These two opposite effects result in an optimum via CD, which offers best performance. We also show that this optimum via CD depends on the resistivity of the via material and the dielectric constant of inter-layer dielectric (ILD) surrounding the via. Via design guidelines for TiN/Co via material and for a futuristic barrier-less metal with equivalent resistivity 1/10th of cobalt via, is presented for different dielectric constants of surrounding dielectrics.**

Keywords—Via optimization, DTCO, Ring Oscillator, Circuit Modeling, FinFET, Nano-sheet FET, RC delay, Process Optimization.

I. INTRODUCTION

Vias are used for connecting two metal lines at different level. The size of the via is usually designed keeping in consideration either higher packing density at advanced nodes leading to smaller size, or higher current density for a smaller voltage drop to support power grids, resulting in a larger size [1]. The metal used for the via or the dielectric surrounding the via, are usually not considered while designing a layout. An increment in the size of the via leads to reduced via resistance, which favors improved performance.

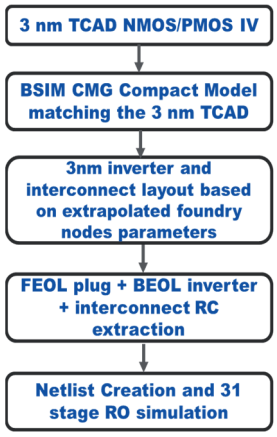

Fig. 1. Flow chart for 31-stage ring-oscillator (RO) performance evaluation, already presented in [2] [3].

If the size of the via is increased keeping the pitch constant, an increment in size of the via results in reduced gap between two adjacent via. Thus, the capacitance between two via increases with increment of via CD, which results in reduced performance. Therefore, an optimum size of the via exists which results in best performance, and would depend on the resistivity of the via metal and dielectric surrounding the via. In this paper, using detailed front-end of line (FEOL), back-end of line (BEOL) and circuit simulations, we show such optimum size of the via resulting in optimum ring-oscillator (RO) performance, as a function of via metal and dielectric parameters.

II. DESCRIPTION OF APPROACH

The ring-oscillator (RO) circuit simulation framework (Fig. 1) is used to see the impact of via CD modulation on RO stage delay. Firstly, FinFET based FEOL TCAD deck is established at 3 nm node for both NMOS and PMOS transistors. Next, the BSIM-CMG compact model is calibrated to the TCAD generated IV/CV characteristics. The 3nm inverter layout for middle-of-line (MOL) & BEOL layers is drawn next (Fig. 2 (a)), using which the BEOL 3D structure is generated (Fig. 2 (b)). The parasitic resistance and capacitance of MOL & BEOL is extracted from this 3D structure. Using the FEOL compact model and MOL/BEOL parasitic for inverter and interconnect, the 31-stage RO simulations are performed. This flow is discussed in detail in [2] and [3]. The parameters used in this study are shown in Fig. 3. Via-0 (Fig. 2(b)) is used for CD optimization.

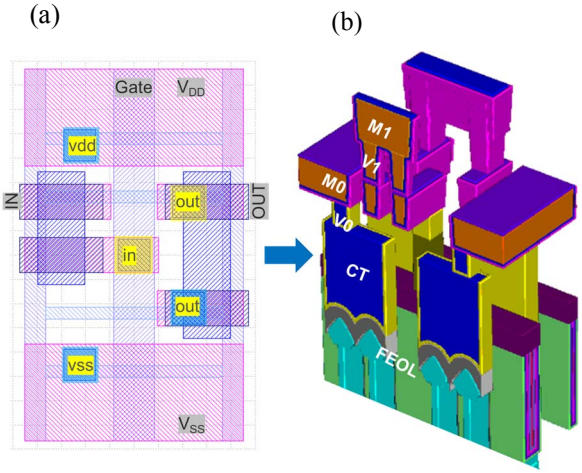

Fig. 2. (a) Inverter Layout at 3 nm node. Via-0 connections are highlighted (b) Schematic of the BEOL inverter structure of an inverter, used for RC extraction.

Parameter	Value (nm)
Gate Pitch	45
Fin Pitch	24
W_{FIN}	5
H_{FIN}	60
Spacer W	5
L_G	14
Contact CD	13
CT/CG CD	13
Via 0 CD	13

Fig. 3. List of FEOL and BEOL parameters used in the study.

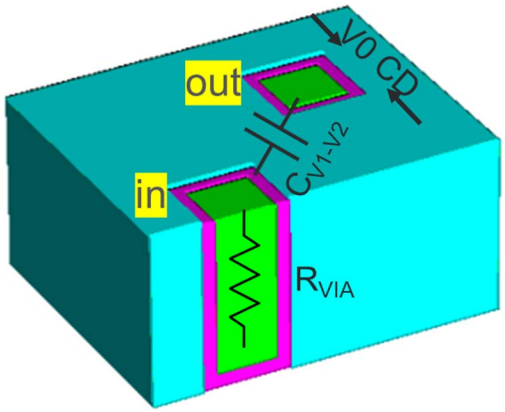

Fig. 4. Via-0 at in and out node from (b). The resistance of the via and capacitance between them is highlighted. Goal of this paper is to optimize Via-0 CD for best circuit performance.

III. Results And Discussions

To study the impact of via CD modulation, the via connected to IN and OUT port of the inverter are considered (Fig. 2 (b) and Fig. 4). Fig. 4 shows the resistance of a via, and the capacitance between two via, which in turn decides the capacitance between IN and OUT port of an inverter.

Fig. 5 (a) shows the normalized resistance of via vs. via CD, for two via metals: Co and a futuristic barrier-less metal with equivalent resistivity 1/10th of cobalt via. The normalization is done with respect to Co via resistance at 13 nm CD. Co based via has a TiN liner of 2 nm thickness. Fig. 5 (b) shows the relative capacitance between the two via vs. via CD, for different dielectric constant of ILD surrounding the via. For a via CD increment of 8 nm, resistance reduces ~70 % while the capacitance increases by 2× (Fig. 5(a) & (b)).

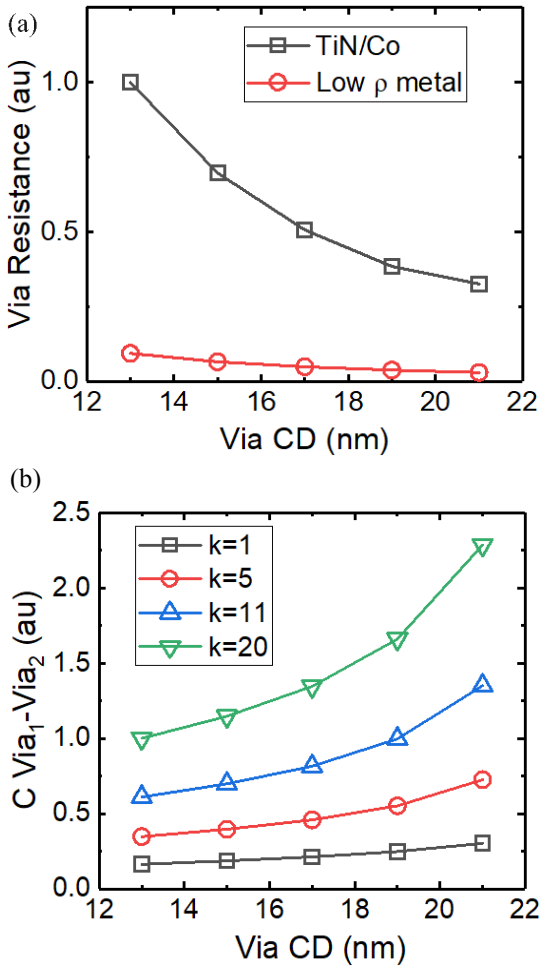

Fig. 5. (a) Via-0 resistance vs. Via CD for different Via-0 material systems. Via resistance improves as per the expectation. (b) Capacitance between two vias vs. Via-0 CD, for different ILD dielectric constants. Coupling capacitance increases as a function of Via CD.

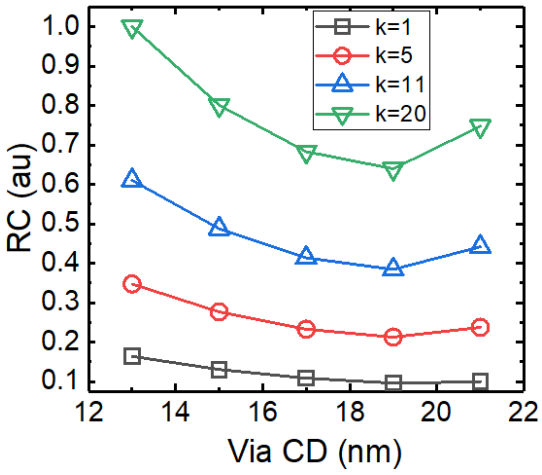

Fig. 6. RC time constant as a function of Via CD for TiN/Co via material, for different ILD k. At lower k, increasing Via-0 CD only helps in reducing time constant. At higher k values (>= 5), an optimum via CD exists for minimum RC time constant.

The collective effect of resistance reduction and capacitance increment with via CD is shown in Fig. 6, where in the RC time constant (multiplication of via R and C) is shown for TiN/Co, for various ILD dielectric constant. It is observed that for ILD k=1 (for air spacers [3]), the via CD increment only results in RC time constant reduction, as the capacitance does not increase as significantly with increment in via CD. However, for ILD k = 5 and above, the RC vs. via CD is a U-shape curve, depicting an optimum via CD point with lowest RC.

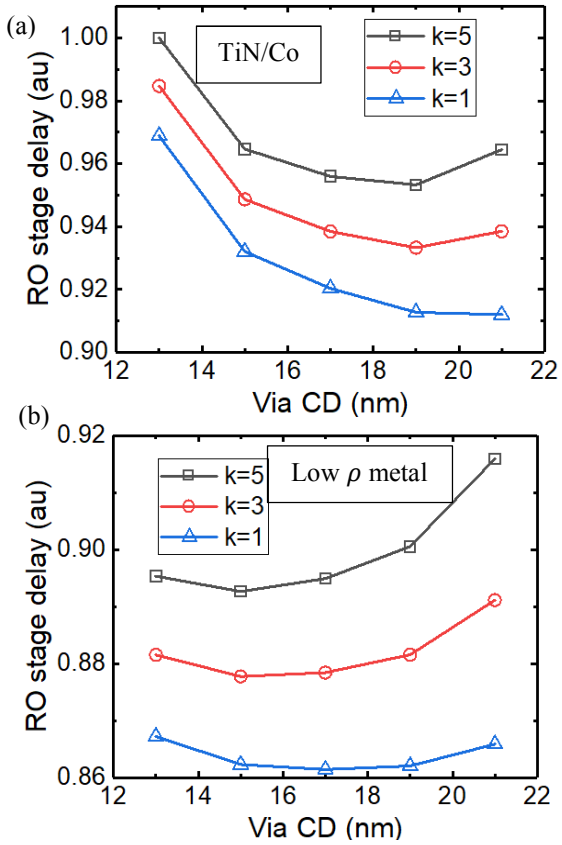

Fig. 7. (a) RO stage delay vs. Via CD for TiN/Co Via-0 material, for ILD k of 1,3 and 5. We observe that RO delay first decreases with reduction in Via-0 CD and then increases. Reduction is attributed to reduction in via resistance and increment is attributed to increased capacitive coupling. Thus, an optimum performance point exists. At low k (k=1), the optimum point is not seen because capacitance is very low. (b) same as (a) but for lower ρ Via-0 material. For lower ρ, the resistance is very low to begin with. Thus, increasing CD does not give much performance benefit as capacitance degradation starts to degrade the performance earlier

The entire circuit RO delay with such via CD change is shown in Fig. 7 (a) for TiN/Co and (b) for low resistivity metal (ρ). The plots are normalized with respect to TiN/Co metal at nominal via CD of 13 nm. Analogous to individual layer RC time constant, RO delay also suggests that for ILD k=1, the via CD increment will only help in improving performance. However, for both k = 3 and 5, a via CD of 19 nm shows best performance with a RO stage delay reduction of ~ 5 %. For the lower ρ metal, increasing via CD does not yield much performance boost as resistance of via is already low to begin with. At ILD k = 1, there is an optimum point at CD = 17 nm. However, for k=3 and 5, an optimum point exists at lower via CD.

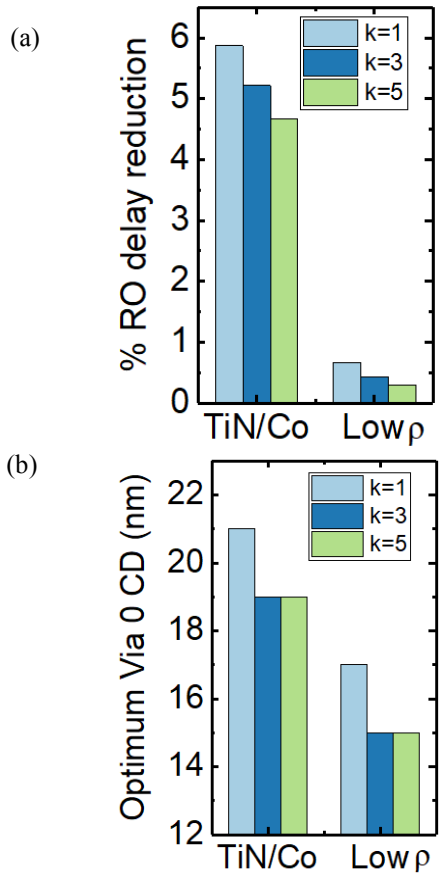

Fig. 8. (a) Maximum reduction in RO delay for TiN/Co and lower ρ Via-0 material system, at ILD k = 1, 3 and 5. For Co, ~ 5% reduction is observed, however for lower ρ material, benefit is less than 1 %. (b) Via-0 CD for optimum performance at ILD k = 1, 3 and 5, for Co and lower ρ metal. For Co material system, a larger Via-0 CD of 19-21 nm would be beneficial, but for a low resistance material system, a smaller Via-0 CD of 15-17 nm would be optimum.

Fig. 8 (a) summarizes the performance boost which can be obtained for both TiN/Co and low ρ via material. Using proper via CD, TiN/Co can enable performance boost about 5 %. The optimum via CD is shown in Fig. 8 (b), for both metals, and for different ILD k's. For air-spacer, larger via CD can give better performance, however for ILD k=3 and 5, a smaller via CD can give an optimum performance point. One way to achieve larger via CD is application of suitable mask bias. For example, a 3 nm mask bias would result in 19 nm via CD at a nominal via CD of 13 nm.

IV. Conclusion

We propose via material system (via material resistivity & surrounding ILD's dielectric constant) based via CD design at 3 nm node to enable up to 5 % performance gain. Such a method can also be used in congruence with via CD design for other BEOL layers to enable even larger performance gains.

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