Complementary FET Device and Circuit Level Evaluation Using Fin-Based and Sheet-Based Configurations Targeting 3nm Node and Beyond

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Abstract— **Complementary FET (CFET), implemented by stacking NMOS and PMOS on top of each other, is considered as an emerging option to continue logic scaling beyond 3nm node. It can be configured with a fin-on-fin (fin-based CFET) or sheet-on-sheet (sheet-based CFET) structures. In this paper, we use 3D-TCAD simulation to compare those two configurations at both device and circuit levels. For accurate comparison between these two CFET configurations, we deploy a drift-diffusion simulation framework, calibrated to semi-classical sub-band BTE (Boltzmann Transport Equation). We show that for the same effective channel width, nMOS of sheet-based CFET has 10% higher drive-current compared to fin-based CFET. For pMOS, sheet-based CFET shows 5% lower drive-current compared to fin-based CFET. When compared for the same device footprint with increased nanosheet width, nMOS and pMOS sheet-based CFET shows 73% and 47% higher drive current respectively compared to fin-based CFET. Using 31-stage ring-oscillator as a representative circuit, we show that for the same electrical channel width, the circuit performance of the sheet-based CFET is 2.6% higher than the fin-based CFET at Vdd of 0.7V. When compared for the same device footprint, sheet-based CFET shows 9% higher circuit performance compared to the fin-based CFET.**

Keywords— Complementary FET, FinFET, Nano-sheet FET, DTCO, Ring Oscillator, Circuit Modeling

I. Introduction

In current CMOS technology, feature size scaling of FEOL and BEOL are reaching their limit due to weaker electrostatic controllability and increased portion of parasitic. Complementary FET (CFET) is an attractive option to continue logic area scaling. First, CFET stacks nMOS and pMOS vertically, thus the layout area previously utilized for nMOS devices becomes available. Second, this vertical stacking of nMOS and pMOS offers simplified access of the transistor terminals [1], such as by shorting n/p drain contacts internally. This allows the design of the standard cell library with lower number of M0 tracks, further reducing the standard cells height and area. Overall, it has been shown that using CFET, 25% area scaling can be achieved for both logic and SRAM [2]. Currently FinFET as well as Nanosheet are considered as main candidates for advanced CMOS technology. Similarly, CFET can also be realized using a fin-based configuration (FBC) or a sheet-based configuration (SBC). In this paper, we perform both device and circuit level evaluation for those two configurations at 3nm node dimensions.

II. Description Of Approach

First, we performed 3D-TCAD process simulations using a CFET process flow (Fig. 1) and 3nm CFET dimensions (Fig. 2). CFET inverter layout (Fig. 3) assumes two fins for FBC and one N/P stack for SBC shown in Fig. 4. The N/P stack in SBC is assumed to consist of two nanosheets for each nMOS and pMOS to achieve the same electrical channel width as in FBC. In both CFET structures, nMOS is stacked on top of pMOS (with 30nm separation) so that pMOS can benefit from substrate induced stress for mobility improvement. The nMOS device is assumed un-stressed while a 500MPa compressive stress is assumed for pMOS.

CFET Process Flow

- ❑ Si/SiGe Fin Formation
- ❑ Dummy Gate
- ❑ Spacer
- ❑ Cavity Etch
- ❑ Inner Spacer
- ❑ Bottom Epi & Contact
- ❑ NP Isolation
- ❑ Top Epi
- ❑ ILD
- ❑ RMG
- ❑ Top Contact

Fig. 1. CFET process flow

Parameter	Value
Gate Pitch	45 nm
Gate Length	15 nm
N/P Space	30nm
Fin Pitch	26nm
Fin Height	18nm
Fin Width	5nm
Nanosheet Pitch	39nm
Nanosheet Width	18nm
Sheet Thickness	5nm

Fig. 2. 3nm CFET parameters used in 3D-TCAD simulations

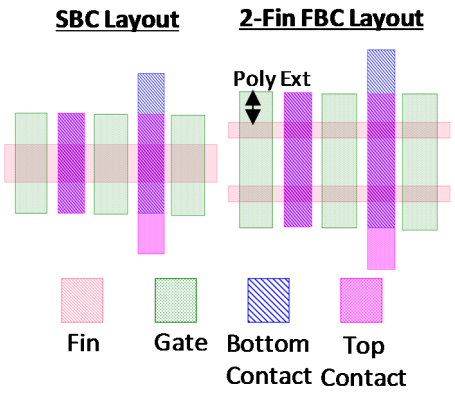


Fig. 3. Layout for SBC and 2-Fin FBC

For proper comparison, both FBC and SBC are assumed to have the same size of silicon channels, with a cross-section of 18nm by 5nm. Both devices are assumed to have the same poly extension, set to half of the fin-to-fin spacing (Fig. 3).

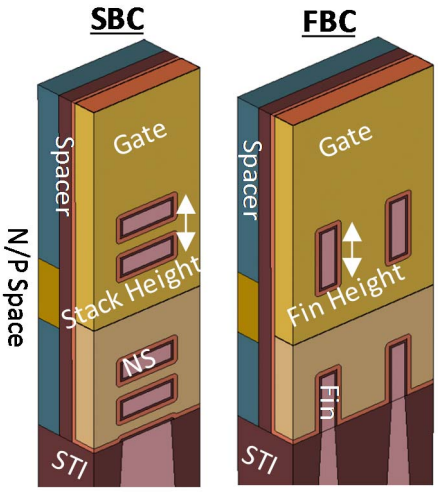


Fig. 4. Nanosheet-based CFET and Fin-based CFET, showing only half gate pitch from the middle of channel to middle of the Drain. 18nm of fin height by 5nm of fin width, Fin height are used for nMOS and pMOS in FBC which is equal to Si/SiGe/Si stack height in SBC.

Under these assumptions, SBC offers a 25% footprint reduction of the active area. Additionally, for both nMOS and pMOS, SBC and FBC are assumed to have the same doping profile and gate work function. This leads to very similar electrostatics (subthreshold slope and DIBL) for FBC and SBC. To accurately model the nature of electron and hole transport at these ultra-short 3nm node dimensions, first we solved the semi-classical sub-band Boltzmann transport equations (BTE), self-consistently with the Poisson and Schrodinger equations for both FinFET and nanosheet structures (Fig.5). The current-voltage characteristics are then used for calibration of the simplified drift-diffusion modeling framework. The density gradient, low field mobility and high-field saturation model parameters in the drift-diffusion framework are tuned for this calibration.

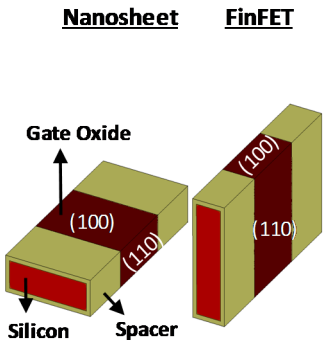
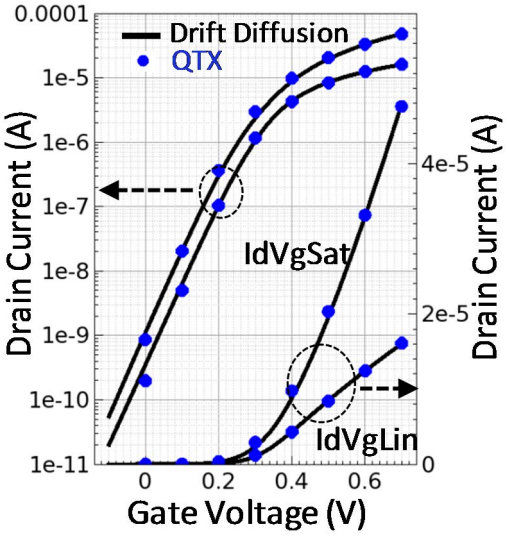


Fig. 5. Simplified Nanosheet and FinFET structures used for Sub-band BTE (Boltzmann Transport Equation) simulation.

(a)



(b)

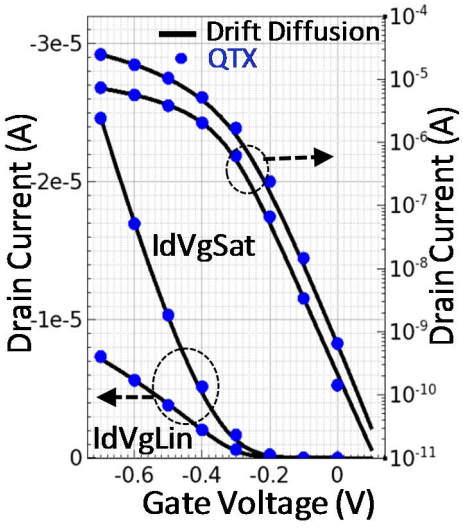


Fig. 6. Calibration of Drift-diffusion models to Sub-band BTE simulations: IDVG characteristics of (a) nMOS, (b) pMOS

A good matching is achieved in the current-voltage characteristics for both nMOS (Fig. 6a) and pMOS (Fig. 6b) in both linear and saturation conditions. Simultaneously, similar carrier density profile (Fig. 7) is also achieved between the semi-classical sub-band BTE and simplified drift-diffusion framework.

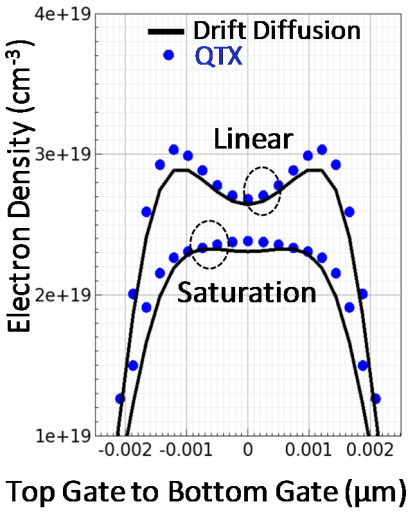


Fig. 7. Calibration of electron density distribution for Drift-diffusion models to Sub-band BTE simulation

Using this calibrated drift-diffusion framework, the performances of FBC and SBC devices are further analyzed. To evaluate FBC and SBC at circuit level, we perform 31-stage ring-oscillator (RO) simulation considering only the FEOL part, using the simulation framework described in [4].

III. Results And Discussions

Fig. 8 shows the electron mobility distribution along gate pitch direction in nMOS for SBC and FBC. Mobility profile along fin pitch direction in the middle of channel is shown for nMOS (Fig. 9a) and pMOS (Fig. 9b).

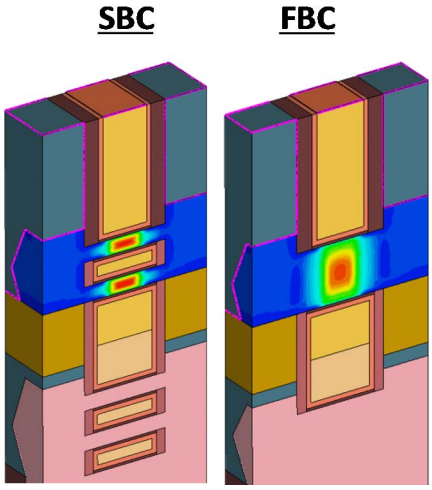


Fig. 8. 3D eMobility distribution in nMOS.

SBC channel is dominated by (100) surface while FBC channel is dominated by (110) surface. For silicon, (100) surface provides higher electron mobility than (110) surface. Hence, higher electron mobility is seen in SBC nMOS. On the other hand, hole mobility for (100) surface is lower than the one of (110) surface, thus SBC pMOS shows lower hole mobility.

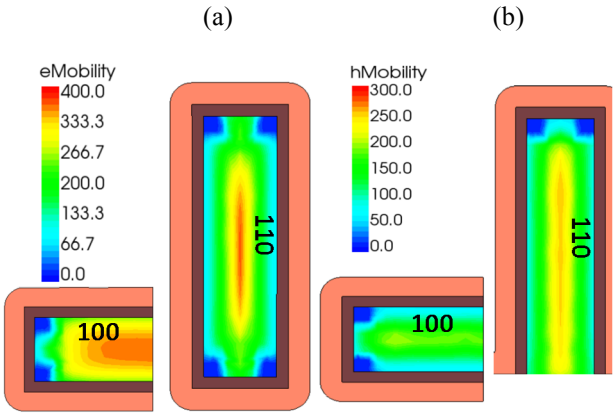


Fig. 9. Mobility distribution for Sheet and Fin in the middle of channel for (a) nMOS and (b) pMOS. Electron mobility is higher for (100) surface orientation compared to (110); hole mobility is lower for (100) surface orientation compared to (110).

Fig. 10 shows Ron and Cinv comparison for FBC and SBC. With the same channel volume, SBC nMOS shows 16% lower Ron (normalized series resistance) compared to FBC while pMOS shows 10% higher Ron. Due to 25% smaller footprint for SBC, parallel capacitance from gate to drain is lower, leading to 9% lower Cinv (inversion gate capacitance) compared to FBC.

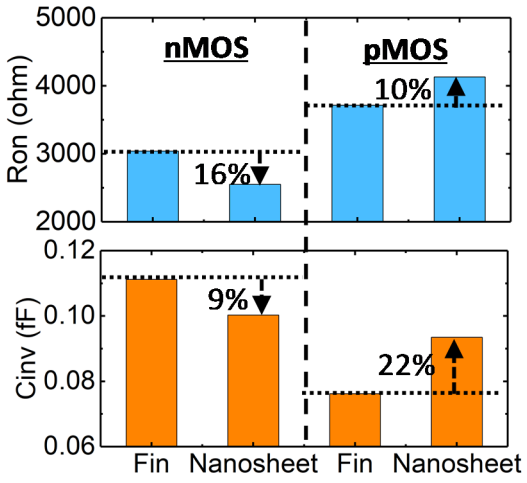


Fig. 10. Ron and Cinv comparison for FBC and SBC.

On the other hand, pMOS in SBC structure shows 22% higher Cinv that could be explained by two main reasons: (i) a parasitic bottom device is formed when the nanosheet structure is fabricated on bulk Si substrate. This parasitic device contributes more to capacitance than to current. (ii) bottom gate height is increased due to an additional sacrificial SiGe layer for SBC pMOS, and adds capacitance from gate to drain.

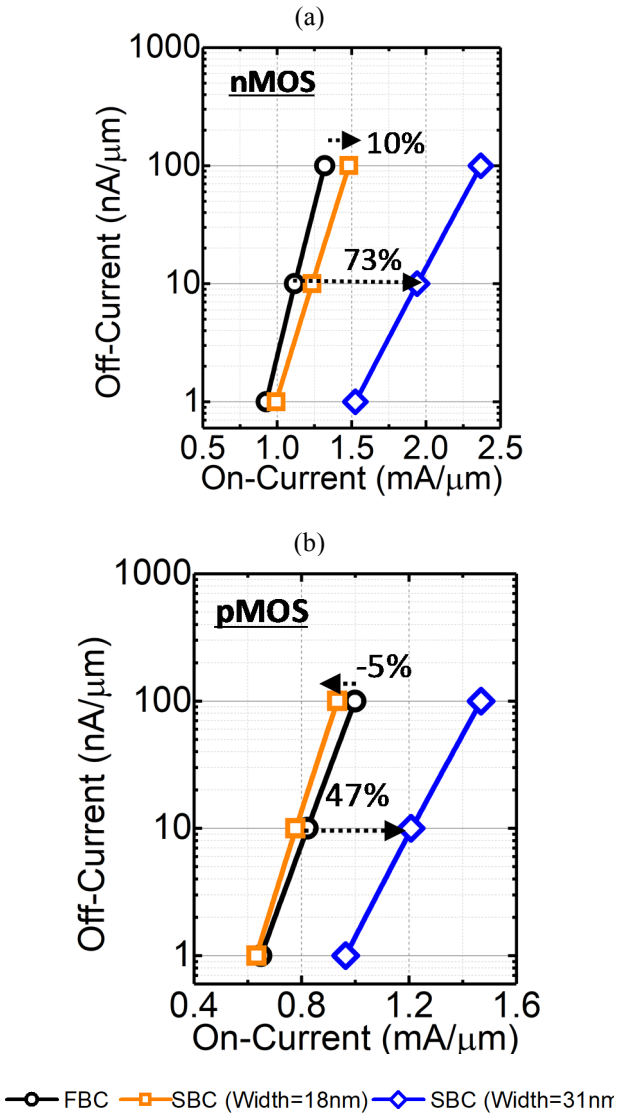


Fig. 11. Ion-Ioff performance comparison for (a) nMOS and (b) pMOS. SBC nMOS shows 10% Ion-Ioff improvement over FBC; SBC pMOS shows 5% Ion-Ioff degradation compared to FBC. For both nMOS and pMOS, increasing Nanosheet width to 31nm (to match the same active device footprint as CFET with 2 Fin design) significantly improved performance.

When comparing the on-state current at the same off-state current, SBC nMOS shows 10% Ion improvement over FBC (Fig.11a) while SBC pMOS shows 5% Ion degradation compared to FBC (Fig.11b). To match the same active device footprint as of FBC CFET with 2 fin design, nanosheet width in SBC is increased to 31nm. With increased nanosheet width, nMOS and pMOS drivability can be higher than FBC by 73% and 47% respectively due to higher effective channel width.

To evaluate the combined impact of drive-current and parasitic capacitance on circuit performance, a 31-stage ring oscillator is simulated as a representative circuit. SBC overall RO performance (frequency) is 2.6% better compared to FBC

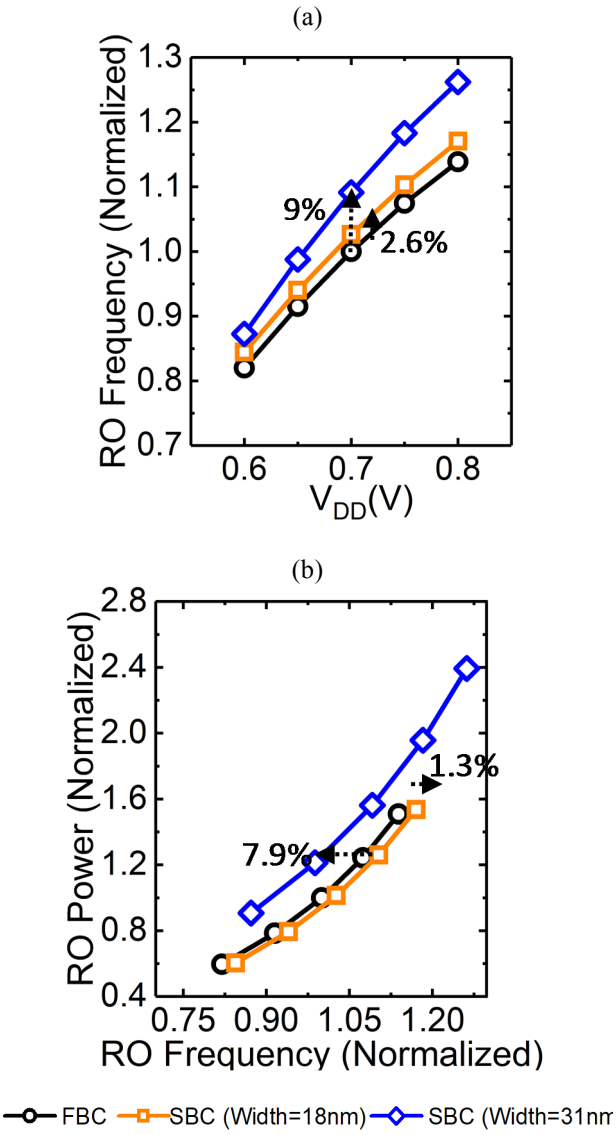


Fig. 12. Ring-oscillator Performance comparison of 3 CFET structures

(Fig.12a). With increased nanosheet width, RO performance can be 9% better than FBS due to higher drivability. For the same power consumption, SBC with 18nm nanosheet width shows 1.3% higher performance (Fig.12b). With increased nanosheet width, the capacitance in SBC becomes higher, which leads to lower performance.

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