L-UTSOI: A compact model for low-power analog and digital applications in FDSOI technology

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***Abstract*— With the maturity of CMOS technologies and their use for low power various analog and digital applications, some additional effects must be modeled or enhanced to improve the accuracy of SPICE models. Indeed, with the decrease of supply voltages/currents and the use of the back bias in Fully-Depleted Silicon On Insulator (FDSOI) technologies, the devices operate close to the weak-moderate inversion, where gm/Id figure is impacted by effects like the depletion of source/drain electrodes and the parasitic currents such as Impact ionization current in moderate inver-sion and Gate Leakage current in weak inversion, can have a significant impact on the model accuracy. This paper describes the latest significant improvements of L-UTSOI model (formerly Leti-UTSOI) related to version 102.4. These model extensions are validated against Silicon experimental data.**

Keywords*— *L-UTSOI, compact model, SPICE, FDSOI.

I. INTRODUCTION

L-UTSOI [1] is a compact model dedicated to Fully-Depleted on Silicon-On-Insulator (FDSOI) Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) technologies with low doped channel, developed at CEA-LETI and previously named Leti-UTSOI [2]. This SPICE model, used in semiconductor industry, is a standard model [1] available in most commercial simulators. L-UTSOI is a surface-potential based model that accounts for the creation of a strong inversion layer at the both interfaces and contains all relevant physical effects such as mobility degradation at high field, velocity saturation, short channel effects, gate currents, backplane depletion, gate induced source/drain leakage, STI induced stress effects, self-heating, etc [3]. L-UTSOI model gives an accurate description of currents, charges and their derivatives (i.e. transconductance, conductance and capacitances and higher order derivatives). The latter is especially important for analog and RF circuit designs.

In this paper, we present the new physical insights included in L-UTSOI model version 102.4 [3]. In Section II, we focus on the gm/Id dedicated to short channel transistor and, in section III, we describe the impact ionization evidence and modeling, in section IV, we detail accurate model for overlap gate currents. And last section illustrates L-UTSOI model extraction using 28nm FDSOI technology.

II. FOCUS ON GM/ID: INTRODUCTION OF EFFECTIVE DOPING

L-UTSOI model is used for analog designs and gm/Id is one of the key figures of merit. To address this point we have improve initial short channel model [2] in moderate inversion regime. Figure 1.a and 1.b illustrates the discrepancy on short channel gm/Id figures of merit. The origin of this inaccuracy comes from the Source and Drain (S/D) depletion, which affects the transistor DC behavior in the subthreshold and moderate inversion regimes. In L-UTSOI, this effect of S/D depletion is accounted by modifying the boundaries conditions at the source/drain sides in the calculation of the 2D electrostatic effect (i.e. as a correction to the surface potential calculation that modulates the Short Channel Effect (SCE) and the Drain Induced Barrier Lowering (DIBL)).

The starting point of this improvement for the short channel devices is the calculation of the longitudinal profile (x direction) of the surface electrostatic potential accounting for short channel effects [4]:

$$\psi_{2D(x)} = \psi_{1D} + \left(\psi_{edge} - \psi_{1D}\right)e^{-x/\lambda_{2D}} + \left(\psi_{edge} - \psi_{1D}\right)e^{-(L-x)/\lambda_{2D}} \quad (1)$$

where ψ_{1D} is a smooth minimum function between the long channel surface potential at the center and its threshold value (to extend the validity in moderate inversion), ψ_{edge} is the electrostatic potential at the edge of S/D regions and λ_{2D} is the bi-dimensional characteristic length of the device.

This expression is valid in the subthreshold regime, where the longitudinal electric field at the edge of the S/D region is, respectively: $E_{x,edge} = \pm\left(\psi_{edge} - \psi_{1D}\right)/\lambda_{2D}$. In the depleted region of the S/D electrodes, we simplify the bi-dimensional Poisson's equation by considering that a fraction α of the depletion charge acts on the longitudinal electric field. Writing x_{dep} the depleted region, we have:

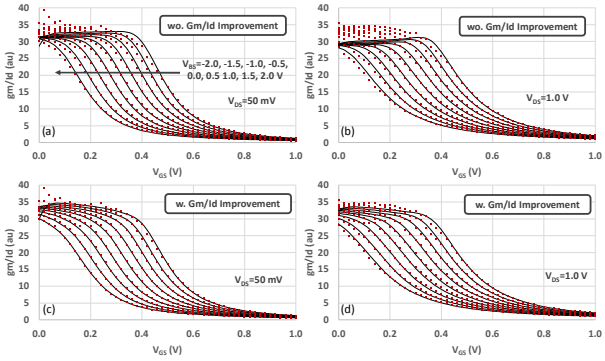

Fig. 1: Comparison between experiments from 28nm technology (symbol) and model (line): For short & wide device gm/Id versus VGS for different VBS without (a) & (b) and with (c) & (d) model improvement (extraction of dedicated NSDDC parameter). (note current has been normalized).

$$\varepsilon_{Si} E_{x,edge} = q\alpha N_{sd} x_{dep} \quad (2.a)$$

$$\psi_{electrode} - \psi_{edge} = E_{x,edge} x_{dep}/2 \quad (2.b)$$

where ε_{Si} is the dielectric permittivity of silicon, q is the electron charge, N_{sd} is the S/D doping level and $\psi_{electrode}$ is the electrostatic potential in the neutral part of the considered electrode (S or D). Together with the previously electric field expression, we obtain the electrostatic potential at electrode edge as:

$$\psi_{edge} = \psi_{1D} + \psi_{dep}\left[\sqrt{1 + 2\,(\psi_{electrode} - \psi_{1D})/\psi_{dep}} - 1\right] \quad (3)$$

where $\psi_{dep} = q\alpha N_{SD}\lambda_{2D}{}^2/\varepsilon_{Si}$ is the depletion potential parameter and where the key parameter to modulate the depletion and, consequently gm/Id, is the effective doping αN_{SD} (named NSDDC as model parameter). The implementation of this effect is detailed in the user's manual [3].

Figure 1.c and 1.d shows the modeling results obtained on short and wide channel transistor gm/Id for a wide range of back biases from -2V to +2V in linear and saturation regimes. An accurate description of the device 2D electrostatics is achieved over this wide back bias range, including the moderate inversion regime thanks to implementation of S/D depletion.

III. Impact Ionization Evidence and Modeling: Low-Level Avalanche Multiplication Current

For a transistor operating in saturation, the longitudinal electric field at the drain side may reach very high values. In this case, electrons travelling through the channel from S to D are accelerated and energy gain can create extra electron-hole pairs by exciting electrons from the valence band into the conduction band. This phenomenon is commonly referred to Impact Ionization (II). In this way, an avalanche of free carriers may arise and the initial flux of carriers is multiplied. In FDSOI transistor, this effect is more significant for thicker oxide transistors, featuring higher supply voltages, and only weak avalanche occurs. This component increases the source/drain

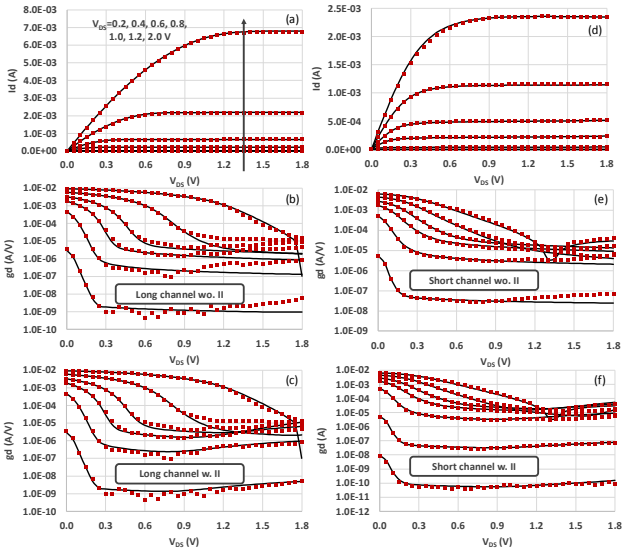

Fig. 3: Comparison between experiments from 28nm technology (symbol) and model (line): For long & wide device (respectively short & wide) (a) drain current versus V_{DS} (respectively (d)), (b) first derivative of drain current (gd) versus V_{DS} without Impact Ionization (respectively (e)) and (c) gd versus V_{DS} with Impact Ionization (respectively (f)) for different V_{DS}. (note current has been normalized).

current (in opposition to bulk MOSFET where the impact ionization results in a bulk/drain current).

Formally, the inclusion of this model in term of physics and code implantation is close to that of PSP model [5]. For low-level avalanche multiplication, the avalanche current is [6]:

$$I_{aval} = I_{DS} \cdot \int_0^L \alpha_n \cdot dx \sim A1 \cdot \Delta V_{sat} \cdot I_{DS} \cdot e^{-\frac{a_2}{\Delta V_{sat}}} \quad (4)$$

where A1 is the II pre-factor, $a_2 = A2 \cdot (T_{KC}/T_{KR})^{STA2}$, A2 is the II exponent, STA2 is the temperature parameter, T_{KC} & T_{KR} are the channel temperature & reference temperature, $\Delta V_{sat} = V_{DS} - A3 \cdot V_{DSsat}$ where V_{DSsat} is the drain to source saturation voltage internally calculated using the surface potential calculation, A3 is the saturation dependence II parameter and I_{DS} is the drain to source current. These 3 model parameters (A1, A2 and A3) are extracted similarly as done with PSP model [5].

Figure 2 shows the comparison between experimental data and simulation including or not this impact ionization current on thick oxide transistor. The agreement is very good using the II current and as expected, the avalanche is small enough to be accurately modeled with the weak avalanche equation previously described. Note also that this extraction has been realized with the self-heating effect activated in the model to capture as accuratly as possible the negative output conductance for high drain current levels.

IV. Accurate Model for Overlap Gate Currents: Fowler-Nordheim Current

In this section, we detail the improvements brought to the gate current model in L-UTSOI. In fact, the gate current model is built similarly as in PSP model [7]. Initially this model comes

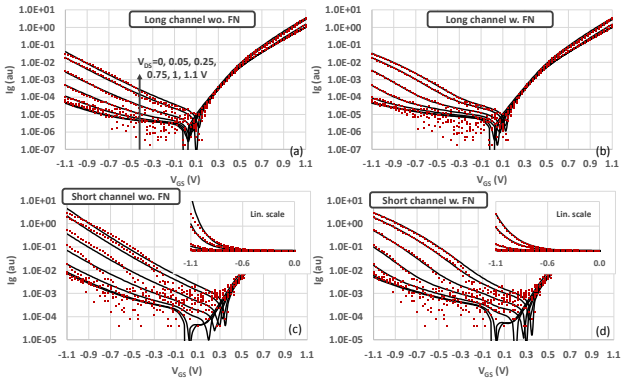

Fig. 3: Comparison between experiments from 28nm technology (symbol) and model (line): gate current versus V_{GS} for long & wide device (respectively short & wide (c-d)) without Fowler-Nordheim (a) (respectively (c)) and with Fowler-Nordheim (b) (respectively (d)) for different V_{DS}. (note current has been normalized).

from [8], where the integration over energy is skipped to obtain explicit function by assuming that all electrons have the same kinetic energy. So, the gate current density at point x in the channel is given by [7-8]:

$$J_{g_{(x)}} = J_0 . \int_0^{\infty} D_{(E,x)} . Fs_{(E,x)} . dy \sim J_0 . D_{(x)} . Fs_{(x)} \qquad (5)$$

where $D_{(E,x)}$ is the transmission coefficient calculated in the WKB approximation, $Fs_{(E,x)}$ is the supply function and x is the position along the channel. This transmission formulation requires further simplification for circuit design. The Taylor expansion is used to obtain [7]:

$$D_{(x)} = e^{-B0.f_{(zg)}} \qquad (6.a)$$

$$f_{(zg)} = \frac{1-(1-zg)^{1.5}}{zg} \sim -\frac{3}{2} + G2.zg + G3.zg \qquad (6.b)$$

where zg is the voltage drop through the gate oxide normalized to the built-in voltage, J_0 and B_0 are constant related to the tunneling current and G2 and G3 are parameters related to Taylor expansion. These two last parameters are the well-known GC2 and GC3 parameters in PSP [5] or GC2OVINV and GC3OVINV in L-UTSOI for overlap region [3]. Reference [7]: clearly explains that these parameters are tunable to compensate the huge assumptions made previously on the integral over energy. In fact, these parameters directly affect the electric field effect on the current shape.

As illustrated on Figure 3.a and 3.c, the extraction of the gate current parameters on long & wide and short & wide channel NMOS transistors evidences that the model is well aligned with experimental data. Nevertheless, it appears to be difficult to perfectly reproduce the gate current for high drain bias in overlap region. GIDL is not the root cause of such effect because this component is smaller than the gate current. The discrepancy observed on different gate current curves is evident for large negative V_{GS} and positive V_{DS} (in NMOS convention); in fact, we observe 2 different behaviors at low and high V_{GD} values.

If we deeply investigate our actual approach (equation 5 and 6), the transmission coefficient is close to the Direct Tunneling

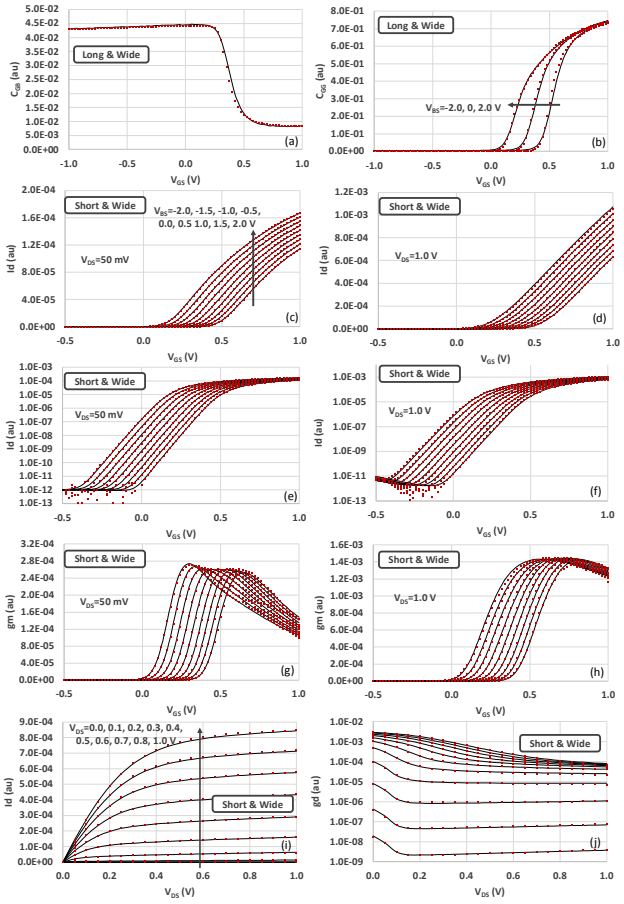

Fig. 1: Comparison between experiments from 28nm technology (symbol) and the model (line). C_{GB} (a) & C_{GG} (b) versus V_{GS} for long & wide device. For short and wide device: current versus V_{GS} in linear regime in lin (c) and log (e) scale (respectively (d) and (f) in saturation regime); first derivative of drain current (gm) versus V_{GS} in linear (g) and saturation (h) regime and Id versus V_{DS} (i) and first derivative of current versus V_{DS} (j). (note current and capacitance has been normalized).

formulation [9]. Historically [10], Fowler-Nordheim tunneling was sufficient to reproduce the gate current in technology generations with oxide thickness above 3-4nm. Indeed, the gate current is dominated by the tunneling of electrons through a triangular dielectric barrier in that case. However, for thinner oxide and with the reduction of the supply voltage the barrier is close to trapezoidal shape and Direct Tunneling is no longer negligible. Nevertheless, the both effects of negative gate voltage and positive drain voltage strongly increase the potential drop across the oxide. Following the definition introduced in [10], we propose to add an additional term related to high electric field close to Fowler-Nordheim equation. The modified gate current equation is:

$$J_g \sim J_0 . Fs_{(x)} . \left[e^{-B0.\left(f_{(zg)}\right)} + FNOV . e^{-B0.\frac{GCOVFN}{zg}} \right] \qquad (7)$$

where FNOV and GCOVFN are the new parameters that govern this Fowler-Nordheim term. Figure 3.b and 3.d, illustrates the comparison between the new model and experimental data, the behavior has been enhanced on the full range of bias conditions.

V. L-UTSOI MODEL EXTRACTION USING 28NM FDSOI TECHNOLOGY

Following the model extraction strategy [3], we have realized a parameter extraction using 28nm FDSOI technology. L-UTSOI is able to model all the features of FDSOI transistor characteristics for any bias configuration, including the case of the strong forward back bias, where two channels take place at the front and back interfaces of the thin silicon body.

Figure 4 illustrates the very good agreement on different electrical characteristics: capacitances (4.a & 4.b C_{GB} and C_{GG} versus V_{GS}) and currents with their associated derivatives (4.c to 4.i Id, gm, gd versus V_{GS} and V_{DS}) in different back bias ranges for short and wide devices. This accuracy is obtained thanks to the activation of backplane depletion, quantum confinement, mobility distinction between front & back channels and physical effects detailed in previous parts.

VI. CONCLUSION

In this paper, we have presented the recent improvements brought to L-UTSOI model to improve its accuracy and predictability in moderate and weak inversion regions. By comparison with experimental data, we have illustrated the enhanced accuracy obtained on gm/Id thanks to the introduction of source/drain depletion effect, on the output conductance thanks to the implementation of the impact ionization effect, and on gate tunneling current, thanks to the adding of a Fowler-Nordheim component. The L-UTSOI model is available in all major commercial SPICE simulators. Those three enhancements significantly contribute to demonstrate L-UTSOI readiness for Low Power circuit design applications

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