Self-Aligned Single Diffusion Break Technology Optimization Through Material Engineering for Advanced CMOS Nodes

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***Abstract*— Though single diffusion break (SDB) acts as an efficient area-scaling enabler for current CMOS technology nodes, it degrades devices' variability performance, which can be mitigated by enabling self-aligned SDB (SA-SDB) technology. Unfortunately, SA-SDB causes PMOS performance degradation due to channel stress relaxation. To solve this issue, we propose material engineering of SA-SDB technology to improve PMOS performance. Using 3D-TCAD simulations, we show that by using stressed oxide for the SA-SDB cavity fill, both PMOS and NMOS device performance can be improved. Furthermore, using ring-oscillator as a representative circuit for CMOS technology evaluation, we showed that the circuit performance can be improved by 13-21% for 2-3 GPa stress in the oxide, thus enabling simultaneous area-scaling and circuit and variability performance improvement with SA-SDB technology for advanced CMOS nodes.**

Keywords*— *Self-aligned Single Diffusion Break, FinFET, Stress relaxation, Ring-oscillator

I. Introduction

Single diffusion break (SDB) as an area scaling enabler is replacing double diffusion break (DDB) in recent CMOS technology nodes [1-3]. Along with area-scaling advantage, SDB comes with the problem of mask placement error leading to epi-volume reduction and drive current variability. To eliminate the mask placement error issue, self-aligned single diffusion break (SA-SDB) technology has recently been proposed [4]. However, SA-SDB impacts the PMOS device performance heavily by relaxing the compressive channel stress induced by the source/drain SiGe source/drain epitaxy. In this paper, we propose a material engineering approach, consisting of stressed oxide deposition in the SA-SDB cavity to recover and further boost the PMOS channel stress and hence the device and circuit performance.

1(a)

FinFET Process Flow

- Fin
- Dummy-Gate
- Spacer
- Source/Drain Epi
- ILD
- Self-Aligned SDB
- RMG
- Contact Trench (CT)
- Contact Gate (CG)
- Via-0 (V0)
- M0
- Via-1 (V1) & M1

1. Fin-cut Patterning
2. Dummy poly-gate etch
3. Active & sub-fin etch
4. Oxide fill
5. Oxide CMP

1(b)

Parameter	Value
Gate Pitch	45 nm
Fin Pitch	24 nm
Fin Width	5 nm
Fin Height	60 nm
Gate Length	14 nm

Figure 1. (a) FinFET process flow used in TCAD process simulation with self-aligned single diffusion break module (SA-SDB). (b) Typical 3nm node parameters used in the TCAD simulations.

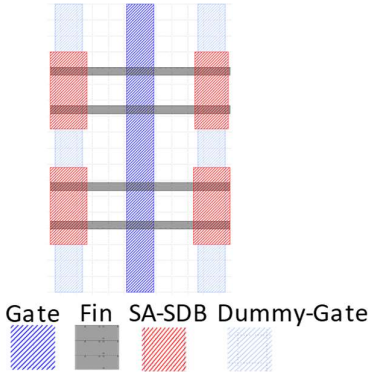

Figure 2. Typical inverter layout for 3nm node showing important layers – fin, gate, dummy gate and SA-SDB. 2 fin structures are assumed for both NMOS and PMOS.

II. Description of Approach

3D-TCAD FinFET process (Fig. 1a) and device simulations are performed to analyze the impact of SA-SDB on device performance for 3nm node (Fig. 1b). In SA-SDB module, first a lithography step is performed using the SA-SDB patterns (Fig. 2). Next the dummy gate and fin are etched creating the SA-SDB cavity, which is then filled with oxide, followed by CMP for planarization. The 3 nm (Fig 3) baseline device does not go through the SA-SDB module. The number of devices (NOD) between the SA-SDB patterns can vary depending on the complexity of the standard cell. Fig. 4 shows a cross-section of device with SA-SDB for NOD=3.

For PMOS with NOD=1, the device has SA-SDB pattern on its both source and drain sides. As a result, after the dummy-gate & fin etch in SA-SDB module, both source & drain SiGe epitaxy can expand, which leads to complete relaxation of the compressive stress in the channel (Fig. 5b).

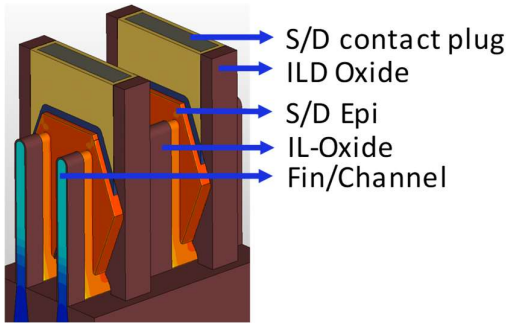

Figure 3. 3D-TCAD 2-fin FinFET structure generated by process simulation using the process flow depicted in figure 1

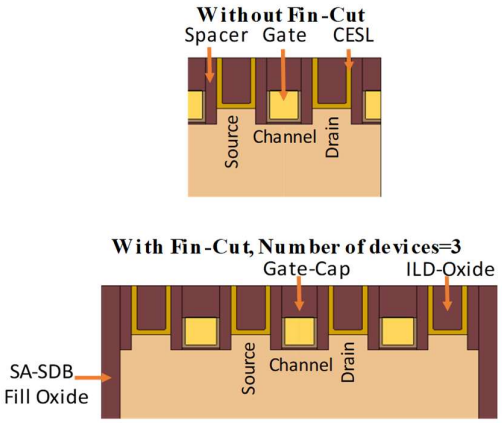

Figure 4. Cross-section of simulated devices with and without SA-SDB fin-cut showing different parts of the FinFET

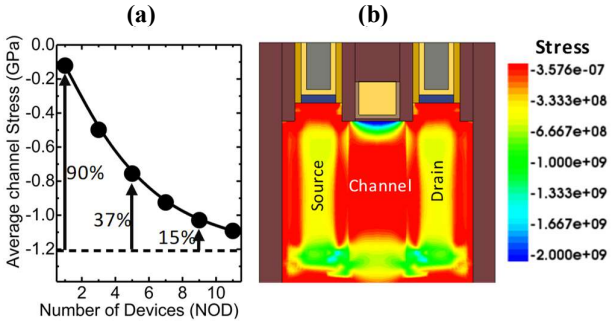

Figure 5. (a) Degradation in channel stress as a function of number of devices (NOD) between 2 fin-cuts (b) FinFET stress distribution for NOD=1, showing very small amount of stress inside channel.

Thus, for the PMOS device with NOD=1, the stress relaxation is close to 90% (Fig. 5a), in line with [4]. The channel stress can be recovered by depositing a stressed oxide during the oxide fill step in SA-SDB module.

III. Results and Discussion

We will focus on PMOS device with NOD=1 to analyze for stress recovery as this device suffers from maximum stress loss. When a stressed oxide is used for SA-SDB cavity fill, the stress gets transferred from oxide to the channel, indicating the effectiveness of this method (Fig. 6a). A compressive stress in

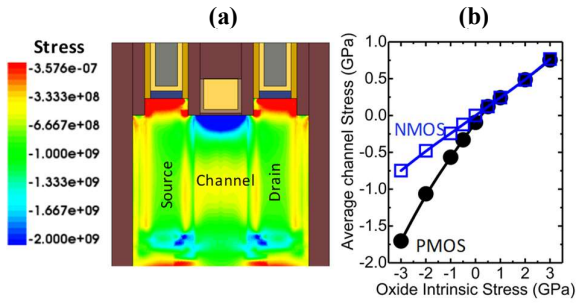

Figure 6. (a) FinFET stress distribution for NOD=1, when 2GPa compressive stress is introduced in the SA-SDB fill oxide, showing recovery of channel stress. (b) Average channel stress as a function of SA-SDB fill oxide intrinsic compressive and tensile stress for NOD=1

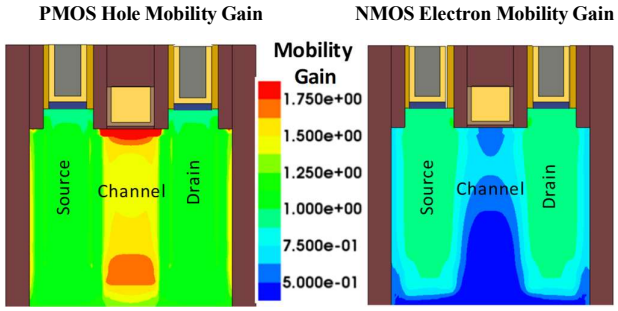

Figure 7. PMOS and NMOS mobility gain when 2GPa compressive stress is used in SA-SDB fill oxide with NOD=1.

the oxide helps to recover compressive channel stress for the PMOS device (Fig. 6b).

A tensile stressed oxide may be preferred for NMOS, leading to tensile channel stress. Having differently stressed oxide fill for NMOS and PMOS calls for additional lithography and process steps. Hence there is a trade-off between performance, cost of fabrication and process complexity.

For a 2 GPa compressively stressed oxide, PMOS channel mobility is boosted by a factor of 1.5 for most part of the channel (Fig. 7). The top of the fin has relatively higher compressive stress, leading to higher mobility boost in this region. Opposite to PMOS, the mobility in NMOS channel is reduced by a factor of 3 when an oxide with 2 GPa intrinsic compressive stress is used for SA-SDB cavity fill (Fig. 7). However, for 2 GPa intrinsic tensile stress in oxide, PMOS mobility decreases to ~0.6X compared to the case without stress in oxide (Fig. 8). The NMOS mobility increases to ~2.4X under same scenario.

The off-currents increases for both tensile and compressive stress and for both NMOS and PMOS due to bandgap and barrier height reduction (Fig. 9). Like mobility, NMOS and PMOS on-current increases with tensile and compressive oxide stress respectively.

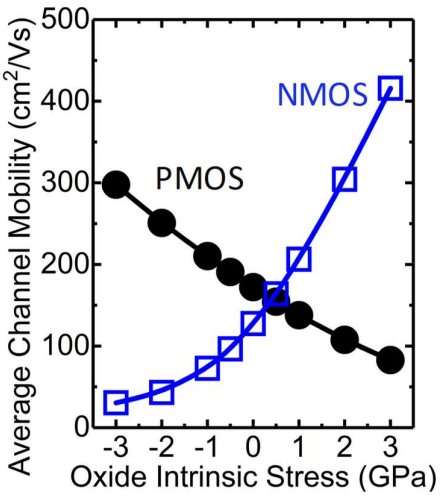

Figure 8. Average NMOS and PMOS channel mobility as a function of SA-SDB fill oxide intrinsic stress for NOD=1

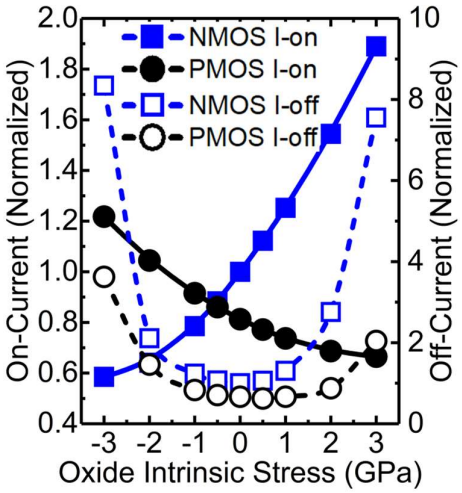

Figure 9. NMOS and PMOS on-current and off-current as a function of SA-SDB fill oxide intrinsic stress for NOD=1

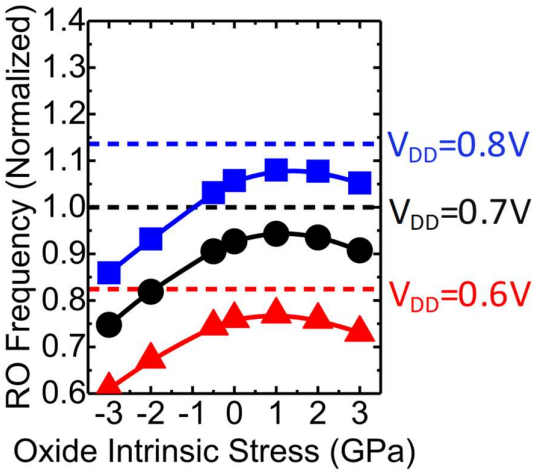

Figure 11. 31-stage ring-oscillator frequency when same type of stress (either tensile or compressive) is used for both NMOS and PMOS in SA-SDB fill oxide.

At constant off-current (achieved by work-function tuning), the PMOS device on-current degrades by 16% when the SA-SDB fin-cut is performed and its cavity fill oxide is deposited without any intrinsic stress (Fig. 10). The on-current for PMOS can be fully recovered with 2GPa intrinsic compressive stress in SA-SDB oxide fill. With 2 GPa tensile stress in oxide, the PMOS on-current degrades by 31% compared to the baseline case. For NMOS, the baseline device does not have any stress in channel. Hence performing SA-SDB fin-cut does not impact its drive-current. With 2GPa compressive stress in oxide fill, its drive current degrades by 40% (Fig. 10). However, with 2 GPa tensile stress in oxide, the NMOS drive current can be boosted by 42%.

To analyze the impact of stress recovery in SA-SDB technology on circuit performance, 31-stage ring-oscillator (RO) simulations are performed using the framework described in [5]. Two scenarios are studied. In the first one, same oxide fill is performed for both NMOS and PMOS. Thus both NMOS and PMOS have same type of stress. For compressive stress, NMOS drive-current degrades. So overall RO performance (frequency) degrades for compressive stress (Fig. 11). For tensile stress, PMOS drive-current degrades. Thus, the RO frequency degrades as PMOS becomes the bottle-neck. Thus for either tensile and compressive stress, the RO frequency is lower than the baseline case (without SA-SDB fin-cut). In this scenario, the RO performance (frequency) is optimum with ~1 GPa tensile stress and is ~ 5% lower than the baseline case.

In the second scenario, a tensile and compressively stressed oxide fill with same magnitude of stress are assumed for NMOS and PMOS respectively. Since both NMOS and PMOS drive current improve in this scenario, it is possible to achieve same RO performance as of baseline with 1GPa oxide stress (Fig. 5b). Using higher amount of oxide stress - such as 2 or 3 GPa, RO performance can be enhanced upto 13% and 21% respectively, thus highlighting the effectiveness of stressed oxide deposition.

IV. Conclusion

Using 3D-TCAD simulations, we demonstrated that the stress loss in PMOS with self-aligned single diffusion break technology can be fully recovered using compressively stressed oxide fill. We also showed that using oxide fill with

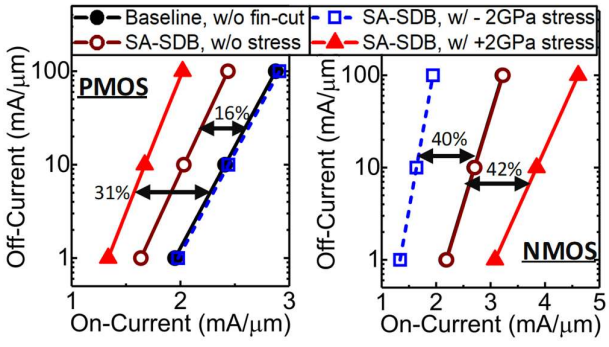

Figure 10. I-on vs I-off characteristics of NMOS and PMOS in presence of SA-SDB, with and without stress in fill oxide

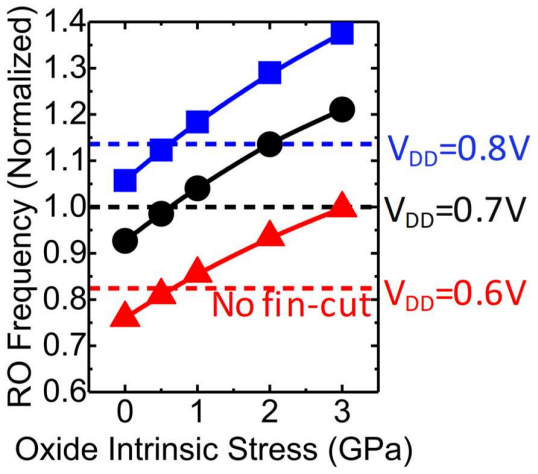

Figure 12. 31-stage ring-oscillator frequency when opposite types of stress are used for both NMOS and PMOS in SA-SDB fill oxide. Tensile stress is used for NMOS, whereas compressive stress is used for PMOS

compressive stress oxide for PMOS and tensile stress for NMOS can improve both device performance. In this scenario, the ring-oscillator performance can be improved by 13-21% for 2 - 3 GPa intrinsic oxide stress.

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