Impact of Schottky Barrier on the Performance of Two-Dimensional Material Transistors

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***Abstract* — Double-gated monolayer two-dimensional (2D) material transistor is expected to offer ideal (~60 mV/dec) subthreshold swing (SS) for gate lengths well below 10 nm. However, the ideal 2D transistor assumes Ohmic contacts whereas a realistic metal/2D Schottky contact can degrade SS. Transport simulations including scattering is necessary to correctly describe carrier thermalization and predict the SS degradation. Scaled 2D transistors with a Schottky barrier height (SBH) smaller than 100 meV and doping concentration in the extension region larger than $2x10^{13}$ cm^{-2} are required to achieve high performance.**

Keywords*- 2D *van der Waals materials, WS_2, Schottky contact, sub-threshold swig, future CMOS technology

I. Introduction

For applications of abundant-data computing in the immediate future, high density transistors integrated with functional (e.g. memory) components are needed [1]. Unavoidable surface roughness of three-dimensional (3D) bulk materials (e.g. Si, Ge, and III-V compounds) limits the scaling of transistors [2]. Two-dimensional (2D) van der Waals materials with pristine surface in principle are promising for continuous transistor scaling and heterogeneous integration [2]. Owing to the appropriate transport effective mass and high phonon-limited mobility of both electrons and holes, monolayer (ML) tungsten disulfide (WS_2) is one of the potential channel candidates for future CMOS technology [2]. In addition to the intrinsic material property, Schottky contact between metal and 2D semiconductor is known as a challenge to achieve high performance [3, 4]. However, most of the studies treated intrinsic channel performance and Schottky contact resistance independently. The coupling effect between carrier injection from Schottky contact and carrier transport through the channel is ignored. In this work, we simulate the electrical characteristics of ML WS_2 nFET and pFET with integrated source/drain (S/D) Schottky contact considering phonon scatterings. The Schottky barrier degrades the performance of 2D transistors more than just increasing the contact resistance. Phonon scattering and the designs in the extension region could impact the sub-threshold swing of the extremely scaled transistors.

II. Methodology

The bandstructure calculation of ML WS_2 is based on density functional theory (DFT) and the generalized gradient approximation (GGA) in the form of Perdew-Burke-Ernzerhof (PBE) functional with spin-orbit coupling (SOC) applied [5]. The kinetic energy cutoff and k-point mesh were set to 110 Hartree and $10\times10\times1$, respectively. Figure 1a shows the calculated 2D k-space constant energy contours of the lowest energy conduction band of ML WS_2 with Brillouin-zone and high symmetry k-points indicated. Figure 1b shows the calculated bandstructure along high symmetry k-points. The top valance band with spin-orbit splitting is in good agreement with experimental results measured by angle-resolved photoemission spectroscopy (ARPES) [6]. The electronic band structure was then replicated by multi-valley effective mass approximation with non-parabolicity. The ML WS_2 is approximated as an ideal zero-thickness two-dimensional electron/hole gas (2DEG/2DHG). For tunneling simulations based on the WKB approximation, complex bandstructure inside the forbidden gap was computed perturbatively from the real-*k* states [7]. Electron and hole transports were simulated by self-consistently solving 2D Boltzmann transport and Poisson equations including acoustic and optical phonon scatterings [7, 8]. Schottky barrier height (SBH) as a parameter is defined as the difference between the contact metal workfunction and the band edge of ML WS_2 with Fermi energy fixed at the boundary.

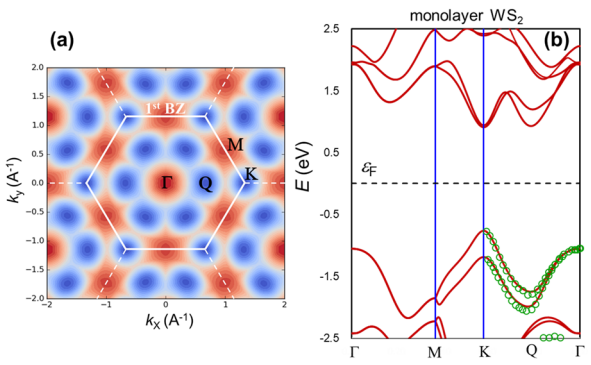

Fig. 1 (a) 2D *E-k* contour of the bottom conduction band of ML WS_2 with 1st Brillouin-zone (BZ) and high-symmetry k-points indicated. Red color for higher energy; blue color for lower energy. (b) Bandstruture of ML WS_2 along high-symmetry directions indicated in Fig. 1a with Fermi level ε_F at zero energy. Symbols are experimental results of ARPES from [6].

III. Result & Discussion

Figure 2a shows the side view of the device with double-gated and S/D edge contact architecture for good electrostatic control and large effective width [2]. The gate length L_G and equivalent oxide thickness (EOT) used are 10 nm and 0.8 nm respectively. With minimal parasitic resistance, intrinsic electrical performance of n- and p-FETs ML WS_2 are nearly symmetric, as shown in Fig. 2b. Although the transport effective mass of hole (~ 0.4 m_0) is heavier than that of electron (~ 0.3 m_0), the large energy separation (> 300 meV) between K and Γ valleys of valence band (Fig. 1b) suppresses intervalley scattering resulting in higher phonon limited mobility than that of nFET [8]. Also, the large energy separation mitigates the velocity degradation from carrier populating into the satellite (Γ) valley with heavy mass at high V_G.

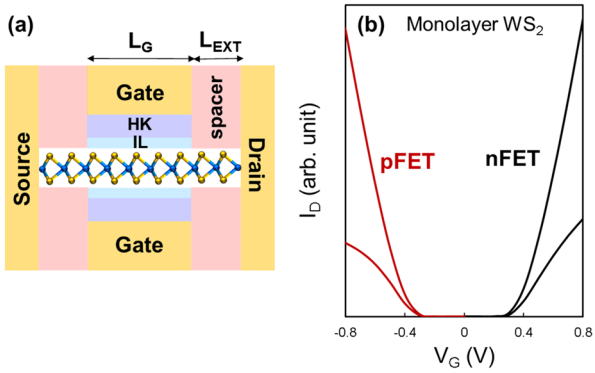

Fig. 2 (a) Simulated device structure with gate length L_G = 10 nm and EOT = 0.8 nm. Material of IL/HK and spacer are *h*-BN/HfO_2 and Si_3N_4 respectively. Under spacer is the extension region with extension length L_{EXT} and doping concentration N_{EXT}. (b) Simulated I_D-V_G of ML WS_2 nFET (black) and pFET (red) at V_D = 0.05 V and 0.75 V with N_{EXT} = 5e13 cm^{-2} and SBH = 0 eV.

We systematically studied 2D transistor performance as a function of SBH of the metal/2D contact and doping concentration in the extension region (N_{EXT}). A correlation between effective drive current I_{EFF} [9] and parasitic resistance R_P (including contact and extension series resistances) with the same I_{OFF} is shown in Fig. 3. As a design guideline, ~70% of the intrinsic 2D transistor drive current can be retained if the total R_p is within ~100 Ω-μm, requiring a SBH of <100 meV and a N_{EXT} of ~2e13 cm^{-2}. The lack of a universal correlation between I_{EFF} and R_P indicates that the impact from SBH is more than just the increase of parasitic resistance. Different extension doping could lead to different drain induced barrier lowing (DIBL). SBH could deplete the carrier in the short extension region inducing source starvation effect [10]. Moreover, the metal/2D Schottky contact can degrade the subthreshold swing (SS). Since maintaining good SS is important for future technology and is one of the motivation to choose layered 2D materials for continuous device scaling. We focus on discussing the SBH induced SS degradation in the following paragraphs.

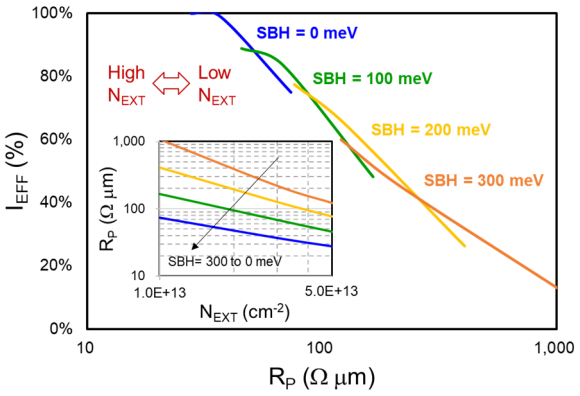

Fig. 3 Percentage of I_{EFF} [8] versus extracted parasitic resistance R_P (including contact and extension series resistances) at the same I_{OFF} = 10^{-3} μA/μm. Inset is R_P versus N_{EXT} for different Schottky barrier height (SBH) 0 (blue), 100 (green), 200 (yellow), and 300 (orange) meV.

Figure 4a shows the impact of the Schottky contact on SS of WS_2 pFET. For large SBH (e.g. > 300 meV), SS can degrade to > 70mV/dec even for the double-gated architecture with extremely thin channel. The degradation is due to energy filtering effect by the Schottky barrier which provides high kinetic energy carriers that can not be effectively controlled by the gate. For a regular MOSFET with a thermalized heavily doped extension, most of the carriers have low energies following the Fermi-Dirac distribution. However, for Schottky barrier contacts, the energy of the carriers injected from the metal is filtered by the Schottky barrier. There could be more carriers with higher energies due to thermal injection over the barrier and tunneling near the top of the barrier. Take the case of SBH = 200 meV as an example, the SS is near ideal (~ 60 mV/dec) for I_D < 10^{-2} μA/μm (channel barrier is still higher than the Schottky barrier), but becomes worse for larger I_D (V_G). As gate voltage increases and channel barrier reduces, those carriers filtered by the Schottky barrier can possess kinetic energies higher than the channel barrier which result in less effective gate control and degrade SS (Fig. 4b). Considering (especially optical phonon) scattering in the extension region is important and ballistic transport tends to be pessimistic in predicting SS (Fig. 4a). This is because optical phonon scattering can thermalize high kinetic energy carriers prescreened by the source-side Schottky barrier, and the carrier distribution at the source-side becomes closer to the Fermi-Dirac distribution at thermal equilibrium.

Figure 5a shows the impact of extension doping concentration N_{EXT} on SS for different SBH. For small SBH (e.g. 100 meV), SS degrades as doping concentration increases due to more serious short channel effect (SCE). For large SBH (e.g. 400 meV), however, SS becomes better as doping concentration increases. Considering the SB width thinning, higher doping can help recover some of the SBH induced SS degradation by increasing the tunneling probability of carriers with low energies through the SB (Fig. 4b). These two competing effects can be observed for medium SBH (e.g. 300 meV) at different current regions. A longer extension length L_{EXT} can do the same trick as higher N_{EXT} shown in Fig. 5b. With longer L_{EXT}, the scattering probability with phonon emission of

high kinetic energy carriers increases, which lowers their energies. And it can be expected that the device behaves as a regular MOSFET as L_{EXT} becomes long enough with complete carrier thermalization. However, for future CMOS technology with small gate pitch, these knobs (L_{EXT} and N_{EXT}) have limited design window without adversely affecting either the SCE or extension series resistance.

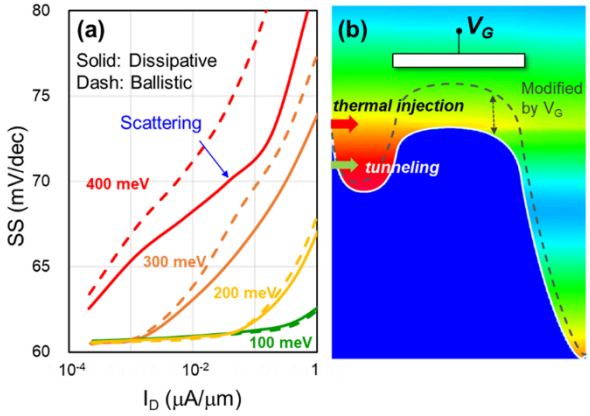

Fig. 4 (a) Sub-threshold swing SS versus drain current I_D for different SBH with L_{EXT} = 5 nm and N_{EXT} = 1e13 cm^{-2} assuming ballistic transport (dash line) and dissipative transport (solid line). (b) Distribution function (red for high and blue for low values) in energy space explains the result in (a). Horizontal axis is along the transport direction and vertical axis is energy. Grey dash line is at low V_G and white solid line is at high V_G.

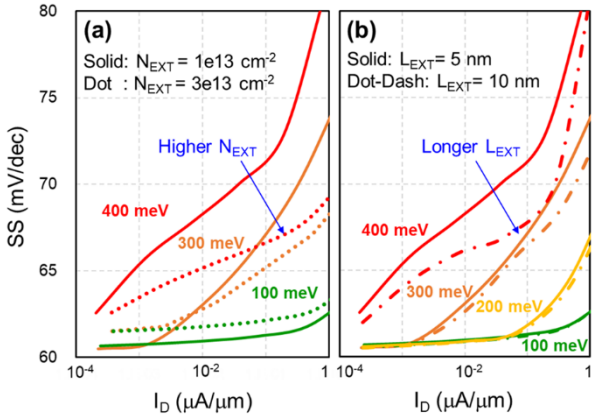

Fig. 5 SS versus I_D for different SBH. (a) Comparison of the effect of SBH on SS between low N_{EXT} = 1e13 cm^{-2} (solid line) and high N_{EXT} = 3e13 cm^{-2} (dot line) with the same L_{EXT} = 5 nm. (b) Comparison of the effect of SBH on SS between short L_{EXT} = 5 nm (solid line) and long L_{EXT} = 10 nm (dot-dash line) with the same N_{EXT} = 1e13 cm^{-2}.

IV. Conclusion

Monolayer WS_2 shows balanced nFET and pFET performances. Small Schottky barrier height for extremely scaled 2D FETs is more critical than that for Si technology nowadays. The impact of a high Schottky barrier is more than that of just the effect on contact resistance. Schottky contact can further degrade subthreshold swing and ballistic transport can over-estimate this effect. High extension doping concentration and long extension length can mitigate the swing degradation but need to be considered along with impact on short channel effect and parasitic resistance.

References

[1] A. M. M. Sabry et al., "Energy-efficient abundant-data computing: The N3XT 1,000x," Computer, vol. 48, pp. 24-33, 2015.

[2] S. K. Su, et al., "Layered semiconducting 2D materials for future transistor applications," (unpublished).

[3] D. Jena, K. Banerjee, and G. H. Xing, "Intimate contacts," Nat. Mater, vol. 13, pp. 1076-1078, 2014.

[4] D. S. Schulman, J. A. Andrew, and S. Das, "Contact engineering for 2D materials and devices," Chem. Soc. Rev., vol. 47.9, pp. 3037-3058, 2018.

[5] S. Smidstrup, et al., "QuantumATK: An integrated platform of electronic and atomic-scale modelling tools," J. Condens. Matter Phys., vol. 32.1, 015901, 2019.

[6] H. Henck, et al., "Electronic band structure of two-dimensional WS_2/graphene van der Waals heterostructures," Phys. Rev. B vol. 97, 155421, 2018.

[7] Z. Stanojević, et al., "Phase-space solution of the subband Boltzmann transport equation for nano-scale TCAD," SISPAD, pp. 65-68, 2016 & GTS Framework 2019 manual.

[8] Z. Jin, et al., "Intrinsic transport properties of electrons and holes in monolayer transition-metal dichalcogenides," Phys. Rev. B, vol. 90, 045422, 2014.

[9] M. H. Na, et al., "The effective drive current in CMOS inverters," IEDM, pp. 5.4.1-5.4.4, 2002.

[10] M. V. Fischetti, et al., "Scaling MOSFETs to 10 nm: Coulomb effects, source starvation, and virtual source model," J. Comput. Electron., vol. 8.2, pp. 60-77, 2009.