12-4

Simulation and Evaluation of Plasmonic Circuits

Mitsuo Fukuda
Electrical & Electronic information Engineering
Toyohashi University of Technology
Toyohashi, Aichi, Japan
fukuda.mitsuo.af@tut.jp

Yasuhiko Ishikawa
Electrical & Electronic information Engineering
Toyohashi University of Technology
Toyohashi, Aichi, Japan
ishikawa@ee.tut.ac.jp

Abstract— This paper presents and discusses the modeling and evaluation of plasmonic circuits including plasmonic devices such as a multimode interferometer, mode converter, multiplexer, logic circuits, and signal transmission networks.

Keywords— plasmonic waveguide, plasmonic mode convertor, plasmonic multiplexer, plasmonic integrated circuit, silicon integrated circuit

I. Introduction

High-performance information communication systems are now indispensable for daily life in various fields, and silicon integrated circuits (ICs) are key devices in such systems. The information processing speed of silicon integrated circuits, however, gradually saturate. To enhance silicon IC operating speeds, optical interconnects have begun to be introduced [1]–[3]. Plasmonic circuits are also promising candidates for this IC enhancement, although the development of these circuits is still in its primitive stage.

In the nanoscale range where silicon photonic waveguides are scarcely applied, plasmonic circuits are strong tools to construct high-speed circuits merged with silicon ICs [4]. Although plasmonic circuits generally exhibit heavy signal-transmission loss via ohmic loss, we have clarified that the circuits formed with SiO_2 stripes on a metal film within the range of less than a few hundred square micrometers exhibit lower transmission loss per single bit when compared with electric circuits even at a bit error rate of 10^{-30} [5]. In addition, we indicated the feasibility of a full adder operating at light speed without large loss or heat generation by applying the configuration developed for a cascadable plasmonic full adder to silicon waveguides [6]. For the plasmonic full adder, the basic operation of plasmonic circuits were numerically and experimentally demonstrated, and the output signals were connected to plasmonic detector-integrated metal-oxide semiconductor field effect transistors. These circuits were fabricated by combining only single- and multi-mode waveguides, the latter acting as multimode interferometers (MMIs). The circuits operated at light speed via interference of transmitted plasmonic signals. Through the plasmonic circuits, various kinds of plasmonic signals were transmitted in nano/micrometer-scale area using the techniques currently used in commercial optical fiber communication systems [4].

The design and modeling techniques for the waveguides have been relatively well established until now, but more precise design and simulation techniques are needed to fabricate the above-mentioned complicated plasmonic circuits operating via interference. Without precise simulations adjusting the waveguide shapes and the propagating modes of signals, the working nano/micrometer-scale plasmonic circuits cannot be practically fabricated. This paper presents and discusses the simulation procedures of the plasmonic circuits. The simulations provided guidelines for design and fabrication of nano/microscale plasmonic circuits, and these simulation results were experimentally confirmed by scanning near-field optical microscopy (SNOM).

II. Modeling of Plasmonic Circuits

We used the 3D finite-difference time-domain method using electromagnetic wave analysis software for the circuit simulations after calculating waveguide parameters such as propagation constants (i.e. complex refractive indices). This was done by solving the characteristic equation of a waveguide for a multilayer structure (e.g., SiO_2 film/metal film/Si substrate) and then for a mesa structure (e.g., SiO_2 mesa structure/metal film/Si substrate). For the calculation, the mesh spacing was changed from a few nanometers to a few tens of nanometers corresponding to the structural complexity to be simulated. The time spacing was set at a range of a few tens of attosecond. Perfectly matched layer (PML) absorbing boundary conditions were applied to minimize the influence of light/plasmon reflection. The large-scale integrated circuits were divided into a few sections and then precisely simulated with small mesh spacing. The circuit designs and simulations were performed taking into consideration the actual fabricated waveguide shapes and the propagating modes of plasmonic signals. The simulated circuits were actually fabricated and then evaluated using SNOM.

III. Plasmonic Waveguides and Components

Surface plasmons (SPs) are quanta of an electromagnetic wave coupled with the collective oscillation of electrons and propagate along the interface between a metal and a dielectric layer (or air) at light speed. To construct plasmonic circuits, waveguides comprising dielectric stripes deposited on a metal film (i.e., dielectric-loaded surface plasmon (DLSP) waveguides) were used in this study because the structure is technically simple and easy to translate to waveguide components. Fig.1 shows an example of a SiO_2-loded waveguide. This acts as a plasmonic single-mode waveguide in 1300 and 1550 nm wavelength bands.

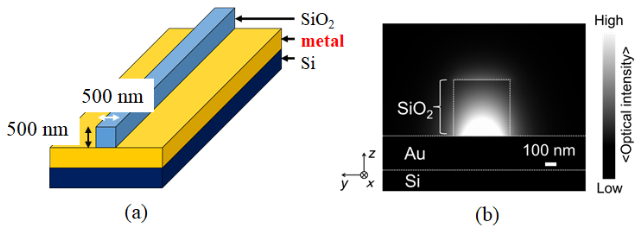

Figure 1. (a) Schematic of plasmonic single-mode waveguide in 1300 and 1550 nm wavelength bands, (b) simulated cross sectional view of optical power distribution.

This work was supported in part by JSPS KAKENHI Grant number JP18K04282.

Plasmonic circuits are planar lightwave circuits, and thus bending and crossing waveguides [7] are necessary to increase circuit flexibility. An example of simulated and experimental results for a bending single-mode waveguide are shown in Fig. 2. For a bending waveguide, an optical power distribution simulation was performed along the upper surface of the mesa-shaped SiO_2 waveguide, and the optical power along the surface was monitored using SNOM. The simulated and experimental results coincided, and simulation was used to identify an optimal structure for a bending waveguide using various conditions, curvatures and degrees of bending. Here, the waveguide samples were fabricated using focused ion beam milling etching, thus modifying the rectangular cross-sectional shapes for the etched mesa-structure. In such cases, the simulation was carried out after modifying the shape of the cross-section to match the fabricated sample. This modification was important to more exactly simulate some complex circuits, although the results of simulation and experiment were not significantly different when only a simple waveguide was examined.

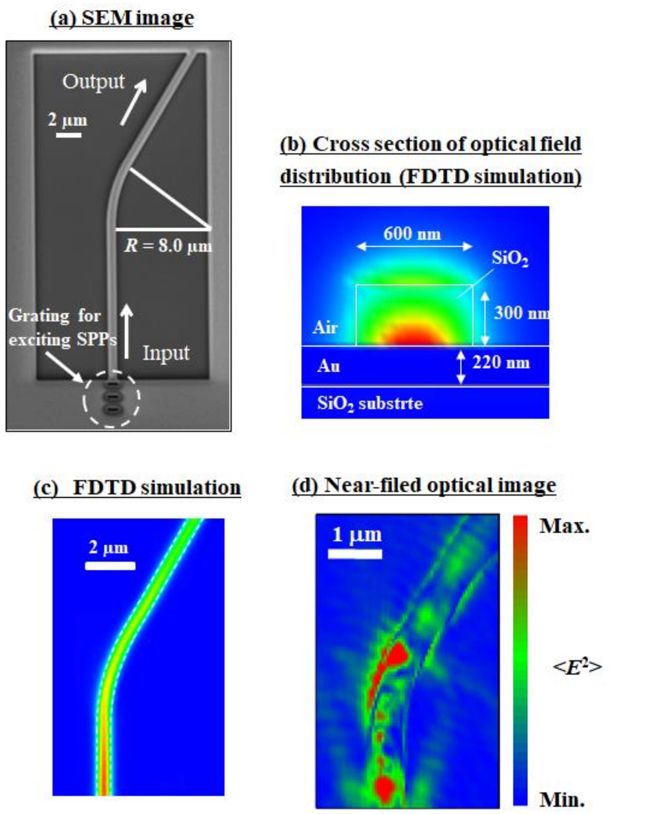

Figure 2. (a) Fabricated bending waveguide, (b) the cross section of plasmonic optical field distribution calculated with FDTD method, (c) simulated plasmonic power distribution along with the bending waveguide, and (d) plasmonic power distribution monitored by SNOM. The wavelength of light incident to the grating is set at 1300 nm.

These waveguide simulations were extended to functional components such as multiplexers, demultiplexers, and mode-converters. These components were constructed by combining single- and multimode waveguides. An example of a plasmonic multiplexer is indicated in Fig. 3. The 1310 and 1550 nm-wavelength plasmonic signals were inputted to the MMI from the different input ports and outputted to the same port through the MMI. In the FDTD simulation and SNOM image in Fig. 3, the plasmonic signal emission from the MMI part is recognized, and some tapered structures were introduced into the MMI to suppress the signal leak [8].

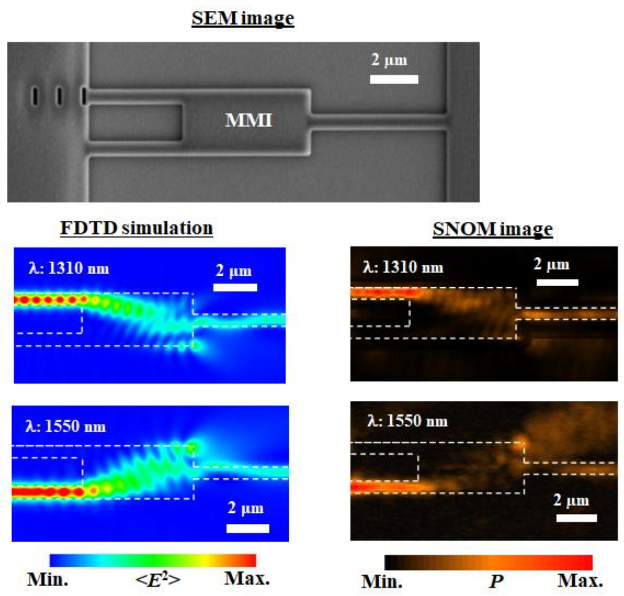

Figure 3. Fabricated multiplexer for 1310- and 1550-nm-wavelength band. The plasmonic signals are converted from highly coherent light beams at the grating set just before the input port.

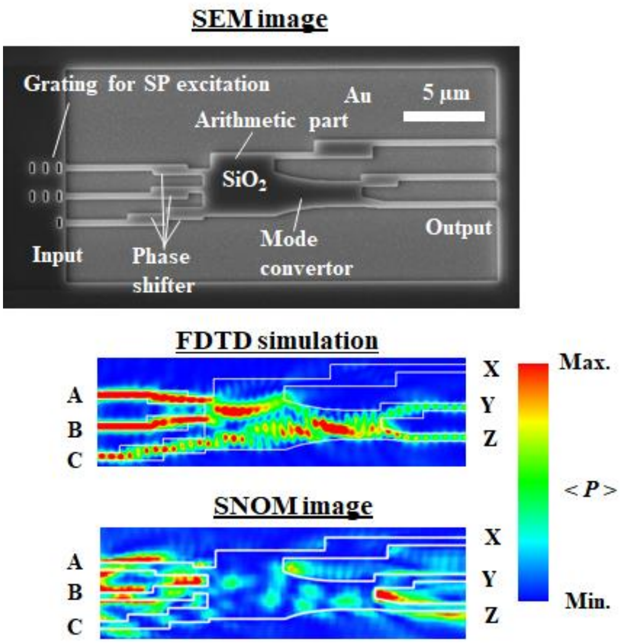

Fig. 4. Fabricated plasmonic logic circuit (half adder). The surface plasmon signals are converted from a highly coherent light beam with a 1310 nm wavelength in the air.

The waveguide and multiplexer discussed above are composed of relatively simple structures. For such components, the performances of the fabricated components well coincide with each other without confirming the distribution of the plasmonic signal phase and propagating modes in single and multimode (MMI) waveguides. In complicated plasmonic circuits, however, the distribution of signal phase and propagating mode in the waveguide has to be considered in the design, if interference of signals is employed in the components such as MMI. Fig. 4 shows the simulation and experimental results for a logic circuit, wherein a SiO_2 film was deposited and patterned on a Au film. The input signals A and B were computed (i.e., interfered in MMI) and outputted to Z through a mode converter. The output Y was an emission port for unnecessary plasmon signals after computing and the key port for maintaining correct interference without noise [9]. The half adder operated well as a Boolean logic circuit. Here, the interference patterns in the MMI (phase shifters, arithmetic part, and mode converter) had to be precisely controlled by optimizing the MMI shapes to suppress the introduction of unnecessary higher-order- mode signals to the next MMI. Without this interference mode control, working circuits with complicated networks could not be fabricated. These procedures are very important for developing nano/microscale circuits and components because experimental examination is difficult for such small components and circuits.

In addition, the propagation modes should be also paid attention at the output port of MMIs. Just after interference in MMI, some modes are introduced to the single-mode waveguide. After transmitting to some extent in the single-mode waveguide, only signals with single-mode remain. If the two MMIs are connected with a single-mode waveguide, signals with higher-order modes outputted from the first MMI are introduced to the next MMI, and the interference in the second MMI is not correctly carried out. This mixing of higher-order modes was suppressed by narrowing the waveguide or lengthening the single-mode waveguide between the two MMIs. By taking these phase and mode control into the consideration, the design and fabrication of working plasmonic cascadable full adder [6] and complicated wavelength-division-multiplexing circuits with MOSFETs [5] was accomplished.

IV. SUMMARY

For simulation and modeling of complicated plasmonic circuits and networks, modeling with reference to the actual fabricated shapes of the individual components and waveguides is indispensable for fabricating working optical networks. Controlling the transmitted optical mode by modifying the shape of the circuit and network is also a key design and fabrication factor to suppress unnecessary interference within the components. Using these techniques, functional and complicated plasmonic logic circuits and networks were obtained.

ACKNOWLEDGMENT

The authors would like to thank Dr. M. Ota, Ms. A. Sumimura, R. Watanabe, and Mr. T. Hirano for their supports and discussions on the design and fabrication of plasmonic waveguides while enrolled at Toyohashi University of Technology.

REFERENCES

[1] M. Haurylau, G. Chen, H. Chen, J. Zhang, N. A. Nelson, D. H. Albonesi, E. G. Friedman, P. M. Fauchet, “On-chip optical interconnect roadmap: challenges and critical direction,” IEEE J Selected Topics Quantum Electron, vol.12, pp.1699–705, 2006.

[2] K. Ohashi, K. Nishi, T. Shimizu, M. Nakada, J. Fujikata, J. Ushida, S. Torii, K. Nose, M. Mizuno, H. Yukawa, M. Kinoshita, N. Suzuki, A. Gomyo, T. Ishii, D. Okamoto, K. Furue, T. Ueno, T. Tsuchizawa, T. Watanabe, K. Yamada, S. Itabashi, J. Akedo, “On-chip optical interconnect,” Proc. IEEE, vol.97, pp.1186–98, 2009.

[3] D.A.B. Miller, “Optical interconnects to electronic chips,” Appl. Opt., vol. 49, pp. F59-F70, 2010.

[4] M. Fukuda, S. Okahisa, Y. Tonooka, M. Ota, T. Aihara, Y. Ishikawa, "Feasibility of Plasmonic Circuits in Nanophotonics," IEEE Access, vol.8, pp.142495-142506, 2020.

[5] M. Fukuda, Y. Tonooka, T. Inoue, M. Ota, “Feasibility of plasmonic circuits for on-chip interconnects,” Solid-State Electron. vol. 156, pp. 33-40, 2019.

[6] M. Fukuda, R. Watanabe, Y. Tonooka, M. Ota, “Feasibility of Cascadable Plasmonic Full Adder,” IEEE Photon. J., vol. 11, No. 4, Aug. 4801612, 2019.

[7] M. Ota, M. Fukuhara, A. Sumimura, M. Ito, T. Aihara, Y. Ishii, M. Fukuda, “Dielectric-loaded surface plasmon polariton crossing waveguides using multimode interference,” Opt. Lett., vol.40, No.10, pp.2269-2272, 2015.

[8] A. Sumimura, M. Ota, K. Nakayama, M. Ito, Y. Ishii, M. Fukuda, “Low return loss plasmonic multiplexer with tapered structure,” IEEE Photon. Technol. Lett., vol.28, No.21, pp.2419-2422, 2016.

[9] M. Ota, A. Sumimura, M. Fukuhara, Y. Ishii, M. Fukuda, “Plasmonic-multimode-interference-based logic circuit with simple phase adjustment,” Scientific Reports, vol. 6, 24546, 2016.