Dynamic Simulation of Write '1' Operation in the Bi-stable 1-Transistor SRAM Cell

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***Abstract*—For the first time, physical insights into the writing process in the bi-stable 1-transistor SRAM cells are provided using dynamic (time dependent) TCAD simulations. The simulations are based on 28 nm planar CMOS technology, and the setup is carefully calibrated against available experimental data. Based on the simulations, we were able to identify clearly the mechanisms involved in the write '1' operation. The dependence of the writing process on drain and gate bias conditions was also investigated.**

***Index Terms*—1T-SRAM; Bi-stability; Dynamic Simulation; TCAD; Impact-ionization**

I. Introduction

6T-SRAM is a key component in microprocessors and system on chip (SoC) applications as embedded memory occupies a significant fraction of the chip area. The SRAM real estate is even larger in Artificial Intelligence (AI) chips. However, the 6T-SRAM cell scaling has become increasingly challenging due to the increasing stability and leakage current problems. A novel bi-stable, one transistor (1T) SRAM structure has been previously disclosed [1], which has the potential to dramatically reduce the SRAM real estate and to revolutionize the in-memory AI computing.

In this paper for the first time we present dynamic (time dependent) simulations of the write operation of the 1T SRAM cell based on 28nm planar CMOS technology.

II. Methodology

The process simulation for the 1T SRAM cell was carried using Sentaurus Process [2]. The corresponding simulation domain is illustrated in Fig. 1. In order to create the SRAM cell in a standard 28nm CMOS process flow of the *n*-channel MOSFET a heavily doped *n*-type 'boost' region is created by ion implantation beneath the source/drain, having peak concentration located deep in the substrate. This creates a floating *p*-type charge storage region isolated by the shallow trench isolations (STIs) on the sides of the transistor and by a *p*-*n* junction from below. The Drain and Gate terminals of the MOSFET are used for reading and writing into the cell and are connected to the Bit Line and Word Line, respectively, while the vertical *npn* transistor formed by the Drain/Source (Emitter), *p*-well (Base) and Boost (Collector) regions plays the key role in holding the data.

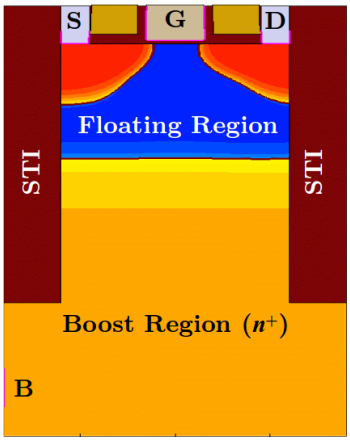

Fig. 1. 1T SRAM simulation domain.

The simulated current-voltage characteristics of the MOSFET at low and high drain bias in steady state conditions are calibrated to fit the experimentally measured data, as illustrated in Fig. 2. The important physical models used in the simulation are: Masetti model for doping dependence and Lombardi and Caughey-Thomas models for field dependence of mobility, doping dependent Shockley-Read-Hall (SRH) recombination model, and the Schenk model for band-to-band tunneling.

Further, impact ionization plays a critical role in the operation of the of 1T SRAM cell. After a number of test run simulations using available models, we found that the Okuto model [3], is the most suitable to compute the ionization coefficient, reproducing the three experimentally observed dips [1], [4] in the base (the floating *p*-well region) current versus base-emitter voltage (*p*-well potential relative to the source) *i.e.* the I_p-V_p characteristics of the vertical *npn* bipolar transistor.

In Fig. 3, we show the impact of different boost voltages on the I_p-V_p characteristics at zero Gate and Drain bias. Here the dips in the I_p-V_p characteristic represent zero net *p*-well current due to reversal of the base current at specific *p*-well potentials (V_p). This mechanism has been studied earlier in conventional bipolar junction transistors and explained in context of the 1T SRAM cell in [1]. In essence, the electrons emitted from the Source arrive at the *p*-well/Boost junction and

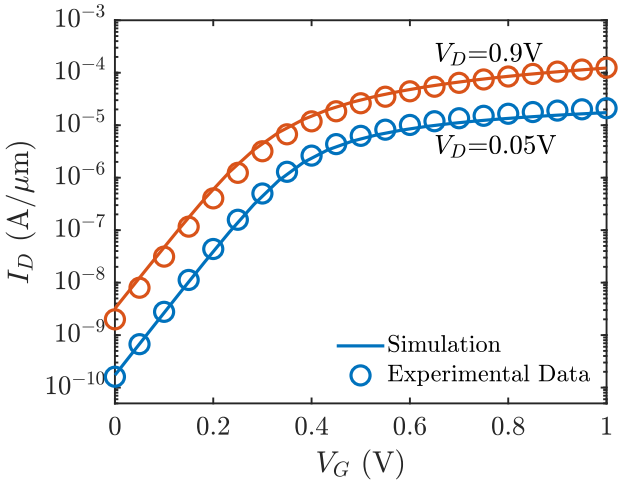

Fig. 2. Calibration of the MOSFET transfer characteristics.

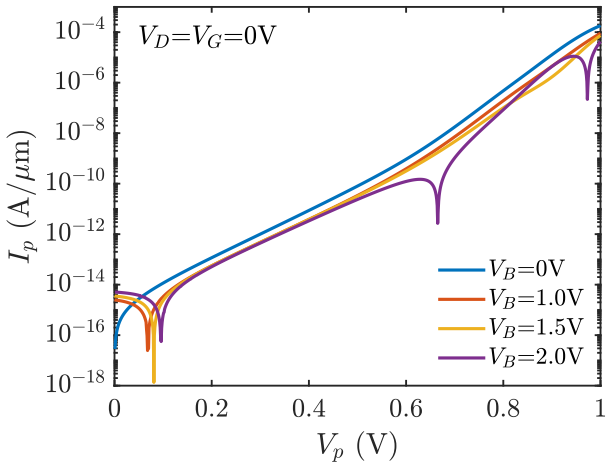

Fig. 3. Base current Vs base-emitter voltage (I_p-V_p) characteristics of the vertical bipolar transistor at different boost voltages (V_B) with V_G=V_D=0V. Here the subscript 'p' refers to the floating p-well region.

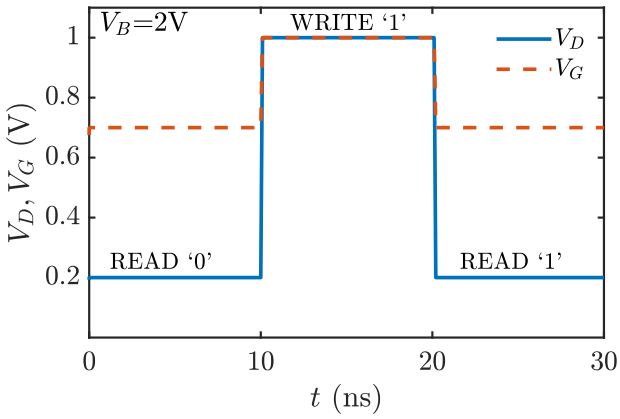

Fig. 4. V_G and V_D waveform for switching sequence comprised of READ '0'→ WRITE '1' → READ '1'. The boost voltage is constant throughout at V_B=2V.

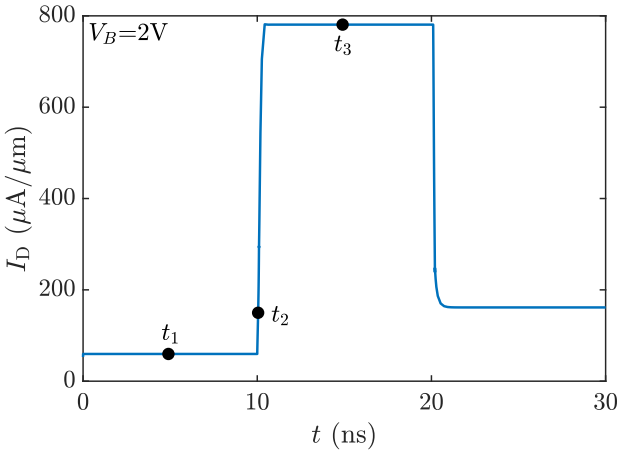

Fig. 5. Switching profile of the 1T-SRAM cell consisting of the READ '0', WRITE '1', and READ '1' operations.

the Drain regions and if the electric field at these junctions are sufficiently high, the electrons will cause impact ionization. The resulting excess holes flow to the base terminal (the p-well region). This reduces the net p-well current, and hence depending on the bias conditions, it can be negative or positive. This gives rise to two stable states: state '0' at low V_p and state '1' at high V_p, with an intermediate metastable state, and this is the origin of the memory effect. Depending on the applied Drain and Gate voltages (V_D and V_G respectively), the cell will be latched to one of the stable states. At low boost voltage, the electric field at the p-well/boost junction is not strong enough for avalanche multiplication and hence we do not observe this bi-stable phenomenon.

III. Results and Discussion

The Write '1' operation of the 1T SRAM cell is associated with the charging of the floating p-well. The dynamic (time dependent) simulation of this process involves fine balance between carrier generation and carrier recombination. In this section, we present simulation results and discussion on the write '1' operation in the 1T-SRAM.

The Drain and Gate terminal input waveform corresponding to read '0', write '1', and read '1' operations is shown in Fig. 4. The nominal Drain and Gate voltages used for writing '1' are 1V each while for reading, the voltages used are 0.2V and 0.7V, respectively. All the ramp times for the transients were 100 ps. The impact ionization rate is calibrated by tuning the 'b' parameter of the Okuto model in order to achieve desired operation.

Fig. 5 shows the cell switching process in terms of the Drain terminal current. The drain current is assessed for reading the cell state. We can see that the read '1' current is higher than the read '0' current. The stability of state '1' over time is achieved without refresh operation, indicating the bi-stability of the 1T-SRAM cell.

In order to understand the switching dynamics, in Fig. 6 we present the two-dimensional distributions of the electron current density, hole current density, potential, and impact ionization at three instants of time during the dynamic simulation:

before the start of the writing process (t_1= 4.9ns), during the application of the write signals (t_2=10.05ns) and after completion of the write '1' process (t_3=14.9ns). These three times are marked in Fig. 5. The MOSFET current increases as the Drain and Gate bias increase. In addition, as a result of impact ionization at the *p*-well/Boost junction and drain end of the channel there are excess holes in the floating *p*-well which is continuously charged during the switching period resulting in the increase of the drain current. Subsequently, a positive feedback mechanism kicks off between increased impact ionization and increased *p*-well/Source junction forward bias which results in sharp switching of the terminal currents.

To examine the effect of impact ionization on the writing process, we performed simulations with varying values of the parameter 'b' in the Okuto impact ionization model. The impact ionization coefficient in this model is given by [3]:

$$\alpha\left(\xi\left(x\right)\right) = a\xi\left(x\right)^{n}\exp\left[-\left(b/\xi\left(x\right)\right)^{m}\right] \qquad (1)$$

where $\alpha\left(\xi\right)$ is the position dependent ionization coefficient, ξ is electric field, n and m are fitting parameters, a and b are linear functions of the lattice temperature. It can be readily seen from (1) that the ionization coefficient decreases with increasing values of b. Accordingly, we can observe from Fig. 7 that a very low b value leads to high impact ionization and the cell cannot sustain '0' state. On the other hand, if a very high value of b is used, the amount of impact ionization is not sufficient to achieve the required level of majority carriers in the *p*-well and the associated positive feedback action is not strong enough to execute stable writing. The dashed waveform corresponds to the b value used in this work.

Next, we have investigated the impact of recombination on the cell switching by changing the carrier lifetimes. Full switching simulations were performed with different electron and hole recombination rates. As can be seen from the results illustrated in Fig. 8, the switching process is greatly affected by the electron and hole lifetimes. We have considered a range of electron and hole lifetimes that are different from the default values for silicon for the purpose of investigating the bi-stability and write operation mechanism. Firstly, increased electron lifetime with hole lifetime set close to the default value leads to an undesirable increase in the currents right at the start of the read '0' period, implying that the '0' state is not stable. In other cases where the lifetimes of both the carriers are reduced, the initial currents remain low, and read '0' is executed properly. However, the write '1' and read '1' currents are significantly lower due the increased recombination rates leading to write failure for extremely short lifetimes. This demonstrates the importance of carrier lifetimes in ensuring bi-stability of the 1-transistor memory cell.

Finally, we simulated the write '1' process with different drain and gate voltages used for writing ($V_{D,W}$, $V_{G,W}$ respectively). As shown in Fig. 9, the write '1' current decreases with reduction in $V_{D,W}$ and $V_{G,W}$. Regardless, successful write '1' operation can be performed even at $V_{D,W}$ = $V_{G,W}$ = 0.6V. This shows that the 1T-SRAM cell is viable at scaled supply

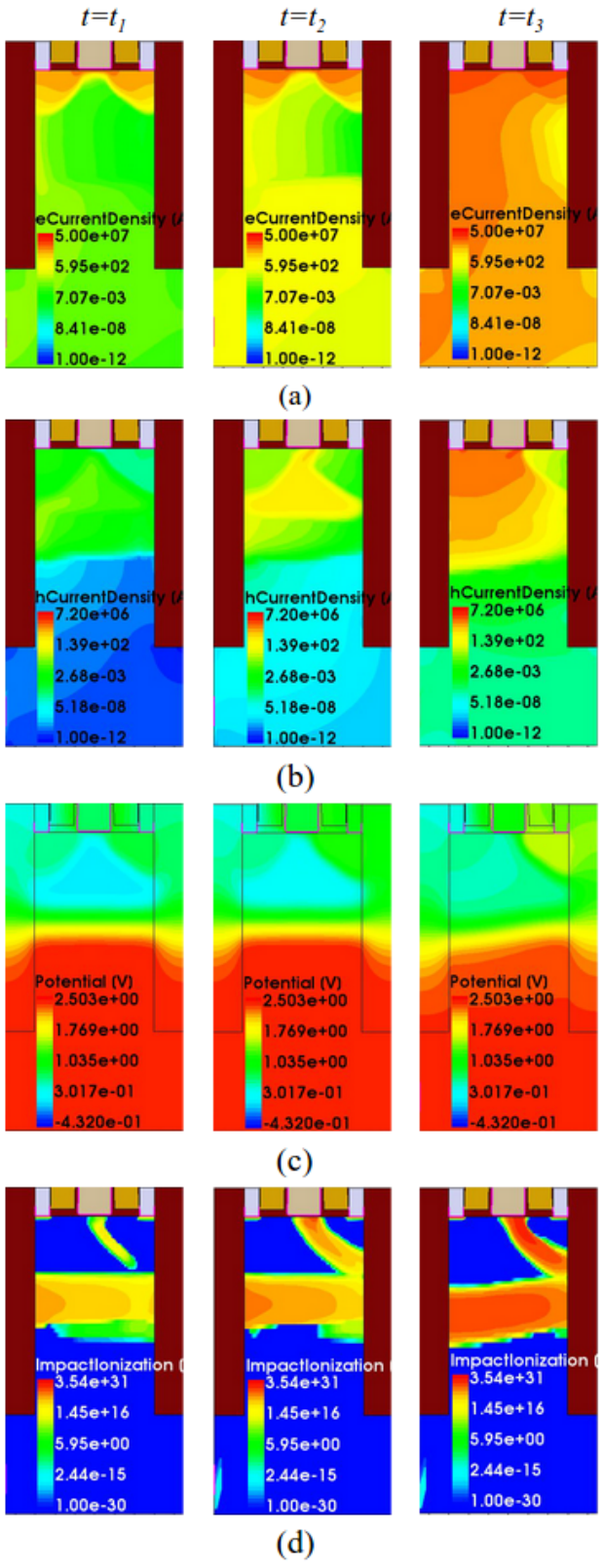

Fig. 6. Temporal snapshots of 2D distributions of (a) electron current density (b) hole current density (c) Electrostatic potential and (d) Impact ionization during the switching. V_B=2V. The three time instants (t_1, t_2, t_3) are marked in Fig. 5.

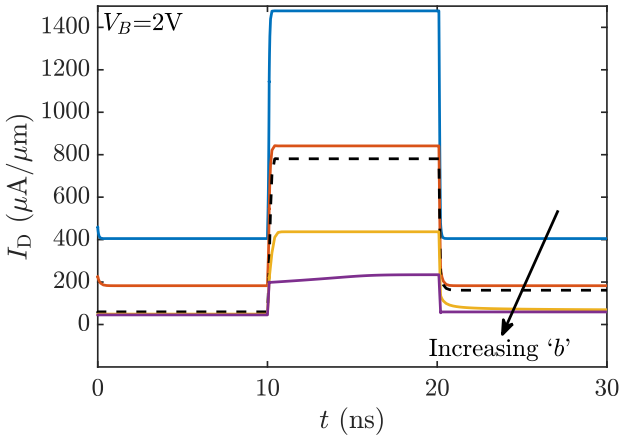

Fig. 7. Impact of the Okuto model parameter 'b' on the switching characteristics.

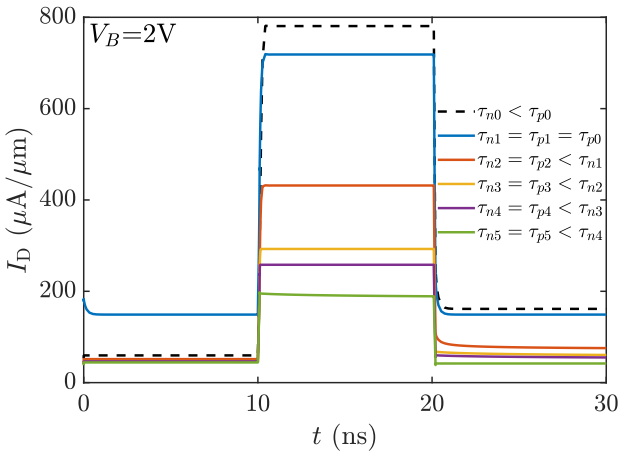

Fig. 8. Time dependent simulations for different carrier lifetimes at V_B=2V. The dashed waveform corresponds to the carrier lifetimes used in this work.

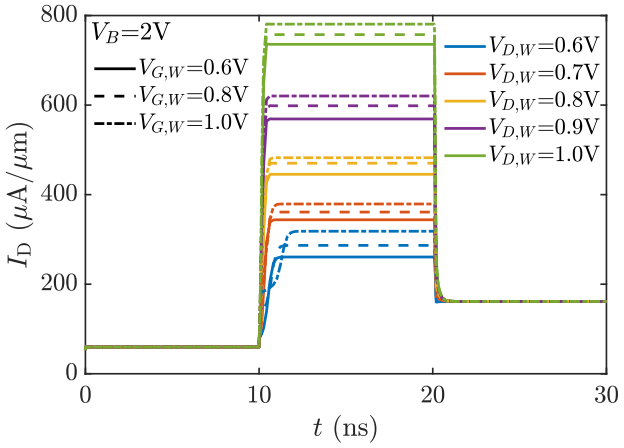

Fig. 9. Switching characteristics at V_B=2V for different values of drain and gate voltages used for writing.

voltages. The read '1' current is not affected by the amplitude of the write pulse.

IV. Conclusion

We have simulated and investigated the time dependent switching characteristics of the bi-stable 1T SRAM cell and have clarified the switching mechanism and the impact of generation and recombination phenomena in the switching process. We also demonstrated that writing '1' can be executed successfully at supply voltages as low as 0.6V.

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