Compact modeling of gate leakage phenomenon in GaN HEMTs

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***Abstract*—This paper implements a physically derived compact model of current conduction and gate leakage in AlGaN/GaN high-electron mobility transistors (HEMTs). The drain-source current conduction through the device is described using the surface potential based virtual-source model applicable for scaled gate length devices. The gate leakage model includes contributions from thermal emission (TE), trap-assisted tunneling (TAT), Poole Frenkel (PF) emission, and Fowler-Nordheim (FN) tunneling. The full I-V model is applied to fabricated AlGaN/GaN HEMTs with SiN passivation and excellent agreement of the model against measured data is demonstrated over a broad bias and temperature range from 298 K to 573 K.**

***Index Terms*—Compact model, GaN HEMTs, Gate leakage, High temperature operation**

I. Introduction

AlGaN/GaN-based high electron mobility transistors (HEMTs) are an excellent candidate to realize high-power and high-frequency electronic devices that could also operate in extreme environment. In particular, AlGaN/GaN HEMTs can support a high concentration of the two-dimensional electron gas (2DEG) at the interface due to polarization engineering, thus obviating the need of additional impurity doping [1]. With a high 2DEG mobility (> 1250 cm^2/Vs), high maximum carrier drift velocity ($\sim 2.5 \times 10^7$ cm/s), and high breakdown field strength (330 MV/cm), AlGaN/GaN HEMTs surpass their III-V counterparts in terms of achieving the desired Johnson figure of merit for microwave and millimeter wave applications [2]. However, despite these advantages, the excessive gate leakage current is a limiting factor in these devices, especially when the devices are subject to high-field and high-temperature operating conditions [3]. Incorporating gate leakage into compact device models is therefore important to accurately assess the technology-device-circuit interaction and further use this assessment to fine-tune the device technology to achieve lower leakage.

When the device is forward biased, the dominant leakage current is due to thermal emission (TE), which increases exponentially with the bias across the gate Schottky contact. In the case of GaN HEMTs in which localized trap centers are often found in the AlGaN layer, the trap-assisted tunneling (TAT) current also becomes important to consider in the forward biased regime of the gate Schottky contact. On the other hand, the leakage through the gate contact is due to the Poole-Frenkel (PF) emission and the Fowler-Nordheim (FN) tunneling when the contact is reverse biased.

While prior works have focused on the physics of gate leakage in AlGaN/GaN HEMTs, there are limited reports of modeling gate leakage within a compact device model that would facilitate accurate circuit simulations. In [3], gate leakage is computed without including the effect of the drain bias and, therefore, is not applicable over a broad bias range. In [4], gate leakage in GaN HEMTs was studied for temperature less than 320 K. However, during nominal device operation in RF circuits, the channel temperature of GaN HEMTs could exceed 450K. Reference [5] uses a simplified Schottky-diode theory to represent the gate-source and gate-drain leakage currents. In [6], the gate leakage current due to the existence of surface traps is reported to be the primary mechanism and is modeled physically by solving the Poisson's and current density equations self-consistently. However, the validity of these models over broad electrical bias and temperature range in short-channel HEMTs has not been established. In this work, a physically motivated model for gate leakage in sub-500 nm gate-length GaN HEMTs is developed. The gate leakage current and the drain-source current are computed self-consistently using the surface-potential-based virtual-source model developed by the co-authors Li and Rakheja. Moreover, the compact model comprehends the nonlinear effects pertinent to GaN technology including nonlinear access region resistances and self-heating under high current density. The model validity is demonstrated by applying it to measured device data over broad bias and temperature range between 298 K to 573 K.

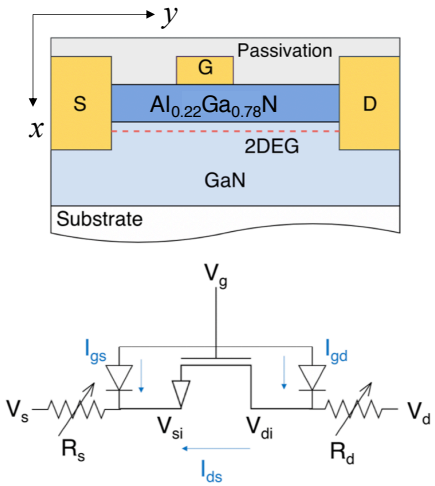

Fig. 1. Illustration of the cross-section of a prototypical AlGaN-GaN HEMT. Below is the equivalent circuit diagram of the GaN HEMT. The gate-source leakage is $I_{\rm gs}$, gate-drain leakage is $I_{\rm gd}$, and nonlinear source/drain resistances are represented as R_s and R_d. The voltages at the intrinsic source and drain nodes are represented as $V_{\rm si}$ and $V_{\rm di}$, respectively. The gate length of the fabricated devuce is 400 nm, and its width is 50 µm. The device is built on SiC substrate.

II. Model Description

A prototypical AlGaN/GaN HEMT device structure and its equivalent circuit model are shown in Fig. 1. The Schottky diodes between the gate metal and the source/drain are shown in the equivalent circuit model. This circuit also indicates the non-linear source and drain access-region resistances, R_s and R_d, respectively. The intrinsic voltage at the source and drain nodes is given as $V_{\rm si}$ and $V_{\rm di}$, respectively. Since the voltage drop across the access regions depends on the drain-source current $I_{\rm ds}$, the intrinsic voltage drops from the gate-to-source, $V_{\rm gsi}$, and the gate-to-drain, $V_{\rm dsi}$, are first obtained from the core drain-source I-V model. These voltage drops are then used as inputs to compute the gate leakage self-consistently with $I_{\rm ds}$. The core drain-source I-V model is based on the virtual-source (VS) approach to current conduction, where in the charges and the velocity of charges at VS are obtained in terms of the Landauer's channel transmission coefficient. The channel transmission is formulated differently for drift-diffusive and quasi-ballistic devices as discussed in [7], [8]. Further, we consider that only the first quantized energy sub-band in the channel is occupied. We have verified the validity of this assumption by conducting coupled Schrödinger-Poisson simulations for the devices examined here. Additional details regarding the core model formulation can be found in [8].

Figure 2 shows the various components of gate leakage in both reverse and forward bias modes of the gate Schottky contact. The TE current component at the gate-source and the gate-drain Schottky contacts in the forward biased mode is given as

$$I^{\rm TE}_{\rm g(s,d)} = I_{\rm TE0} T^2 \exp\frac{-\phi_{\rm TE}}{\phi_t}\left[\exp\frac{V_{\rm g(si,di)}}{\eta_{\rm TE}\phi_t} - 1\right], \quad (1)$$

where $I_{\rm TE0}$ is the product of the Richardson's constant and the contact area $A_{\rm con}$, T is the operating temperature, $\phi_{\rm TE}$ is the Schottky barrier height, $\eta_{\rm TE}$ is the non-ideality parameter of the junction, and $\phi_t = k_B T/q$ (k_B is Boltzmann constant) is the thermal voltage. The TAT current is modeled similarly as (1) but with different values of the non-ideality parameter ($\eta_{\rm TAT}$), Schottky barrier height ($\phi_{\rm TAT}$), and the Richardson's constant ($I_{\rm TAT}$).

Due to the spatial inhomogeneities at the metal-semiconductor interface, which lead to a spatial distribution of the Schottky barriers within the interface plane [9], the Schottky barrier height (ϕ_B) is expressed as

$$\phi_B = \overline{\phi_B} - \frac{\sigma_s^2}{2k_BT/q}, \quad (2)$$

where $\overline{\phi_B}$ is the fundamental or mean Schottky barrier, while σ_s is the standard deviation. Assuming that $\overline{\phi_B}$ is temperature independent and σ_s is either temperature-independent or varies linearly with temperature, (2) shows that ϕ_B increases with an increase in temperature. Experimental data analyzed in this work and others [10] confirm this temperature dependency of ϕ_B. Accordingly, we model $\phi_{\rm TE/TAT}$ as

$$\phi_{\rm TE/TAT} = \phi_{\rm TE/TAT,300} + \gamma_{\rm TE/TAT}(T - 300), \quad (3)$$

where $\phi_{\rm TE/TAT,300}$ is the Schottky barrier height at 300 K, and $\gamma_{\rm TE/TAT}$ captures the linear temperature dependency of the Schottky barrier height.

Under the statistical model of the Schottky contacts, the non-ideality parameter results from the deformation of the spatial barrier distribution when a bias is applied. We restrict ourselves to the case that the non-ideality of a given process is bias independent. This assumption is justified based on the experimental data of AlGaN/GaN HEMTs, as well as other Schottky contacts such as PtSi/Si measured in previous works. For such contacts, the temperature-dependent non-ideality is modeled as

$$\eta = \frac{1}{1 - \rho_2 + \rho_3/(2k_BT/q)}, \quad (4)$$

where ρ_2 (ρ_3) quantifies the bias-dependence of $\overline{\phi_B}$ and σ_s^2. When $-\rho_2 + \rho_3/(2k_BT/q) \ll 1$ and $\rho_2 \ll \rho_3/(2k_BT/q) \ll 1$, we can simplify the non-ideality as

$$\eta = 1 - \frac{\rho_3}{2k_BT/q}. \quad (5)$$

For the purpose of compact device modeling, we represent (5) for TE and TAT processes as

$$\eta_{\rm TE/TAT} = \eta_{0({\rm TE/TAT})} + \kappa_{\eta({\rm TE/TAT})}\left[\frac{1}{T_0} - \frac{1}{T}\right], \quad (6)$$

where $\eta_{0({\rm TE/TAT})}$ is the non-ideality for TE and TAT processes at $T_0 = 300$ K, while $\kappa_{\eta({\rm TE/TAT})}$ is the temperature coefficient of the non-ideality.

The FN tunneling which dominates gate leakage in reverse - biased condition for a given electric field $\mathcal{E}$ across the insulator (AlGaN layer) is given as [11]

$$I^{\rm FN}_{\rm g(s,d)} = A_{\rm con} J_{\rm FN0}(T)\mathcal{E}^2 \exp\left(-\frac{B(T)}{\mathcal{E}}\right),$$
$$\mathcal{E} = \frac{V_{\rm gsi} - \psi_s}{t_{\rm ins}}, \quad (7)$$

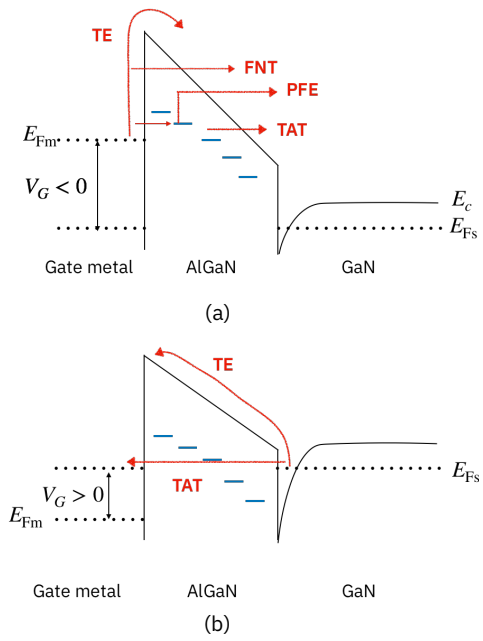

Fig. 2. Illustration of gate leakage mechanisms when the gate-source Schottky contact is (a) reverse biased ($V_G < 0$) and (b) forward biased ($V_G > 0$). TE: thermionic emission, PFE: Poole-Frenkel emission; TAT: trap-assisted tunneling; FNT: Fowler Nordheim tunneling tunneling. $E_{\rm fm}$ and $E_{\rm fs}$ denote the Fermi level in the metal and GaN channel, respectively. E_c denotes the bottom of the conduction band.

where the pre-factor $J_{\rm FN0}(T)$ and the coefficient $B(T)$ are determined from examining the measured gate leakage data. To evaluate the electric field, we need the information on the surface potential, ψ_s, at VS, which is readily provided by the core drain-source I-V model.

From an analysis of experimental data, we find that the temperature dependence of $J_{\rm FN0}(T)$ can be modeled as

$$J_{\rm FN0} = J_{\rm FN00} + \gamma_{\rm FN}(T - T_0)^2. \tag{8}$$

where $I_{\rm FN00}$ is evaluated at $T_0 = 300$ K, while $\gamma_{\rm FN}$ is the second-order temperature sensitivity coefficient of $J_{\rm FN0}$. The exponent $B(T) \propto \sqrt{m_{\rm eff,t}\phi_1}$ depends on the tunneling mass of electrons through the AlGaN layer ($m_{\rm eff,t}$) and the barrier height for tunneling (ϕ_1). Previous works have shown that the barrier height for tunneling in AlGaN/GaN HEMTs reduces with an increase in temperature, implying that $B(T)$ reduces with temperature. Similar temperature-dependent behavior is also observed in our samples (see Sec. III). Hence, we model $B(T)$ as

$$B(T) = B_0 - \gamma_B(T - T_0), \tag{9}$$

where B_0 is the value of $B(T)$ at $T = T_0 = 300$ K, and γ_B measures its temperature sensitivity.

The PF emission gate leakage is due to trap-assisted hopping transport, where the traps located closer to the bottom of the conduction band are involved [12]. In its simplified form, the PF emission gate leakage current is given as

$$I_{\rm PF} = A_{\rm con} C \mathcal{E} \exp\left[\frac{-q(\phi_{\rm PF} - \sqrt{\beta_{\rm PF}\mathcal{E}})}{k_B T}\right], \tag{10}$$

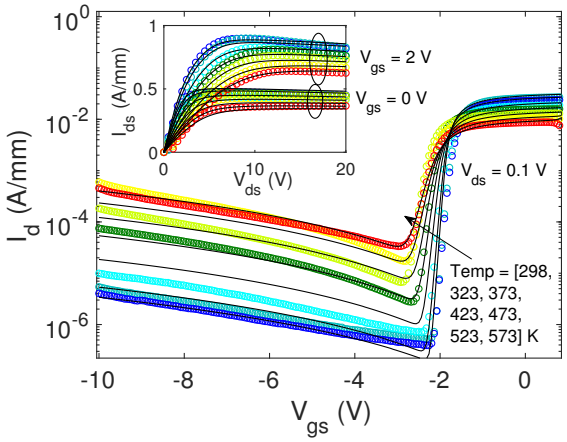

Fig. 3. Validation of the core static I-V model against measured data. Main plot shows transfer curves, while output curves are shown in the inset. Symbols are measured data, while model fits are shown in solid lines.

where C is a constant of proportionality, $\phi_{\rm PF}$ is the emission barrier height with reference to the trap level of the electron, and $\beta_{\rm PF} = q/\pi\epsilon_{\rm ins}$.

III. Results

The cross-section of the fabricated device is shown in Fig. 1. The device consists of a 20-nm thick $Al_{0.22}Ga_{0.78}N$ on top of 900-nm unintentionally doped GaN channel followed by 300-nm GaN buffer. We first match the measured I_d versus $V_{\rm ds}$ and $V_{\rm gs}$ using our core static I-V model. Once the core model parameters are determined, we calibrate the gate leakage model against measurements. Figure 3 shows the results of output and transfer curves of the HEMT obtained from measurements and from model-generated results. We can see that the model does an excellent job to capture the full I-V plane of the device over a broad range of temperature from 298 K to 573 K.

Figure 4 shows a plot of $\ln(J_g^{\rm meas}/\mathcal{E}^2)$ versus $1/\mathcal{E}$ in the reverse-biased mode. Here, $J_g^{\rm meas}$ is the measured gate leakage current density. From the slope of the plot and the y-axis intercept at different temperatures, we can extract $B(T)$ and $J_{\rm FN0}(T)$, respectively (see inset of Fig. 4).

To confirm that the PF emission is insignificant in our devices, in Fig. 5, we show $\ln(J_g^{\rm meas}/\mathcal{E})$ versus $\sqrt{\mathcal{E}}$. The slope of the straight line in this plot is $q\sqrt{\beta_{\rm PF}}/k_BT$. However, the extracted value of $\beta_{\rm PF}$ leads to a significantly higher value of $\epsilon_{\rm ins}$, which for the devices under examination is physically unfeasible. As we discuss later, the gate leakage current from measurements can indeed be fully explained by neglecting contribution from PF emission.

Figure 6 shows the measured gate leakage data versus gate bias at 100 mV drain-to-source bias. We see the model-generated results match the measurements quite well over a broad range of bias and temperature. The model parameters used to obtain the model fits are listed in Table I.

IV. Summary

In this work, a physically motivated compact model is proposed for gate leakage current in GaN HEMTs. The gate

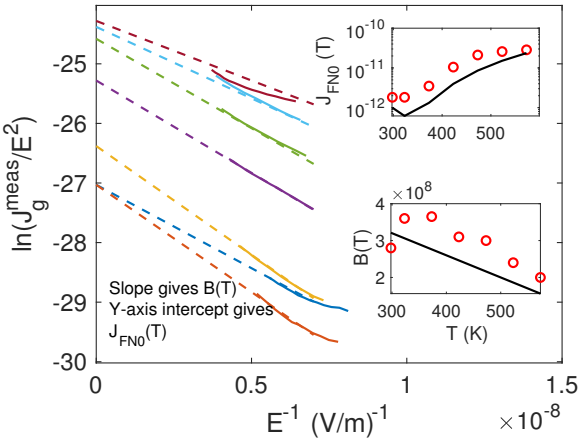

Fig. 4. Main plot shows data on $\ln(J_g^{\rm mes}/\mathcal{E}^2)$ versus $\mathcal{E}^{-1}$ from measurements. Assuming solid line fit to the experimental data allows us to extract temperature-dependent FN tunneling parameters as shown in inset. Solid lines show model fits while symbols are extracted from measurements.

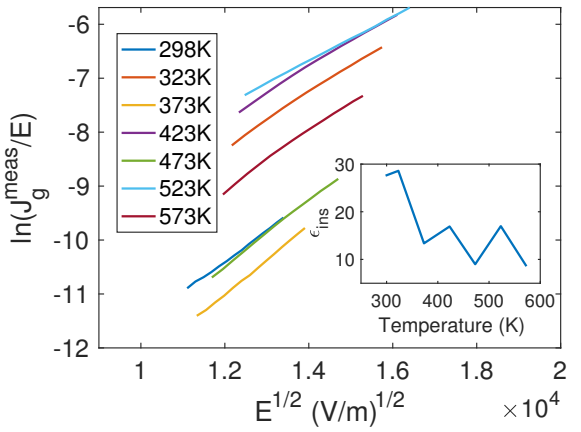

Fig. 5. Assuming PF emission model, the permittivity of the insulator layer is extracted as a function of temperature. As shown in inset, only at very high temperatures the permittivity approaches physically meaningful values, indicating that for our samples PF emission is not dominant.

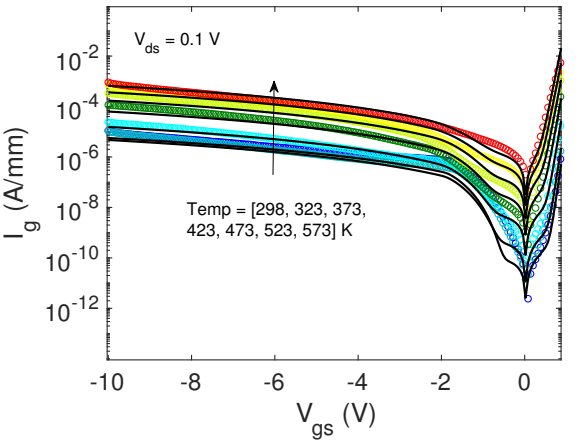

Fig. 6. Validation of the gate leakage model against measured data for broad temperature range. Symbols are measured data points, while solid line corresponds to model fit.

TABLE I
MODEL PARAMETERS USED FOR VALIDATING GATE-LEAKAGE MEASUREMENTS.

Parameter	**Value**
Key core static I-V model parameters	
Device width, W	50 µm
Gate length, L_G	400 nm
Source access region length, $L_{\rm acc,s}$	0.6 µm
Source access region length, $L_{\rm acc,d}$	3.3 µm
Effective mobility, $\mu_{\rm eff}$	1275 cm^2/Vs
Thermal resistance, $R_{\rm th}$	120 K/W
Contact resistance, R_c	3×10^{-4} Ω-m
Non-ideality parameter for the channel, n_0	1.4
TE model parameters	
Schottky barrier height for TE at 300 K, $\phi_{\rm TE,300\ K}$	0.67 V
Temperature sensitivity of TE Schottky barrier height, $\gamma_{\rm TE}$	0.0007 V/K
Non-ideality parameter for TE at 300 K, $\eta_{0,\rm TE}$	15
Temperature sensitivity of TE non-ideality, $\kappa_{\eta,\rm TE}$	100 K
TAT model parameters	
Schottky barrier height for TAT at 300 K, $\phi_{\rm TAT,300\ K}$	1 V
Temperature sensitivity of TE Schottky barrier height, $\gamma_{\rm TE}$	0.00005 V/K
Non-ideality parameter for TAT at 300 K, $\eta_{0,\rm TAT}$	1.5
Temperature sensitivity of TAT non-ideality, $\kappa_{\eta,\rm TAT}$	100 K
FN tunneling model parameters	
Pre-factor in FN tunneling current at 300 K, $J_{\rm FN00}$	6×10^{-13} A/V^2
Temperature sensitivity of FN tunneling pre-factor, $\gamma_{\rm FN}$	3×10^{-16} A/V^{2}K^2
FN tunneling exponent factor at 300 K, B_0	2.3×10^{8} V/m
Temperature sensivity of FN tunneling exponent factor, γ_B	3.4×10^{5} V/mK

leakage model is coupled to our previously developed core static I-V model, a surface-potential based model that can be adapted to handle transport physics of both drift-diffusive with velocity saturation and quasi-ballistic devices. Our gate leakage model is applied to a 400-nm $Al_{0.22}Ga_{0.78}N$/GaN HEMTs from 298 K to 573 K and excellent match of the model against measured data is demonstrated. Our future work will include gate leakage modeling in shorter gate length devices as well as in different epitaxial heterostructures.

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