# Compact Modeling Perspetive – Bridge to Industrial Applications

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***Abstract*—This paper summarizes briefly compact-model development history, which is characterized by the evolution into the role as a bridge between devices and circuits. It is demonstrated that the task of predicting circuitry performance accurately has been realized by considering the microscopic features of the device phenomena in the compact model, which had been previously treated only macroscopically.**

***Keywords—compact modeling, MOSFET, carrier dynamics, Poisson's equation, microscopic phenomena, circuit performance***

## I. Introduction

Diversity is growing in the world with respect to many aspects such as the internet of things (IoT). This became possible mostly due to the rapid technology development enabling and supporting many expectations growing in the society. It is clear that the semiconductor community has been playing an important role in this context. Owing to the difficulty of real-fabrication experiments with advanced technologies, simulation-based experiments have been intensively investigated to speed-up the achievement of targeted goals. The focus of this review is given on the compact-modeling technique, required for practical connection from new device developments to the key circuits of the final product. It is shown that a lot about the individual device characteristics can be further learned through the analysis of circuit performances in addition to the conventional device performances. Thus it can be said that compact models play the role of a bridge connecting devices and circuits. Due to such an important role, compact modeling is shifting from the simple threshold-voltage-based modeling approach, which has been studied for long time by the circuit simulation community, to modeling based on the potential distribution [1]. Progress achieved by this shift is summarized. Further, the compact-modeling improvements, following the evolution of applications, are overviewed and future aspects are also discussed.

## II. Compact Modeling and Simulation Results

### A. Compact Modeling

Compact models have been focusing on describing observed phenomena only on the basis of their essential origins in analytical forms for accurate prediction of circuit performances with less simulation time. The first compact model for circuit simulation was developed by Meyer in 1971, describing the MOSFET features with an equivalent circuit consisting of a current source, capacitances and resistors as shown in Fig. 1 [2]. The applied current equation is based on the simple drift approximation, which describes *I-V* characteristics just as a function of applied biases with the threshold voltage $V_{th}$ [3]. 2D-device simulation taught us that the saturation behavior of MOSFET is due to the loss of the gate control together with the increase of carrier scattering. These MOSFET features have been compact modeled afterwards. Increased needs for RF circuits and reduction of the non-linearity of device performances, causing cross talks in the communication systems, became serious problems to be solved. It was found that the carrier scatterings due to the field induced in the system are the main origin of the non-linearity, as demonstrated in Fig. 2 [4]. Thus the task for compact modeling entered into a new era, namely compact modeling has to consider the microscopic features of the carrier dynamics, which were modeled previously only phenomenologically. At the same time accurate prediction became an important task to complement actual measurements. Therefore, potential-based descriptions, capturing the origin of the device performances, became common and replaced the $V_{th}$-based modeling approach.

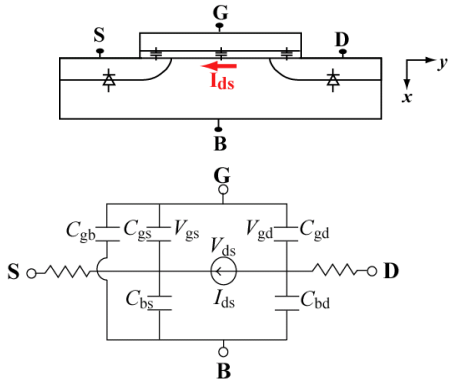


Fig. 1. Equivalent circuit (lower) developed by Meyer for describing a MOSFET (upper) [2].

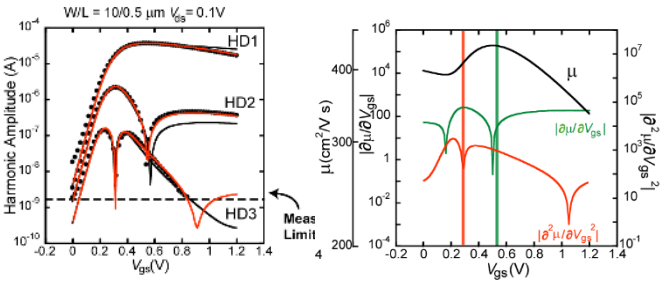


Fig. 2. Measured harmonic amplitudes (a) in comparison to the carrier mobility derivatives (b), showing that the main origin of the harmonics is the non-linearity of the carrier mobility.

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### B. *Relationship between Circuit and Device Performances*

As depiced in Fig. 1, a simple MOSFET model consists of a current source, capacitances and resistances. Generally circuits include external elements such as loading capacitances and resistances to realize requested circuit performances. Fig. 3 shows a simple circuit applied for device-switching-performance measurements [5]. External elements form a low-path filter, which determines switching performance together with the internal device properties, as demonstrated in Fig. 4, where analytical cut-off-frequency descriptions are applied. Internal device properties dominate the switching performance with increased frequency. Therefore, it can be said that the device characteristics determine the RF circuit performances. The origin for this limitation is the carrier-transit delay, causing switching delay as depicted in Fig. 5. Thus the compact modeling has to be done by considering the transit delay explicitly [4].

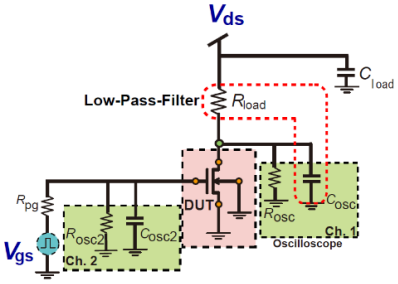


Fig. 3. A circuit applied for transient measurement.

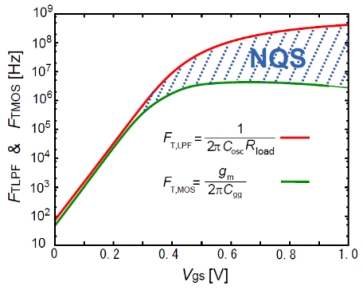


Fig. 4. The low-pass filter frequency $F_{T,LPF}$ and that of a MOSFET $F_{T,MOS}$, used as the DUT shown in Fig. 3, as a function of the input voltage $V_{gs}$.

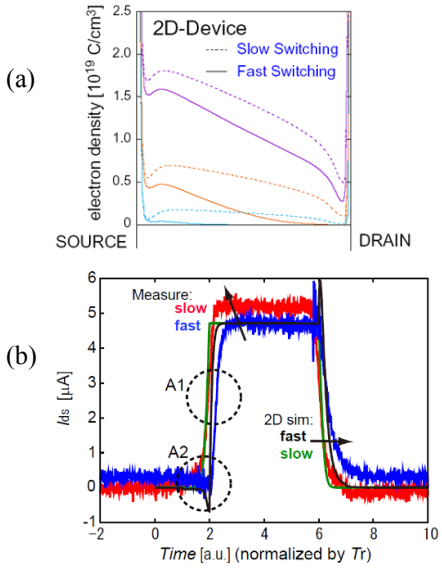


Fig. 5. (a) 2D-device simulation results of the electron-density distribution along the channel during switching-on condition, (b) measured transient currents. Comparisons are shown for two different switching speeds.

## III. Future Aspects

The device development is approaching size limits, causing non-ideal device performances such as increased short-channel effects as well as fabrication variations. Nevertheless, devices for ultra-low power applications are one of the forces driving the development forward. Spintronics is an example. Beyond the potential-distribution modeling approach, compact modeling requires to understand the origin of the microscopic features in addition to averaged macroscopic features. Such investigations might bring an idea whether a new device configuration leads to any advantage over the present status.

### A. *Compact Modeling for Individual Carrier Dynamics*

One important circuit-performance degradation is caused by non-controllable carrier dynamics, which are observed as noise. To predict the noise characteristics accurately, it has been demonstrated that the carrier dynamics within the MOSFET channel is important [6]. Fig. 6 shows 1/*f* noise measurements for different devices and channel lengths. By approximating that trap sites are mostly located at the Fermi energy and the trap density is homogeneously distributed within the oxide with the attenuation coefficient, the 1/*f* feature can be analytically derived. Previously, modeling was done for the 1/*f* characteristics with averaged measurements (see Fig. 6a), to predict circuit performance accurately. However, Fig. 6b shows that averaging might not results in a 1/*f* characteristics for advanced technologies. The reason for deviating from the 1/*f* characteristics is explained by several specific trap states, which dominate the noise characteristics as depicted in Fig. 7a. An analytical description has been developed by considering the carrier-density distribution within the oxide explicitly (see Fig. 7b) [7].

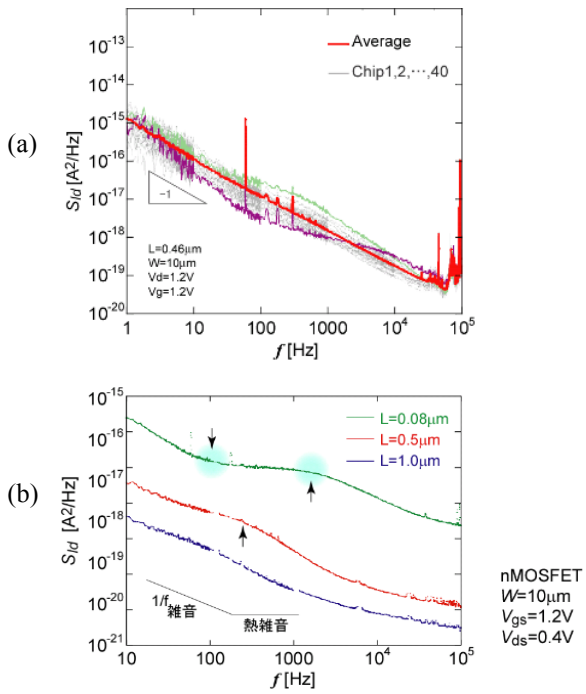


Figure 6. (a) Measured noise characteristics of 40 relatively long-channel MOSFETs and their average showing the 1/f noise characteristics. (b) Measured noise characteristics for different channel lengths.

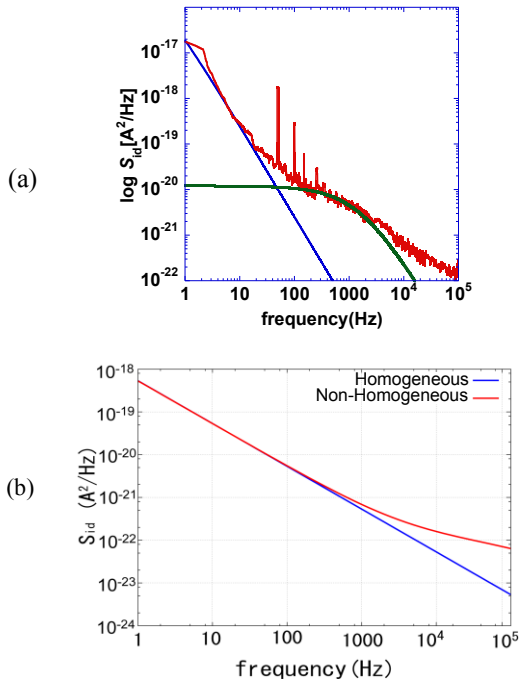


Figure 7. (a) Measured non 1/f noise intensity is attributed to the specific Lorentzian noise, whereas the tail for high frequency is explained by the non-homogeneous trap density within the insulator as shown in (b) [7].

### *B. Circuit Aging Prediction*

Since the signals propagating within circuits are getting weaker and weaker due to the requirements for low-voltage application with extremely scaled-down device size, risks of circuit malfunction are increasing. Carrier trapping is one of the reasons for the malfunction. The trap-density increase in devices is exactly the origin of the circuit aging. Therefore, modeling the trap-density increase during circuit operation is the most essential task to be done. It is known that the carrier trapping is caused by hot carriers, where carriers must have sufficient energy to be trapped. The main difficulty in investigating circuitry aging is that the predicted trap density can never be verified experimentally. The best way to overcome this problem is to develop a sufficiently reliable methodology for the prediction.

The reliability of the simulation results is usually confirmed with accurate reproduction of DC measurements under enhanced stress condition. It is known that the trap-density increase is due to increased crystal defects induced by hot carriers. To extract the trap-density increase accurately, the 1/*f* noise measurement is applied, which can be reduced only to the trap-density increase without additional carrier characteristics as demonstrated in Fig. 8 [8]. Since the noise measurement is usually not included in the conventional measurement package for characterizing device features, the conventional *I-V* measurements, as shown in Fig. 8a, are applied for the trap-density extraction. The most dominant aging feature, namely the aging in the subthreshold slope, suggests that mainly the deep-level trap-density increase is enhanced. In this way, the conventional *I-V* measurements are sufficient to extract the trap-density increase, as shown in Fig. 8b. The extraction result concludes that the trap-density increase can be modeled by the substrate-current integration during stress, where the substrate current is a measure for the occurring amount of the hot carriers. Fig. 9 compares the 1/*f* noise measurements after stress application for two different devices. Obviously different aging features are observed. After enhanced-stress applications for characterizing the device-aging properties, it is seen that measured noise characteristics give rise to an additional feature similar to the Lorentzian noise shown in Fig. 7. More experimental investigation is required to clarify the origin of the different noise feature.

A circuit is an aggregation of different devices, and each transistor has microscopically its individual features, as can be expected from Fig. 6. Till now such a condition is usually treated in the circuit community by a worst/best-case analysis, using boundary definitions. Precise investigations of individual device-parameter variations, such as for the channel length, have been considered by applying the Monte-Carlo method. As shown in Fig. 1, a MOSFET is mainly modeled by a current and capacitances during the initial phase of the development. Circuit simulation is further proceeding to include the non-ideal features of the device characteristics. One investigation possibility is combining the newly detected non-ideality with the Monte Carlo method with different weights for different devices in circuit. For the next generation modeling era more microscopic variation such as the trap density must be considered. Here, another question arises, namely whether the device characteristics measured under the DC condition can predict the circuit performance accurately for e.g. such trapping event. It has been argued that the trap-density extraction under the DC condition cannot be directly applied for the switching investigation [9]. The reason is that a trapping event requires time to accomplish completion, namely the necessity of the trap-time constant. To overcome this problem, the switching measurement has to always accompany the DC measurement.

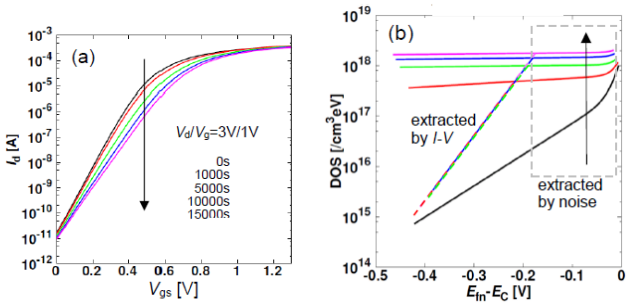


Fig. 8. (a) Measured I-V characteristics after different stress duration. (b) Extracted density of state (DOS) with measured noise intensity increase.

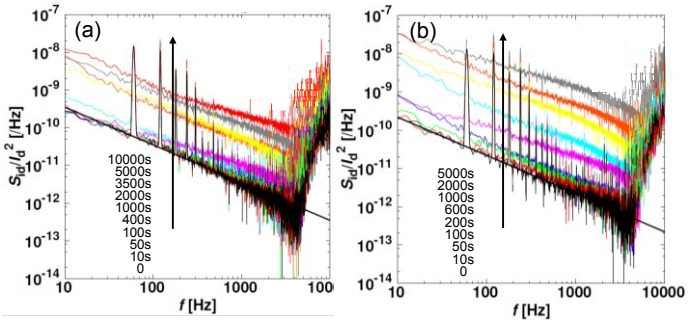


Fig. 9. Measured normalized noise intensity as a function of frequency under different stress duration, (a) with smaller stress condition and (b) with large stress condition.

The conventional circuit simulation for aging consists of two steps. First, the circuit simulation is performed without aging and is devoted only to estimate the stress during the circuit operation. With the estimated stress, aged model parameters are calculated. The second simulation then performs the circuit-aging simulation with the determined aged model parameters. We performed a so-called one-stop simulation for dynamic aging of the small circuit shown in Fig. 10a. The circuit iteration process is used for extracting the trap density accurately at the same time (see Fig. 10b). The resulting trap-density increase during circuit operation is depicted in Fig. 10c. However, this simulation method is possible only for relatively small circuits. If the circuit scale is large, such a simulation takes plenty of simulation time. Consequently, though this method removes the non-consistency of the conventional method, our one-stop method is hardly applicable for real circuit simulation. To overcome this problem, a simple and accurate description for aging of the device characteristics is required. However, the advantage of such macroscopic modeling approach is that the description is so simple that the existing simulation tool can be easily adopted to perform the simulation. For the purpose a reliable bridge between the microscopic feature and the macroscopic description is needed. Fig. 11 shows a measurement conventionally done by the circuit community as an example.

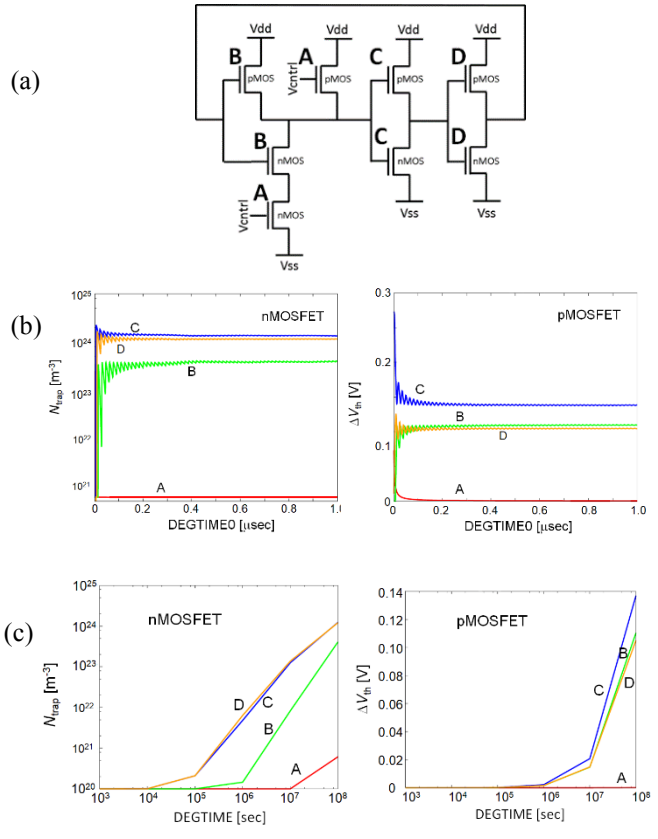


Fig. 10. (a) Studied ring-oscillator (upper left), (b) convergence features of the trap density $N_{trap}$ in the left side the four nMOSFETs and $\Delta V_{th}$ in the right side the four pMOSFETs of the ring-oscillator as a function of circuit simulation time DEGTIME0 after the circuit operation of $10^8$sec, (c) $N_{trap}$ increase of each MOSFET within the circuit as a function of circuit operation time, where pMOSFETs are modeled with the NBIT model shown [8].

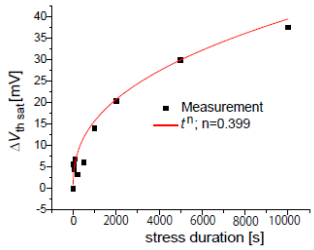


Fig. 11. Conventionally measured aging characteristics for characterizing aging features.

## IV. Conclusion

The presented paper gives an overview of important aspects of the compact-modeling history. The future tasks in conjunction with microscopic device features are discussed. The main insight is the necessity to keep the Poisson equation being used. It has been demonstrated also that investigations of transient characteristics provide further information about the microscopic features of device characteristics.

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## References

[1] J. Watts, C. McAndrew, C. Enz, C. Galup-Montoro, G. Gildenblat, C. Hu, R. van Langevelde, M. Miura-Mattausch, R. Rios, C.-T. Sah, "Advanced compact models for MOSFETs," Modeling and Simulation of Microsystems, pp. 3-12, Anaheim, May 2005.

[2] J. E. Meyer, "MOS models and circuit simulation," RCA Rev., vol. 32, pp. 42-63, 1971.

[3] C.-T. Sah, "Characteristics of the metal-oxide-semiconductor transistors," IEEE Trans. Electron Devices, vol. 11, no. 7, pp. 324-345, 1964.

[4] M. Miura-Mattausch, N. Sadachika, D. Navarro, G. Suzuki, Y. Takeda, M. Miyake, T. Warabino, Y. Mizukane, R. Inagaki, T. Ezaki, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, S. Kumashiro, S. Miyamoto, "HiSIM2: Advanced MOSFET model valid for RF circuit simulation," IEEE Trans. Electron Devices, vol. 53, pp. 1994-2007, September 2006.

[5] D. Hori, Master Thesis, "For predicting ringoscillator oscillation frequency under low voltage operation," Hiroshima University, Higashi-Hiroshima, March 2010.

[6] S. Matsumoto, H. Ueno, S. Hosokawa, T. Kitamura, M. Miura-Mattausch, H. J. Mattausch, T. Ohguruo,S. Kumashiro, T. Yamaguchi, K. Yamashita, N. Nakayama, "1/*f*-noise characteristics in 100nm-MOSFETs and its modeling for circuit simulation," IEICE Trans. Electron., vol.E88-C, pp. 247-254, February 2005.

[7] T. Nakahagi, Master Thesis, "Analysis and modeling of low noise charactersitcs in Poly-Si TFT," Hiroshima University, Higashi-Hiroshima, March 2013.

[8] M. Miura-Mattausch, H. Miyamoto, H. Kikuchihara, T. K. Maiti, N. Rohbani, D. Navarro, H. J. Mattausch, "Compact modeling of dynamic trap density evolution for predicting circuit-performance aging," Microelectronics Reliability, vol. 80, pp. 164-175, 2018.

[9] Y. Tanimoto, A. Saito, K. Matsuura, H. Kikuchihara, H. J. Mattausch, M. Miura-Mattausch, and N. Kawano, "Power-loss prediction of high-voltage SiC-MOSFET circuits with compact model including carrier-trap influence," IEEE Trans. Power Electronics, vol. 31, pp. 4509-4516, June 2016.