NEGF simulations of stacked silicon nanosheet FETs for performance optimization

Hong-Hyun Park
Device Laboratory
Samsung Semiconductor Inc.
San Jose, California, USA
honghyun.p@samsung.com

Woosung Choi
Device Laboratory
Samsung Semiconductor Inc.
San Jose, California, USA

Mohammad Ali Pourghaderi
Semiconductor R&D Center
Samsung Electronics
Hwasung-si, Gyeonggi-do, Korea

Jongchol Kim
Semiconductor R&D Center
Samsung Electronics
Hwasung-si, Gyeonggi-do, Korea

Uihui Kwon
Semiconductor R&D Center
Samsung Electronics
Hwasung-si, Gyeonggi-do, Korea

Dae Sin Kim
Semiconductor R&D Center
Samsung Electronics
Hwasung-si, Gyeonggi-do, Korea

***Abstract*— We present quantum transport simulation results of stacked silicon nanosheet (SiNS) nFETs. Our simulations are based on the non-equilibrium Green's function (NEGF) method which is capable of dealing with all major physical effects necessary for steady-state electron transport in the complex-shaped devices. In order to help find optimal device design many split simulations for various geometry and process conditions were performed as a demonstration.**

Keywords—quantum transport, non-equilibrium Green's function (NEGF), stacked nanosheet FET

I. Introduction

The FinFET technology is the most advanced node for commercial logic device fabrications nowadays. Its success was enabled mainly by the larger effective channel width and stronger gate controllability than previously used planar FETs. As long as we stick to the concept of field-effect transistor, a key technology requirement to boost the device performances will be to achieve better gate controllability. Hence, gate-all-around FETs are being studied as an ultimate structure for future logic devices [1]. Stacked silicon nanosheet FETs are considered as one of the strong candidates which have potential to replace FinFETs [2]. Although the fabrication processes of SiNS FETs are more complex than those of FinFETs, the better gate controllability is more favorable to shorter channel length and better performance. An example of dual SiNS FET is shown in Fig. 1. The number of channel stacks can be more than two in reality.

Considering the size and shape, the stacked SiNS FET is expected to have significant quantum and atomistic effects with its performance. Also, there are many design variables related to geometry dimensions or process conditions, which might not be optimized one by one because of their possible intercorrelations. In this case a tool which can accurately estimate the device performance to the changes of the design variables is required. We employ the self-consistent NEGF-Poisson approach in this work because of its rigorous and general theoretical basis which does not depend on the design variables.

In this paper we explain our simulation models and demonstrate how the NEGF simulation can be used for the optimization of the design of dual SiNS nFETs.

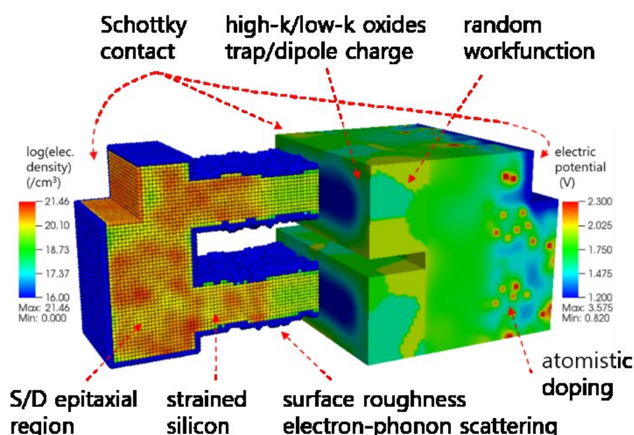

Fig. 1. Structure of simulated dual SiNS nFET and physical models avalable in our in-house NEGF solver. Electron density and electric potential profiles at $V_G = 1$ V and $V_D = 0.01$ V are visualized from atomistic and continuum simulation domains, respectively.

II. Simulation Method

We use our in-house atomistic and quantum transport simulation tool. For device simulations the NEGF and the Poisson equations are solved self-consistently. The NEGF solver covers the silicon region for carrier transport while the Poisson solver covers the whole region for electrostatic potential. The NEGF solver is equipped with various models to take into account all the major physical phenomena as shown in Fig. 1. The following are explanations of the physical models:

1) The bandstructure of the conduction band of silicon is modelled by the effective-mass approximation (EMA) [3, 4]. Each ellipsoidal valley is characterized by a mass tensor with nonparabolicity correction. The model parameters for each valley are calibrated against tight-binding simulation results to take into account the effects of quantum confinement and strain/stress more accurately [5, 6]. For the sake of numerical efficiency only three valleys out of six are considered without loss of accuracy.

2) Electron-phonon scattering is modelled based on the deformation potential theory which can capture intra- and inter-valley scattering processes [7]. The basic parameters were calibrated to fit bulk mobility of silicon [8, 9]. To fit

978-1-7281-0940-4/19/$31.00 ©2019 IEEE

experimentally observed mobility decrease in the strong inversion regime which could not be captured by the original scattering model, the deformation potential values are adjusted to be enhanced near the surface of the channel [10].

3) Atomistic doping model is used to consider the effects of dopant variation and impurity scattering explicitly in the NEGF simulations [11, 12]. Random and discrete point charges are generated from a given continuous doping profile according to Poisson statistics.

4) Remote Coulomb scattering due to high-k dielectric layer can be modelled by putting static monopole or dipole charges into the source terms of the Poisson solver.

5) Atomistic traps can be generated based on [13]. This effective trap model works well as long as the self-consistent Born approximation (SCBA) does not fail to converge due to any resonance states at the traps.

6) Surface roughness on the channels is generated according to given sets of amplitude and correlation length [14]. Different roughness and random seeds can be applied to different channels. Although the quality of generated surface depends on the lattice constant of the simulation structure, the simulation results were not sensitive to the atomic-scale resolution.

7) To consider the variability effect due to the gate metal phenomenologically, it is assumed that the gate metal consists of grains with random sizes and workfunction values [15]. Some parameters such as the distribution of the grain size and the distribution of workfunction values are necessary.

8) In quantum transport simulations the gate contact is usually modelled as a Dirichlet boundary condition in the Poisson solver with the assumption that there is no current through the contact. To be more realistic, we can treat the contact as an open-boundary lead like the source/drain contacts and calculate the gate leakage current. In order to improve the numerical efficiency, we have improved the conventional recursive Green's function (RGF) technique [16] to be able to simulate arbitrary-shaped devices [17].

9) Schottky contacts are attached on the source/drain epitaxial regions as shown in Fig. 1. In quantum transport simulations, it is usually assumed that a contact is a semi-infinite extension of its connected part of the simulation domain [18, 19], which is not appropriate for realistic metal-semiconductor interfaces. So, in this work the contact model was improved more realistically by two modifications. Firstly, virtual metals are introduced for contacts. Each type of metal requires three parameters under EMA model, i.e. effective mass, workfunction, and band edge. The workfunction parameter is used to give desired Schottky barrier height when a Dirichlet boundary condition is applied to the contact and the other parameters are calibrated to give desired I-V characteristic or Schottky resistance. Secondly, the new contact model assumes that each of the contact atoms is an independent reservoir of carriers and does not interact with the other contact atoms. By this assumption different incident directions can be set for different contact atoms so the shape of a contact can be an arbitrary curved surface. Another advantage is that the calculation of the contact self-energy function is much faster than that of conventional contact models because the function can be evaluated independently for each atom.

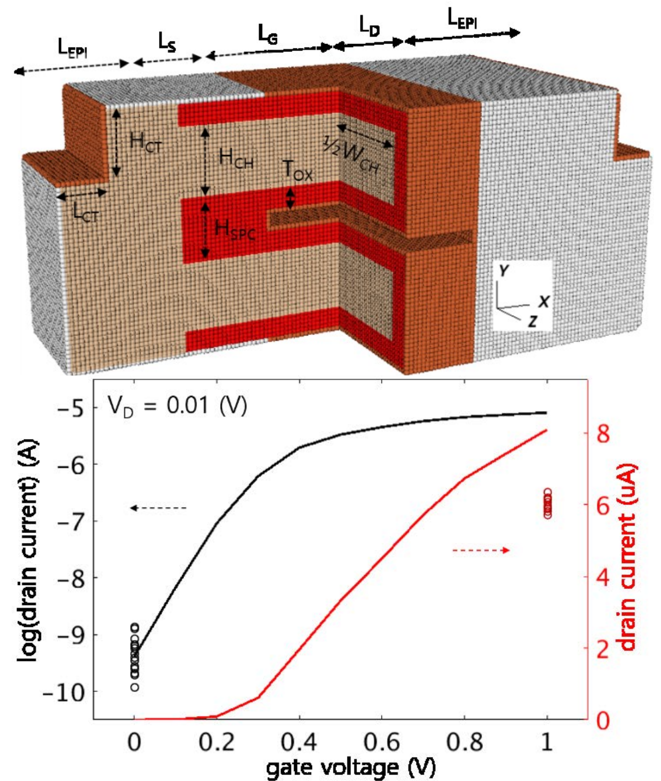

Fig. 2. (TOP) Base simulation structure for the sensitivity analysis of dual SiNS nFETs. Silicon, oxide, and contact metal regions are represented in ivory, red, and orange colors, respectively. The space between the channels is not empty in real devices but filled with gate metal. This particular structure has two SiNSs as its channels and bulky epitaxial regions for source and drain. The dimensions of this base structure are 50 nm, 22 nm, and 24 nm along x, y, and z directions, respectively. The channels are lightly doped with p-type and the source/drain regions are heavly doped with n-type. (BOTTOM) I_D-V_G characteristic of the base simulation structure. The lines are the case of continuum doping model without surface roughness in the channels or random workfunction of metal grains. For the simulations with atomistic dopant, surface roughness, and random workfunction models, only V_G = 0 V and V_G = 1 V were performed, which are are marked with dots according to different random configurations. The variation in I_{OFF} and the degradation of I_{ON} are confirmed.

III. Simulation Results

To show a demonstration how the design variables of stacked SiNS nFETs affect the device performance, we performed many split simulations by changing each design variable one by one from the base device shown in Fig. 2. Please note that the simulated device structures and conditions are not based on real devices but set for the demonstration of this simulation study. All the simulation results are obtained from self-consistent NEGF simulations with the models explained in the previous section. Here, some models like atomistic traps, dipole changes due to remote Coulomb scattering, and gate leakage were not activated because these require statistical analysis based on experimental data or have minor effects on the device performance. All the simulation parameters were calibrated to reproduce basic electrical properties of materials and the same set of parameters were used for all the simulations. The simulation is highly parallelized by MPI, OpenMP, and GPU. A typical simulation time for each bias condition is about 4~5 hours using 80 cores of Intel® Xeon® CPU E5-2699 v3 @ 2.30GHz.

TABLE I. SENSIVIITY OF VTH, SS, AND ION TO THE CHANGES OF DESIGN VARIABLES (V_{DS} = 0.01 V)

variable change	*Δ Vth (mV)*	*Δ SS / SS*	*Δ Ion / Ion*
L_G -14 %	-54	15.9 %	4.8 %
EOT 20 %	-17	4.6 %	-2.8 %
W_{CH} -50 %	61.2	-9.8 %	-42.1 %
H_{CH} 33 %	-71	18.5 %	19.1 %
S_{SPC} 33 %	1.1	1.8 %	0.4 %
L_{CT} 100 %	-0.1	0.2 %	9.9 %
H_{CT} 100 %	0.4	0.4 %	14.1 %
L_{OVL} 0 → 0.4 nm	-17	4.1 %	4.2 %
L_{UDL} 0 → 0.4 nm	15.1	-4.7 %	1.1 %
N_{CH} 1E17 → 0 /cm^3	-0.8	0.1 %	2.1 %
$N_{S/D}$ 3E20 → 2E20 /cm^3	9	-0.8 %	-21.6 %

Table I shows how much threshold voltage (V_{TH}), subthreshold slope (SS), and on-current level (I_{ON}) are affected by the change of design variables. Although just 11 design variables and 3 performance criteria were considered in this paper to find the steepest gradient for better device performance, in principle we can play with any geometry and simulation conditions. Since the model parameters of NEGF solver are only related to the properties of materials, we have high confidence of the accuracy of the simulation results within the limitation of the NEGF formalism itself. In reality, some practical considerations such as fabrication difficulty, cost, yield should be taken into account in the optimization process.

IV. CONCLUSION

In this paper we have shown a demonstration how the self-consistent NEGF-Poisson method can be used to help optimize the design of stacked SiNS nFETs. We could evaluate the sensitivity of device performance to the changes of design variables such as geometry and process conditions.

REFERENCES

[1] B.-H. Lee, M.-H. Kang, D.-C. Ahn, J.-Y. Park, T. Bang, S.-B. Jeon, J. Hur, D. Lee, and Y.-K. Choi, "Vertically Integrated Multiple Nanowire Field Effect Transistor," Nano Lett. 15 (12), pp. 8056-8061, 2015.

[2] N. Loubet et al., "Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET," in Proc. Symp. VLSI Tech. Dig., pp. 230-231, 2017.

[3] E. O. Kane, "Band structure of indium antimonide," J. Phys. Chem. Solids, vol. 1, pp. 249-261, 1957.

[4] W. R. Frensley, "Boundary conditions for open quantum systems driven far from equilibrium," Rev. Mod. Phys., vol. 62, no. 3, pp. 745-791, 1990.

[5] J. C. Slater and G. F. Koster, "Simplified LCAO Method for the Periodic Potential Problem," Phys. Rev., vol. 94, no. 6, pp. 1498-1524, June 1954.

[6] T. B. Boykin, "Strain-indluced, off-diagonal, same-atom parameters in empirical tight-binding theroy suitable for [110] uniaxial strain applied to a silicon parameterization," Phys. Rev. B 81, 125202, 2010.

[7] S. Jin, Y. J. Park, and H. S. Min, "A three-dimensional simulation of quantum transport in silicon nanowire transistor in the presence of electron-phonon interactions," J. Appl. Phys., vol. 99 (12), pp. 123719-123729, 2006.

[8] C. Jacoboni and L. Reggiani, "The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials," Rev. Mod. Phys. 55, pp. 645-705, 1983.

[9] M. V. Fischetti and S. E. Laux, "Band Structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," J. Appl. Phys. 80, pp. 2234-2252, 1996.

[10] T. Ohashi, T. Tanaka, T. Takahashi, S. Oda, and K. Uchida, "Experimental Study on Deformation potential (Dac) in MOSFETs: Demonstration of Increased Dac at MOS Interfaces and Its Impact on Electron Mobility," IEEE J. Electron Devices Soc., vol. 4, pp. 278-285, 2016.

[11] A. Asenov et al., "Simulation of statistical variability in nano-CMOS transistors using drift-diffusion, Monte Carlo and non-equilibrium Green's function techniques," J Comput Electron, pp. 349-373, 2009.

[12] Y.-M. Niquet, V.-H. Nguyen, F. Triozon, I. Duchenmin, O. Nier, and D. Rideau, "Quantum calculations of the carrier mobility: Methodology, Matthiessen's rule, and comparison with semi-classical approaches," J. Appl. Phys. 118, 054512, 2014.

[13] M. G. Pala and D. Esseni, "Interface Traps in InAs Nanowire Tunnel-FETs and MOSFETs—Part I: Model Description and Single Trap Analysis in Tunnel-FETs," IEEE Trans. Elec. Dev. vol. 60, no. 9, pp. 2795-2801, 2013.

[14] M. Luisier, "Quantum Transport Beyond the Effective Mass Approximation," Ph.D. dissertation, ETH Zurich, 2007.

[15] Y. Li and H.-W. Cheng, "Random Work-Function-Induced Threshold Voltage Fluctuation in Metal-Gate MOS Devices by Monte Carlo Simulation," IEEE Trans. Semicond. Manuf., vol. 25, no. 2, pp. 266-271, 2012.

[16] R. Lake, G. Klimeck, R. C. Bowen, and D. Jovanovic, "Single and multiband modeling of quantum electron transport through layered semiconductor devices," J. Appl. Phys. 81 (12), pp. 7845-7869, 1997.

[17] H.-H. Park, W. Choi, M. A. Pourghaderi, J. Kim, U. Kwon, and D. S. Kim, "Toward more realistic NEGF simulations of vertically stacked multiple SiNW FETs," in Proc. SISPAD Conference, pp. 206-209, 2018.

[18] M. P. Lopez Sancho, J. M. Lopez Sancho, and J. Rubio, "Highly convergent schemes for the calculation of bulk and surface Green functions," J. Phys. F: Met. Phys. 15, pp. 851-858, 1985.

[19] M. Luisier, A. Schenk, and W. Fichtner, "Atomistic simulation of nanowires in the sp3d5s* tight-binding formalism: From boundary conditions to strain calculations," Phys. Rev. B 74, 205323, 2006.