A First Principle Insight into Defect Assisted Contact Engineering at the Metal-Graphene and Metal-Phosphorene Interfaces

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***Abstract*—In this work we have studied bonding nature of Graphene and Phosphorene with metal (Pd) followed by carrier transport behavior and contact resistance engineering across the metal-Graphene and the metal-Phosphorene interfaces using Density Functional Theory (DFT) and Non Equilibrium Green's Function (NEGF) computational methods. We have studied, how carrier transports at the interfaces is limited by van der Waals (vdW) gap across the interfaces and how the gap can be reduced by creating the Carbon vacancy (defect engineering) at the Graphene-Palladium interface. We have seen that the defect engineering enhances the Carbon-Palladium bond at the interface which reduces the van der Walls (vdW) gap, hence contact resistance due to corresponding reduction in the tunneling barrier width at the interface. We have also studied that the defect engineering (Phosphorous vacancy) at the Phosphorene-Palladium interface is not effective as Graphene-Palladium interface because it has less interfacial (vdW) gap than Graphene-Palladium interface intrinsically.**

Keywords—DFT; NEGF; vdW

I. INTRODUCTION

Invention of Graphene [1] along with other 2D materials (eg. TMDs, Phosphorene) [2] has opened new door for the semiconductor device scaling research but very soon it has been realized that the contact resistance at the metal-2D material interface [2], [3] is the main bottleneck for their performance improvements. The contact resistance at the interface is high due to Schottky barrier, tunnel barrier and various kinds of trap states (eg. defect assisted, metal induced) at the interface [3]. Defect engineering (creating vacancy at the metal-2D material interface) is a promising technique for contact resistance improvement in the Graphene based transistors [4], [5], but its physics and chemistry at the interface is needed to be explored more. Defect engineering at other 2D elemental material-metal contacts like Phosphorene-metal is not explored yet so it can also be explored to see the impact of the defect engineering on the carrier transport through its interfaces and also corresponding physics and chemistry at the interface.

In this work, we have explored the interface chemistry and carrier transport physics of Graphene and Phosphorene with metal (Pd) using DFT and NEGF methods supported in Quantum ATK package [6], [7], [8]. We have studied how Graphene-metal and Phosphorene-metal bonding properties at their contact interfaces are changed when Carbon (C) and Phosphorous (P) vacancies are created (defect engineering) at the intrinsic Graphene-Palladium and Phosphorene-Palladium contacts respectively. We have studied how carrier transmission probability and hence contact resistance at the interfaces changes due to change in interfacial bonding distance by these defect engineering. We have explained the improvement in the contact resistance due to defect engineering at the Graphene-Palladium interface by corresponding improvement in the carrier transmission probability. Finally after transport current analysis at the interfaces, we have concluded that defected engineering is a promising way to improve the contact resistance (~2.3 times) at the Graphene-Palladium interface but it is not promising way for the Phosphorene- Palladium interface.

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II. COMPUTATION DETAILS

All the bulk structures are optimized with 0.01 eV/Å force tolerance and 0.001 eV/Å^3 energy tolerance. Palladium (Pd) is cleaved in [111] direction before creating Graphene-Palladium (Gr.-Pd) and Phosphorene-Palladium (Ph.-Pd) interfaces for minimum interfacial strain, which is applied on the metal to minimize the strain effect on the Graphene/Phosphorene. The Interface width and length are 8.382 Å and 12.062 Å for Graphene- Palladium and, 16.49 Å and 9.92 Å for Phosphorene-Palladium interfaces respectively. The density mesh cutoff is 75 Hartree with 10 k-points along the width and 200 k-points along the channel of the devices in the calculation with local density approximation (LDA) exchange correlation functional. A source–drain bias of 250 mV is applied to conduct the carrier transport analysis on 300K electron temperature.

III. RESULTS AND ANALYSIS

When the carrier (electron or hole) transports through the metal-2D material interface, it encounters tunnel barrier and Schottky barrier at the interface. There are following four parameters which determines the carrier transport probability at the interface: (i) Tunnel barrier width; (ii) Tunnel barrier height; (iii) Schottky barrier width and (iv) Schottky barrier height (Figure 1). Tunnel barrier width is the van der Waals (vdW) gap between metal and 2D materials which can be reduced by enhancing metal and 2D materials bonding by creating vacancy at the interfaces.

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In the First step, we have computed bond energy minima optimization for the Graphene-Pd and Phosphorene-Pd interfaces using DFT for their intrinsic interface and interfaces with vacancy. It is observed that the Carbon (C) vacancy at the Graphene-Pd interface region improves the 'Pd-C' covalent bond while Phosphorous (P) vacancy does not have a major impact on the bonding at Phosphorene-Pd interface (Figure 2).

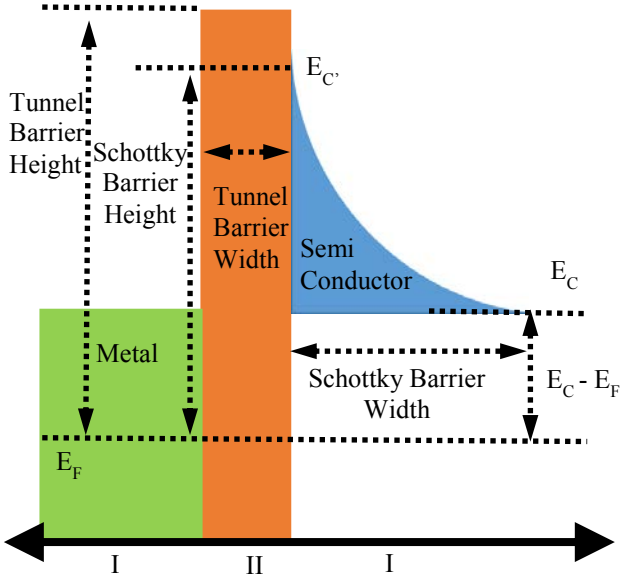

Figure 1: Schematic of different types of barriers in the carrier transport at the metal-2D materials interface.

Graphene has weak vdW interaction with 'Pd' due to unavailability of vacant orbital in the 'C' atom. When a 'C' vacancy is created at the interface, Graphene-Pd bond becomes stronger due to bonding of 'Pd' with vacant orbitals available at the three nearest neighbor 'C' atoms of the vacant site which reduces average bond length from 2.61 Å to 2.50 Å. Phosphorene has relatively stronger bond with 'Pd' intrinsically due to interaction of 'Pd' electron cloud with vacant 3d orbitals available in Phosphorous. However, unlike Graphene-Pd interface, the bond length is not significantly affected (2.20 Å to 2.18 Å) in the presence of 'P' vacancy at the Phosphorene-Pd interface.

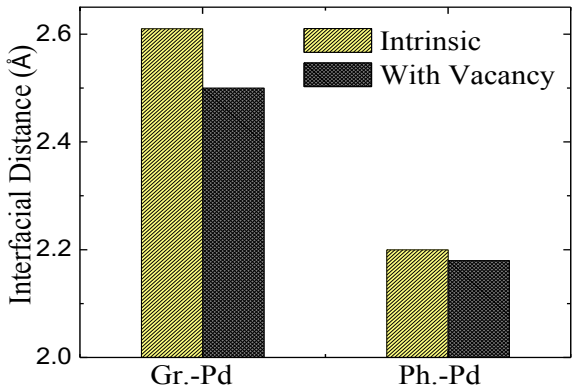

Figure 2: Defect Engineering (Creating Vacancy) reduces interfacial distance significantly (2.61 Å to 2.50 Å) for Graphene-Pd interface but it doesn't have significant impact on the interfacial distance (2.20 Å to 2.18 Å) of the Phosphorene-Pd interface.

Contact resistance of the metal-semiconductor interface is determined by carrier (electron for this work) transmission probability (CTP) and density of state (DOS) near fermi level of the interface. CTP reflects how easily the electron can move from metal to semiconductor (and vice versa) at the interface. When electron flows from metal to semiconductor across interface, it moves from fermi level state of the metal side to the conduction band minima (CBM) of the semiconductor side. There are mainly two barriers available at the interface to throttle the electron flow, Schottky barrier and tunnel barrier. The tunnel barrier depends on the interfacial distance between metal and semiconductor. Defect engineering on the Graphene-Pd interface reduces the interfacial distance and hence reduces the tunnel barrier (Figure 3). Reduction in the tunneling barrier enhances the electron transmission probability of the electron at the interface (Figure 4).

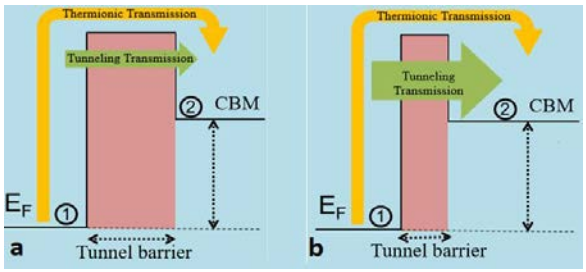

Figure 3: Representation of tunneling distance and hence electron transmission probability in the (a) intrinsic and (b) defect engineered Graphene-Pd interfaces. 'b' has more electron transmission probability than 'a' due to less tunneling distance.

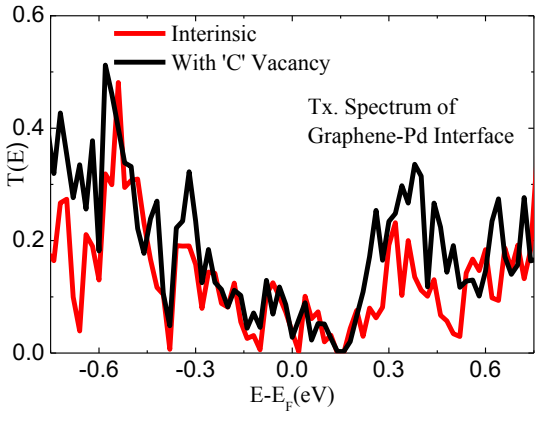

Figure 4: Transmission probability of electron at the intrinsic and defect engineered Graphene-Pd interfaces, computed using DFT and NEGF. Defect engineered interface has better transmission probability than intrinsic interface.

Intrinsic Phosphorene-Pd interface has less interfacial distance and hence tunneling distance than intrinsic Graphene-Pd interface so it has better electron transmission probability than Graphene-Pd interface as shown in Figure 5. Since defect engineering in the Phosphorene-Pd interface hasn't significant impact on the interfacial and hence tunneling distance, so it has similar transmission spectrum as corresponding intrinsic interface (Figure 6)

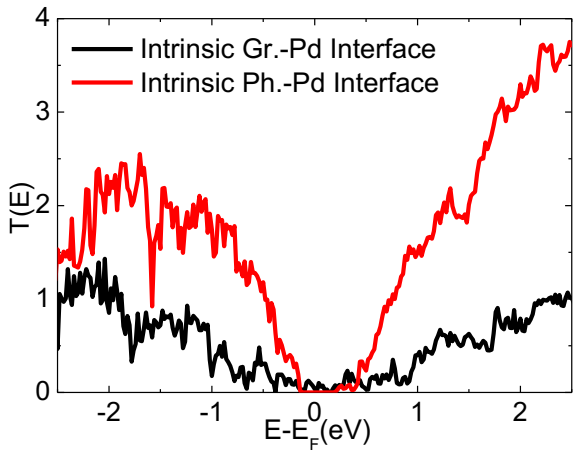

Figure 5: Transmission probability of electron at the intrinsic Graphene-Pd and Intrinsic Phosphorene-Pd interfaces, computed using DFT and NEGF. Intrinsic Graphene-Pd interface has better transmission spectrum than intrinsic Phosphorene-Pd interface.

Enhancement in the electron transmission probability due to defect engineering reduces the contact resistance and hence increases the current flow across the Graphene-Pd interface.

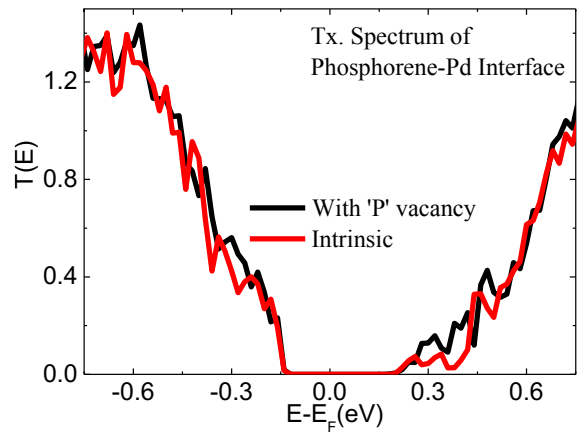

Figure 6: Transmission probability of electron at the intrinsic and defect engineered Pd-Phosphorene interfaces, computed using DFT and NEGF. Both interfaces have similar transmission spectrum

Defect engineering doesn't improve the transmission probability at the Phosphorene-Pd interface hence it doesn't improve the current but decreases due to excess sheet resistance added by Phosphorous vacancy at the interface (Figure 7).

IV. CONCLUSION

We have studied the impact of the defect engineering on the Pd-C and Pd-P bonds at the Graphene-Palladium and Phosphorene-Palladium interfaces respectively. We have seen that defect engineering reduces the average Pd-C bond length but it doesn't change average Pd-P bond length significantly at corresponding interfaces. Reduction in the bond length enhances the carrier transmission probability and hence reduces the contact resistance (~2.3 times) due to reduction in the tunnel barrier at the Graphene-Palladium interface. Reduction in the contact resistance due to defect engineering at the Graphene-Palladium interface is in agreement with the reported experimental work [5]. 'P' vacancy doesn't result in a significant improvement in contact resistance at Phosphorene- Palladium interface due to insignificant changes in the tunnel barrier.

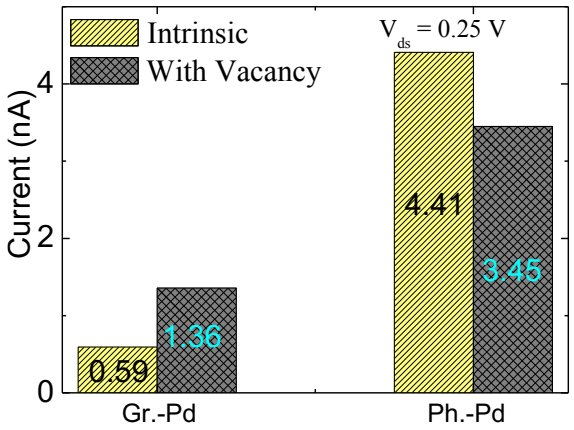

Figure 7: Computed current values across the intrinsic and defect engineers Graphene-Pd and intrinsic and defect engineers Phosphorene-Pd interfaces respectively using DFT and NEGF. Defect engineered Graphene-Pd interface has higher current than corresponding intrinsic interface. Defect engineered Phosphorene-Pd interface has lower current than corresponding intrinsic interface. Phosphorene-Pd interface has higher current than corresponding Graphene-Pd interface.

V. ACKNOLEDGMENT

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