

Simulation and Investigation of Electrothermal Effects in Heterojunction Bipolar Transistors

Xujiao Gao
electrical models and simulation
sandia national laboratories
Albuquerque, USA
xngao@sandia.gov

Gary Hennigan
electrical models and simulation
sandia national laboratories
Albuquerque, USA
glhenni@sandia.gov

Lawrence Musson
electrical models and simulation
sandia national laboratories
Albuquerque, USA
lcmusso@sandia.gov

Andy Huang
electrical models and simulation
sandia national laboratories
Albuquerque, USA
ahuang@sandia.gov

Mihai Negoita
electrical models and simulation
sandia national laboratories
Albuquerque, USA
mnegoit@sandia.gov

Abstract—We present a comprehensive physics investigation of electrothermal effects in III-V heterojunction bipolar transistors (HBTs) via extensive Technology Computer Aided Design (TCAD) simulation and modeling. We show for the first time that the negative differential resistances of the common-emitter output responses in InGaP/GaAs HBTs are caused not only by the well-known carrier mobility reduction, but more importantly also by the increased base-to-emitter hole back injection, as the device temperature increases from self-heating. Both self-heating and impact ionization can cause fly-backs in the output responses under constant base-emitter voltages. We find that the fly-back behavior is due to competing processes of carrier recombination and self-heating or impact ionization induced carrier generation. These findings will allow us to understand and potentially improve the safe operating areas and circuit compact models of InGaP/GaAs HBTs.

Index Terms—heterojunction bipolar transistor, TCAD, self-heating, impact ionization, mobility reduction, hole back injection

I. INTRODUCTION

Heterojunction bipolar transistors (HBTs) based on the InGaP/GaAs material system are widely used in wireless communication systems, due to their higher power, faster switching speed, and higher efficiency, when compared to silicon devices. It is generally recognized [1] [2] that the electrothermal effect (a.k.a. self-heating effect) has a strong influence on device performance of III-V HBTs. The interplay of self-heating with impact ionization (a.k.a. avalanche breakdown) limits their safe operating areas (SOAs) [3] [4]. Several papers [3] [4] [5] have reported the measured SOAs of

This work is funded by the Advanced Scientific Computing (ASC) program at Sandia National Laboratories. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA-0003525. The views expressed in the article do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

InGaP/GaAs HBTs in non-radiation environments. Accompanying the experimental work, there exists a number of papers [1] [2] [6] [7] that employed Technology Computer Aided Design (TCAD) device codes to model the self-heating effect in III-V HBTs. Although Rinaldi *et al.* [8] [9] were able to simulate the complex device failure characteristics due to self-heating and impact ionization in silicon bipolar transistors, modeling and understanding of device failure mechanisms in III-V HBTs is quite limited. In fact, the physics of self-heating and its interplay with impact ionization in III-V HBTs is not well understood. This is evidenced by the fact that existing compact HBT models often do not work well [10] when modeling the self-heating effect even in the operating regimes far from device failure.

In this paper, we present physics-based TCAD simulation and modeling of self-heating and impact ionization effects in an InGaP/GaAs HBT. We present a detailed physics understanding of the self-heating effect and its interplay with impact ionization. This understanding would enable us to potentially improve the SOAs and circuit compact models of these devices.

II. MODELING APPROACH

Simulations were done using Charon [11], a multi-dimensional, Messaging Passing Interface (MPI) based parallel TCAD device code, which we developed at Sandia National Laboratories. Charon supports isothermal drift diffusion (DD) modeling and coupled electrothermal (i.e., DD + lattice heating) simulation. Our device of interest is an emitter-up $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}/\text{GaAs}$ NP^+N HBT [12]. Figure 1 shows the simulated two-dimensional (2D) structure, which represents a truncated half-finger cross-section of a real device. The coupled model is applied to all the semiconductor regions, while the lattice heat equation is solved in the metal and nitride regions. To properly simulate device self-heating, temperature dependencies were incorporated in all important material mod-

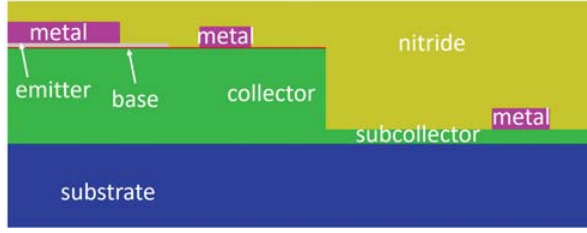


Fig. 1. Simulated 2D structure for a lattice-matched $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}/\text{GaAs}$ HBT. The emitter is n-type $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}$, the base is p^+ -type GaAs, while the collector and subcollector are n-type GaAs. The metal regions provide electrical contacts. To properly simulate the lattice heating, the capping nitride region and a small part of the semi-insulating GaAs substrate are also included.

els, including band gap, carrier mobility, thermal conductivity, and heat capacity [13]. The carrier mobility models are similar to those given in [14]. For impact ionization (II), several GaAs II models [15] [16] [17] were studied and found to produce similar II coefficient vs. field curves. The Plimmer II model [16] was used in this work. Carrier transport across the emitter-base (E-B) heterojunction (HJ) is governed by thermionic emission (TE) and tunneling processes [18]. The net hole TE current density across the HJ is given by

$$J_{TE,p} = A_p^* T^2 \left[\frac{p_E}{N_{V,E}} - \frac{p_B}{N_{V,B}} \exp\left(-\frac{\Delta E_V}{k_B T}\right) \right]. \quad (1)$$

Here A_p^* is the Richardson coefficient and other symbols have their usual meanings. Our simulation results show that the tunneling current across the HJ contributes only about 10% of the total current in the HBT.

The choice of thermal boundary conditions plays a vital role in determining the temperature profile. The bottom of the simulated structure had a thermal conductance of $10 \text{ W}/(\text{K}\cdot\text{cm}^2)$ estimated from the substrate thickness and GaAs thermal conductivity. The top surface had a thermal conductance of $200 \text{ W}/(\text{K}\cdot\text{cm}^2)$ obtained by fitting simulated results to measured output response data at a given base current.

III. RESULTS AND DISCUSSION

We first investigate the self-heating (SH) effect in the InGaP/GaAs HBT without II. Figure 2 shows the simulated common-emitter results under constant base currents (I_B). The black solid curves in the top figure are widely observed in simulation and experimental results [1] [4] for III-V HBTs. The negative slopes in these curves are often attributed to the reduction of carrier mobility with increasing temperature [1]. However, this explanation is only one part of the puzzle, because the simulated collector current (I_C) vs. collector voltage (V_{CE}) curves still show strong negative slopes, even when the temperature dependencies were removed from the mobility models, as shown by the red curves in the top of Fig. 2. We discovered that the other dominant mechanism is the hole back injection from the base to the emitter. This can be seen from the blue curves, which show a much smaller decrease in I_C at high V_{CE} , when the temperature in the exponential term of the

hole TE model (1) was replaced by 300 K. The observation becomes more evident from the bottom plot of Fig. 2. In the low temperature regime, I_C shows a power-law reduction with increasing temperature, indicating the reduced carrier mobility is responsible for the I_C reduction. In the high temperature regime, I_C shows an exponential reduction with increasing temperature, indicating the base-to-emitter hole back injection dominates the decreasing in I_C . For medium temperatures, both mechanisms play an important role in reducing I_C .

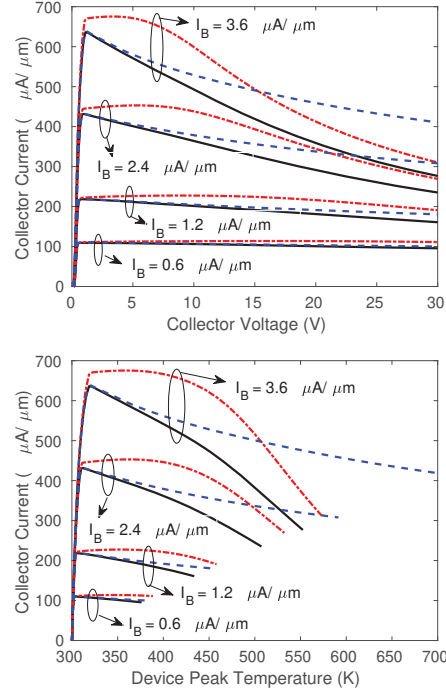


Fig. 2. Simulated I_C vs. V_{CE} (top) and I_C vs. device peak temperature (bottom) curves under constant I_B . Black solid curves were obtained with all temperature dependencies included. Red dot-dashed curves were obtained with the temperature dependencies removed from the mobility models. Blue dashed curves were obtained with the temperature in the exponential term of the hole TE model (1) replaced by 300 K, whereas keeping all other temperature dependencies in the simulation. The device peak temperature was taken to be the maximum temperature in the simulation domain at a given bias condition.

In the case of constant base-emitter voltages (V_{BE}), the I_C vs. V_{CE} curves are very different from those of the constant I_B case. Figure 3 shows the simulated I_C (top) and device peak temperature (bottom) vs. V_{CE} curves using the SH model without II under constant V_{BE} . We observe that the simulated device is significantly heated up, especially in the high V_{BE} and/or high V_{CE} regimes. The simulated temperature profiles corresponding to the turning point and the peak current for the case of $V_{BE} = 1.26 \text{ V}$ are plotted in Fig. 4. We see that the temperature has a strong non-uniform shape and the device is heated up mostly in the active region below the emitter.

The I_C - V_{CE} curves in Fig. 3 clearly show fly-back behavior

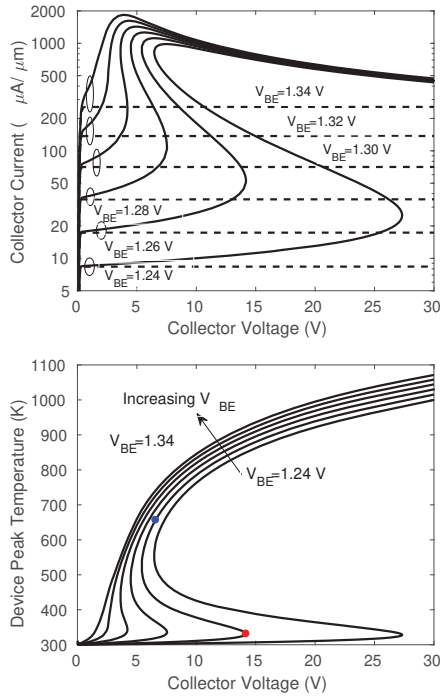


Fig. 3. Simulated I_C (top) and device peak temperature (bottom) vs. V_{CE} curves under constant V_{BE} . Black solid curves were obtained using the SH model without II, whereas black dashed curves were obtained using the isothermal DD model without II.

at low V_{BE} values, whereas this SH induced fly-back does not occur in the constant I_B case (Fig. 2). Though similar phenomena were observed by other authors [8] [9], the underlying physics was still unclear. We found that, during the fly-back process, I_B increases and the transistor gain decreases (Fig. 5), while the device temperature keeps increasing (Fig. 3). This indicates that fly-back occurs due to competing mechanisms of SH induced carrier generation and standard carrier recombination processes. At a given low V_{BE} , as the device heats up with increasing V_{CE} , thermal generation increases carrier densities and hence increases the overall carrier injection from the emitter, leading to larger I_C on the fly-back curve; on the other hand, carrier recombination in the base also increases due to excess carriers, which leads to larger I_B and smaller gain. At high V_{BE} , the fly-back does not occur, because carrier injection from the emitter electrode is so high that it obscures the effect of thermal carrier generation.

Furthermore, we notice that, at high I_C , independent of V_{BE} , all the I_C - V_{CE} curves show negative slopes and converge to more or less the same curve. This is because the base-to-emitter hole back injection dominates at high temperatures and the device loses its transistor action. It is worth pointing out that the simulated I_C - V_{CE} curves without the fly-backs at high V_{BE} are qualitatively very similar to the measured curves by Lee *et al.* [4] for a different InGaP/GaAs HBT design.

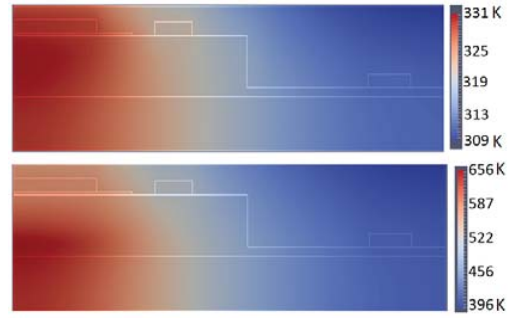


Fig. 4. Simulated device temperature spatial profiles at the turning point (top), indicated by the red dot in the bottom panel of Fig. 3, and at the peak current (bottom), indicated by the blue dot in the bottom panel of Fig. 3, for the case of $V_{BE} = 1.26$ V.

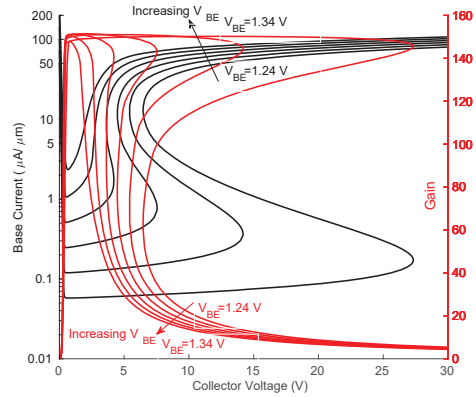


Fig. 5. Simulated I_B (black) and gain (red) vs. V_{CE} curves that correspond to the black solid curves in Fig. 3.

To investigate the impact ionization effect in the HBT, we simulated the I_C - V_{CE} curves using the isothermal DD model with the Plimner II coefficients [16]. As shown in Fig. 6, the I_C - V_{CE} curves also show fly-back behavior using the II model alone. The II induced fly-back is due to competing processes of avalanche carrier generation and standard carrier recombination. However, the fly-back occurs at a much higher voltage for a given V_{BE} , even when the critical fields in the II model were reduced by 25%. In addition, unlike in the SH case where the I_B are always positive (i.e., the electrode provides holes to the device), the I_B values here are negative (i.e., the device supplies holes to the electrode). We note that the II induced fly-back behavior was experimentally measured in InGaP/GaAs HBTs by R. Jin [5].

Using the SH and II models together resulted in the I_C - V_{CE} curves plotted in Fig. 7 for constant V_{BE} . Clearly, the I_C - V_{CE} curves are determined by SH and slightly affected by II when the II critical fields were set to 1.25 times the Plimner values. As the critical fields were reduced to 75%, the I_C - V_{CE} curves (blue) show more fly-backs and fly-forwards than the SH case.

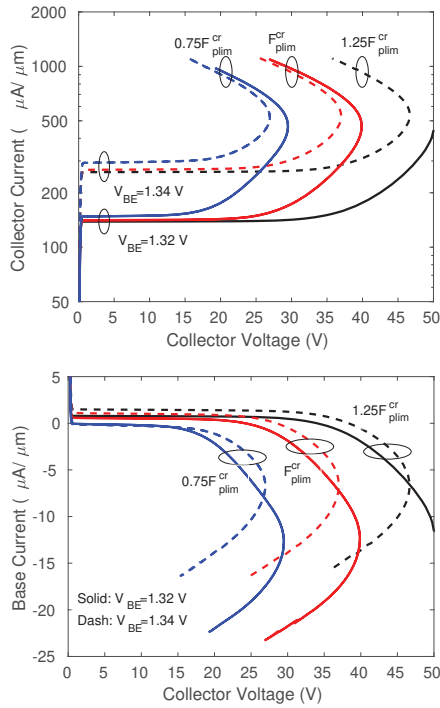


Fig. 6. Simulated I_C (top) and I_B (bottom) vs. V_{CE} under constant V_{BE} , obtained using the isothermal DD model with the Plimmer II parameters. The critical fields in the II model were modified to 1.25 (black) and 0.75 (blue) times the original values (red).

However, when measuring a real HBT, the device would burn out due to SH long before it could reach the second fly-back (II induced). It indicates that the device failure in an InGaP/GaAs HBT under quasi-DC operation is mainly caused by SH and little affected by II.

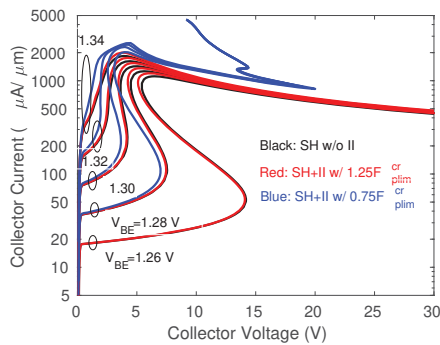


Fig. 7. Simulated I_C vs. V_{CE} curves under constant V_{BE} , obtained using different model configurations. The black curves were obtained using the SH model without II. The red and blue curves were obtained using the SH and II models with the critical fields set to 1.25 (red) and 0.75 (blue) times the original Plimmer values.

IV. CONCLUSION

We have shown the negative slopes of common-emitter output responses in InGaP/GaAs HBTs are not only due to carrier mobility reduction, but more importantly also due to the increased base-to-emitter hole back injection, with increasing temperature. Both SH and II can cause fly-backs in the output responses of HBTs under constant base-emitter voltages. The fly-back behavior are caused by competing processes of carrier recombination and thermal or avalanche induced carrier generation. Device failure under quasi-DC operation is dominated by self-heating because the impact ionization induced fly-back occurs at a much higher voltage.

REFERENCES

- [1] L. L. Liou, J. L. Ebel, and C. I. Huang, "Thermal effects on the characteristics of AlGaAs/GaAs heterojunction bipolar transistors using two-dimensional numerical simulation," *IEEE Trans. Electron Devices*, vol. 40, no. 1, pp. 35–43, 1993.
- [2] A. Kager and J. J. Liou, "Two-dimensional numerical analysis of AlGaAs/GaAs heterojunction bipolar transistors including the effects of graded layer, setback layer and self-heating," *Solid-State Electronics*, vol. 39, no. 2, pp. 193–199, 1996.
- [3] C. P. Lee, F. H. F. Chau, W. Ma, and N. L. Wang, "The safe operating area of GaAs-based heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 53, no. 11, pp. 2681–2688, 2006.
- [4] C. P. Lee, N. G. M. Tao, and B. J. F. Lin, "Studies of safe operating area of InGaP/GaAs heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 943–949, 2014.
- [5] R. Jin, "Sub-nanosecond pulse characteristics of InGaP/GaAs HBTs," Lehigh Univ. Lehigh Pres., Tech. Rep., 2011.
- [6] B. R. Lin, N. G. M. Tao, C. P. Lee, T. Henderson, and B. J. F. Lin, "2D numerical simulation for InGaP/GaAs HBT safe operating area," in *The 9th European Microwave Integrated Circuits Conference.*, 2014, pp. 1–4.
- [7] C. Mukerjee and C. K. Maiti, "Simulation and modeling of self-heating effects in heterojunction bipolar transistors," *J. Basics and Appl. Phys.*, vol. 3, no. 1, pp. 16–25, 2014.
- [8] N. Rinaldi and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: Part I - single-finger devices," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 2009–2021, 2005.
- [9] —, "Theory of electrothermal behavior of bipolar transistors: Part III - impact ionization," *IEEE Trans. Electron Devices*, vol. 53, no. 7, pp. 1683–1697, 2006.
- [10] P. J. Robertson, "HBT compact thermal model," Sandia National Laboratories, Tech. Rep., 2018.
- [11] <https://chiron.sandia.gov/>.
- [12] S. Choi and G. M. P. et al., "Thermal design and characterization of heterogeneously integrated InGaP/GaAs HBTs," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 6, no. 5, pp. 740–748, 2016.
- [13] X. Gao, G. L. Hennigan, L. Musson, A. Huang, and M. Negoita, "Simulation and investigation of electrothermal and dose rate effects in heterojunction bipolar transistors," *submitted to J. radiation effects research and engineering*, 2019.
- [14] W. R. Wampler and S. M. Myers, "Model for transport and reaction of defects and carriers within displacement cascades in gallium arsenide," *J. Appl. Phys.*, vol. 117, no. 045707, 2015.
- [15] G. E. Stillman, V. M. Robbins, and K. Hess, "Impact ionization in InP and GaAs," *Physica*, vol. 134B, pp. 241–246, 1985.
- [16] S. A. Plimmer, J. P. R. David, G. J. Rees, and P. N. Robson, "Ionization coefficients in $\text{Al}_x\text{Ga}_{1-x}\text{As}$ ($x = 0 - 0.60$)," *Semicond. Sci. Technol.*, vol. 15, pp. 692–699, 2000.
- [17] C. Groves, R. Ghin, J. P. R. David, and G. J. Rees, "Temperature dependence of impact ionization in GaAs," *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2027–2031, 2003.
- [18] X. Gao, B. Kerr, and A. Huang, "Analytic band-to-trap tunneling model including band offset for heterojunction devices," *J. Appl. Phys.*, vol. 125, no. 054503, 2019.