Device-to-circuit modeling approach to Metal – Insulator – 2D material FETs targeting the design of linear RF applications

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***Abstract*—We present a physics-based device-to-circuit modeling approach to metal – insulator – 2D material based field-effect transistors (2DFETs). Starting from numerical simulations based on the self-consistent solution of the 2D Poisson and 1D Drift-Diffusion equations, we obtain the electrostatics and current-voltage characteristics of such devices. Then, assuming small-signal operation, a charge-based equivalent circuit is fed with the small-signal parameters computed from the numerical results and then it is implemented in a standard circuit simulator. This framework enables the design and assessment of linear radio-frequency applications based on novel and emergent 2DFETs. The approach has been applied to an experimental MoS_2 transistor by benchmarking the transfer characteristics and then predicting the expected performance of such device as a common-source power amplifier, for instance a power gain of 8.6 dB at 2.45 GHz.**

Keywords*—2D material, drift-diffusion, field-effect transistor, molybdenum disulfide, power amplifier, radio-frequency, small-signal

I. Introduction

Since the emergence of graphene, a wide number of two-dimensional (2D) materials have been experimentally demonstrated in an impressive short period of time [1]. Indeed, some of them have already shown potential as channels in field-effect transistors (FETs), being promising candidates to replace and/or augment conventional CMOS technology in a near future. In this context, it becomes essential to develop a methodology able to interpret the electrical measurements of novel 2D material based FETs (2DFETs), to expedite fast prototyping and enabling the design and assessment of linear radio-frequency (RF) circuits based on such devices.

While physics-based numerical simulations provide rigorous information about the electrical operation of a device, their computational burden is quite demanding even for the evaluation of the DC operation of a single transistor. As a consequence, such approach is out of the question for general AC circuit-level simulations. Much more efficient models or methodologies are thus needed for the design and optimization of circuits based on emergent 2DFETs.

In this work, our proposal is to take advantage of the accuracy and potential of numerical simulations by computing the DC operation of a selected device to later build, under a small-signal approximation, a charge-conserving equivalent circuit able to carry out the AC circuit design (implying its analysis and optimization) in commercial circuit simulators. A schematic description of the methodology proposed is depicted in Fig. 1. We have applied this device-to-circuit modeling methodology to an experimental MoS_2-FET, demonstrating the design of a microwave power amplifier based on such a device.

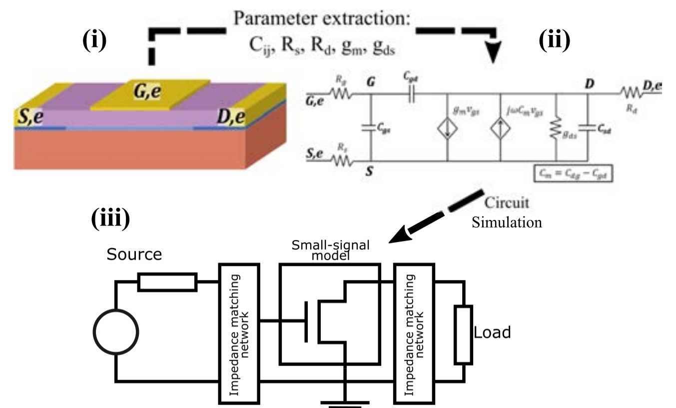

Fig. 1. Schematic description of the approach proposed in this work: from (i) self-consistent simulations of a single device to (ii) the extraction of the small-signal parameters of a charge-based equivalent circuit and (iii) the circuit design, implying its analysis and optimization, in a standard circuit simulator.

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The paper is structured as follows. Section II introduces the numerical self-consistent simulator used to compute the electrostatics and the drain-to-source current. Then, Section III presents the small-signal equivalent circuit used in circuit simulators to describe a 2DFET. Section IV encompasses the comparison of the DC electrical simulations of a MoS_2-FET with experimental measurements together with the design of a power amplifier based on that device. Finally, the conclusions are drawn in Section V.

II. Self-Consistent Simulator of 2DFETs

A. Electrostatics and drain current

The numerical simulation comprises the 2D Poisson equation self-consistently coupled with the 1D Drift-Diffusion (DD) transport equation. Under equilibrium conditions, the electron (hole) density profile, n_L (p_L), is calculated using the 2D density of states. The 2D electron (hole) distribution is obtained combining the longitudinal charge profile with a fixed sinusoidal profile (φ_L) that defines the charge spread along the semiconductor thickness. As emerging 2DFETs suffer from interface traps that degrade the device performance, we have included this effect distributing the trapped charge density in a Gaussian spatial profile along the direction normal to the 2D material – insulator interface. Out of equilibrium, n_L (p_L) is calculated using the 1D DD transport equation which reads as:

$$\begin{aligned} J_n(x) &= qn_L(x)\mu(x)\frac{\partial V(x)}{\partial x} + qD_n\frac{\partial n_L(x)}{\partial x} \\ J_p(x) &= -qp_L(x)\mu(x)\frac{\partial V(x)}{\partial x} + qD_p\frac{\partial p_L(x)}{\partial x} \end{aligned} \tag{1}$$

where J_n (J_p) stands for the 1D electron (hole) current density which is given as a function of position x along the channel (positive x direction is from source, x = 0, to drain, $x = L$; where L is the channel length); V is the potential profile along the 2D channel; D_n (D_p) is the electron (hole) diffusion coefficient; q is the electron charge; and μ is the carrier mobility which has been assumed the same for both type of carriers and dependent on the longitudinal electric field as follows [2]:

$$\mu = \frac{\mu_0}{\left[1+\left(\frac{\mu_0}{v_{sat}}\left|\vec{E}_x\right|\right)^{\beta}\right]^{1/\beta}} \tag{2}$$

where μ_0 is the low-field mobility; v_{sat} is the carrier saturation velocity; β is the saturation coefficient and E_x is the electric field along the longitudinal direction.

B. Charge-based capacitance model

An accurate modeling of the intrinsic capacitances of FETs requires the consideration of any change in the channel charge distribution as a response to the changes of terminal voltages. Thus, once the device electrostatic description is completed, the charge density, $Q_{net} = q(p_L - n_L)$, is integrated along the channel (Q_g) and then split into the drain (Q_d) and source (Q_s) components by making use of the Ward-Dutton's linear charge partition scheme [3], which guarantees charge conservation, as follows:

$$\begin{aligned} Q_g &= -W\int_0^L Q_{net}(x)dx \\ Q_d &= W\int_0^L \frac{x}{L}Q_{net}(x)dx \\ Q_s &= -\left(Q_g + Q_d\right) = W\int_0^L\left(1-\frac{x}{L}\right)Q_{net}(x)dx \end{aligned} \tag{3}$$

In particular, a three-terminal device can be modelled with only four independent capacitances by assuming that the dynamic description is charge-conservative and reference-independent [4]. Each element C_{ij} describes the dependence of the charge at terminal i with respect to a varying voltage applied to terminal j, assuming that the voltage at any other terminal remains constant as follows:

$$C_{ij} = -\frac{\partial Q_i}{\partial V_j} \quad i \neq j \qquad\qquad C_{ij} = \frac{\partial Q_i}{\partial V_j} \quad i = j \tag{4}$$

where i and j stand for g, d, and s.

III. Small-Signal Description of 2DFETs

When electronic devices are employed in analog and RF circuits, their terminals are biased with a DC voltage over which a time-varying signal is superimposed. If the amplitude of that time-varying excitation is small enough, the resulting small current and charge variations can be expressed in terms of it using linear relations. This way a non-linear device can be treated as a linear circuit with conductance, inductance and capacitance elements forming a lumped network [5]. The appropriate small-signal equivalent circuit of a 2DFET is shown in Fig. 2 [4]. It presents two important features: (i) it guarantees charge conservation paying attention to the nonreciprocity of the capacitances and (ii) it includes the metal contact and access resistances, which are of upmost importance when dealing with low dimensional FETs.

Accordingly, our methodology is based on the accurate calculation of the different small-signal elements contained in the equivalent circuit depicted in Fig. 2 with our self-consistent simulator. Specifically, the capacitances are numerically computed by evaluating (3) and (4); the conductances by calculating: $g_m = \partial I_{ds}/\partial V_{gs}$ and $g_{ds} = \partial I_{ds}/\partial V_{ds}$; and the resistances $R_s = R_{s,acc}+R_c$; $R_d = R_{d,acc}+R_c$ are split into the series combination of the access and metal contact resistances, respectively. $R_{s,acc}$ and $R_{d,acc}$ are extracted from the numerical simulations, while R_c and the gate resistance, R_g, are treated as fitting parameters.

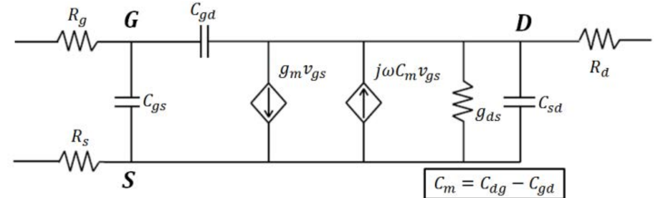

Fig. 2. Charge-based small-signal model suited to 2DFETs. The small-signal elements are: g_m transconductance, g_{ds} output conductance and C_{gs}, C_{gd}, C_{sd} and C_{dg} independent intrinsic capacitances. R_g is the gate resistance and R_d, R_s account for the contact and access resistances of the drain and source, respectively.

IV. Results

A. MoS_2-based FET

In this section, we validate the proposed approach against the measured characteristics of an experimental 2DFET [6]. The device consists of an *n*-type monolayer CVD-grown MoS_2 (length of $L = 450$ nm) deposited on 285-nm thick SiO_2, and covered by a 30-nm thick HfO_2 controlled electrostatically by a metal gate of 250-nm length. We calibrate our simulator by comparing the experimental DC transfer characteristic (symbols) with our simulations (solid line) as shown in Fig. 3. The accurate fit is achieved assuming $R_c = 200\Omega$. Then we extract the intrinsic small-signal parameters, summarized in Table I, for an operation bias point of V_{GS} = -3.9V and V_{DS} = 0.7V corresponding to the saturation regime.

TABLE I. Extracted Small-Signal Parameters of the MoS_2-FET [6]

Element	Value	Element	Value
C_{gs}	13.317 fF	g_m	10.8 mS
C_{gd}	1.745 fF	g_{ds}	0.58 mS
C_{dg}	7.039 fF	$R_{d,acc}$	4.37 kΩ
C_{sd}	-0.415 fF	$R_{s,acc}$	1.04 kΩ

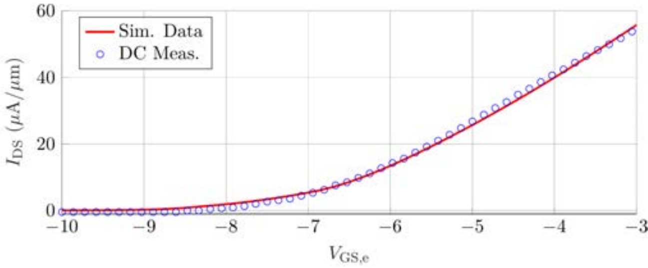

Fig. 3. Fitting of the measured transfer characteristic reported in [6] ($V_{DS,e}$ = 3.5V).

B. Design of a power amplifier based on a MoS_2-FET

Once the device has been thoroughly characterized, the performance of a power amplifier operating at the ISM band is assessed by taking advantage of the Keysight© ADS design tools. The design of the RF linear circuit is based on the MoS_2-FET (described in Section IV.A) but considering an optimized device in which the underlapped access regions have been removed ($R_s = R_d = R_c$). Finally, $R_g = 10\Omega$ is assumed.

First, the main RF figures of merit of the device under test are analyzed; which in turn are the cutoff frequency, f_T, and the maximum frequency of oscillation, f_{max}. f_T stands for the frequency at which the current gain (h_{21}) of the transistor drops to unity and the f_{max} is the frequency at which the power gain (U, Mason's invariant [7],[8]) becomes unity. Such gains are evaluated from the short-circuit admittance parameters as follows [4]:

$$h_{21}(\omega) = -\frac{y_{21}}{y_{11}}$$
$$U(\omega) = \frac{|y_{12} - y_{21}|^2}{4\left(\mathrm{Re}[y_{11}]\mathrm{Re}[y_{22}] - \mathrm{Re}[y_{12}]\mathrm{Re}[y_{21}]\right)} \quad (5)$$

Fig. 4 shows the h_{21} and U of the MoS_2-FET as estimated in the circuit simulator by connecting 50Ω-ports to the gate-source and drain-source terminals of the equivalent circuit depicted in Fig. 2. The maximum stable gain / maximum available gain (MSG/MAG), calculated as in [9], are also shown in Fig. 4. Both U and MSG/MAG becomes unity at the same frequency, f_{max} = 109 GHz. In practice, as a rule of thumb, the operating frequency of the power amplifier should be lower than ~20% of the transistor's f_{max} to guarantee sufficient power gain [10]; thus, the selected design frequency is 2.45 GHZ where a MSG of 19.8 dB is available.

Considering the tradeoff between operating far from the unstable region and getting high power gain, the design of an Input Matching Network (IMN) and an Output Matching Network (OMN) has been carried out to properly adapt the input and output impedances to the source (Z_s) and load (Z_l) impedances, respectively, at the frequency of operation. Fig. 5a shows the schematics of the proposed power amplifier where the OMN and IMN have been included as a network of lumped elements. Table II contains the magnitude of the *S*-parameters after the matching. Fig. 5b shows the input voltage (V_{in}) and the amplified output voltage (V_{out}) when an incident input power (P_{in}) of -20 dBm (small-signal operation) is delivered by the power source. The proposed design results in a power gain of 8.6 dB for a frequency of operation of 2.45 GHz demonstrating its potential application in RF electronics.

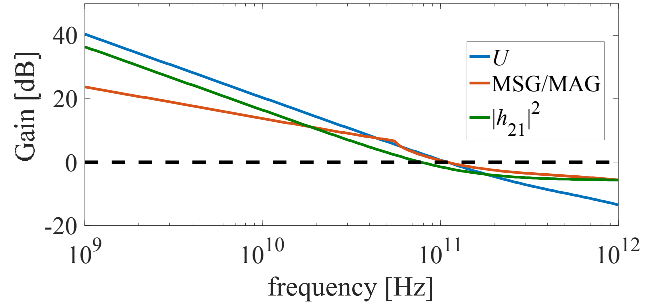

Fig. 4. Radio-frequency performance of the MoS_2-FET under test described by the small-signal parameters provided in Table I. Specifically, the small-signal current gain ($|h_{21}|$), the unilateral power gain (U) and the maximum stable gain / maximum available gain (MSG/MAG) are plotted versus frequency.

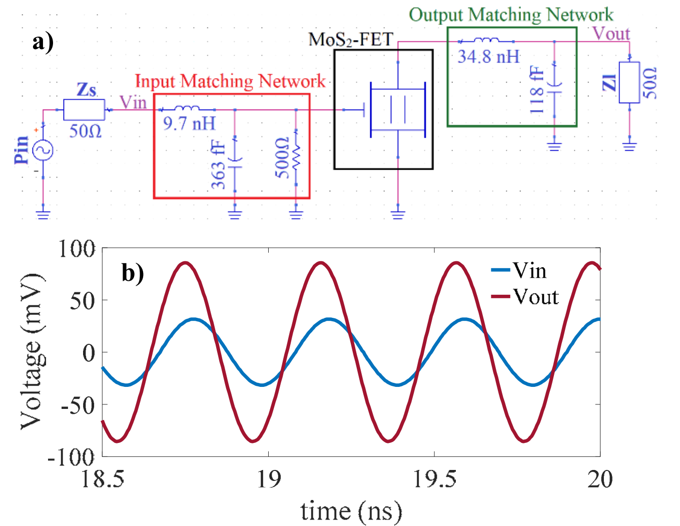

Fig. 5. a) Microwave power amplifier design based on a novel 2D technology. The MoS_2-FET symbol contains the network depicted in Fig. 2 and the small-signal elements described in Table I. b) Input and output voltages showing an amplification of 8.6 dB at 2.45 GHz.

TABLE II. MAGNITUDE (IN dB) OF THE S-PARAMETERS AT 2.45 GHZ AFTER INPUT AND OUTPUT MATCHING

S_{11}	S_{12}	S_{21}	S_{22}
-73.45	-31.03	8.65	-24.54

V. CONCLUSIONS

A device-to-circuit modeling approach to 2DFETs is proposed, allowing the design, optimization and analysis of circuits for linear RF applications. In a first step, the electrostatics and DC current-voltage characteristics of such devices are obtained by means of a robust and accurate self-consistent simulator. Then, a small-signal equivalent circuit suited to 2DFETs is used for circuit simulation feeding its elements with the results achieved in the previous step. The design of a matched power amplifier based on an optimized experimental MoS_2-FET is predicted to operate at 2.45 GHz showing a power gain of 8.6 dB.

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