OFF Current Suppression by Gate-gontrolled Strain in The N-type GaAs Piezoelectric FinFETs

Yuxiong Long[1], Jun Z. Huang[2,*], Zhongming Wei[1], Jun-Wei Luo[1], Xiangwei Jiang[1,†]
[1]Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China, †email: xwjiang@semi.ac.cn
[2]MaxLinear Inc., Carlsbad, CA 92008, USA, *email: junhuang1021@gmail.com

***Abstract*—The gate-controlled compressive strain induced by piezoelectric layers (piezo-layers) is used to suppress the OFF current of n-type GaAs piezoelectric FinFETs (Piezo-FinFETs). Quantum ballistic transport of n-type GaAs Piezo-FinFETs is modeled by the self-consistent Schrödinger–Poisson system. Our results suggest that n-type GaAs Piezo-FinFETs reduce OFF current by an order of magnitude for both high performance and low power applications compared with their counterparts without piezo-layers. The influences of device orientations on device performance is also investigated. The optimal device orientation of n-type GaAs Piezo-FinFETs is on the crystal surface (111).**

Keywords—FinFET, Piezoelectric, Steep slope, strain modulation

I. Introduction

Silicon complementary metal–oxide–semiconductor (CMOS) scaling is approaching its limits, and the reduction of operating voltage (V_{DD}) become very difficult due to the fundamental thermal limit, for which the scaling of subthreshold swing (SS) is limited to 60 mV/decade [1], [2].

Therefore, as a new channel material, the III–V group compound semiconductors is introduced in which the velocity of charge carriers is much higher than in silicon. This would cause a reduction in operating voltage without a loss of performance [3].

However, n-type III-V transistors suffer from a large OFF current (I_{OFF}) leakage as a result of low effective mass. As an intriguing device concept, the Piezo-FinFETs with piezoelectric layers in gate stacks has been proposed to enhance ON current and meanwhile achieve a steeper SS [4], [5]. Furthermore, Piezo-FinFETs can be redesigned by simply changing the piezo-gate voltage to V_{DD} to suppress OFF current and also achieve a steeper SS.

In this work, n-type GaAs Piezo-FinFETs has been studied. The device transport characteristics is obtained by self-consistently solving the open-boundary Schrödinger equation and Poisson equation. An asymptotic waveform evaluation (AWE) technique combined with complex frequency hopping (CFH) is used to speed up the numerical calculation [6]. The influence of device orientations on device performance is also systematically discussed.

II. DEVICE CONCEPT AND SIMULATION APPROACH

A. Device structure

The device structure of n-type GaAs Piezo-FinFETs is shown in Fig. 1. The Fin width is 5nm and channel length is 14 nm. The PZT-5H is chosen as a piezoelectric material in this work, and the piezo-layers have a thickness of 5 nm which can sustain a 0.5 V supply voltage [7]. The piezoelectric layer is placed between the control-gate and piezo-gate. In order to suppress OFF current, the voltage of control-gate equals gate voltage, while the voltage of piezo-gate is set to supply voltage (V_{DD}), so that there is an electric filed applied to the piezo-layers in the OFF-state, and meanwhile the piezo-layers are expanded which causes a large compressive strain to the channel in the OFF-state. Furthermore, this dynamic strain reaches its maximum in the OFF-state. However, there is no strain induced by piezo-layers in the ON-state due to the equal voltage of control-gate and piezo-gate. Therefore, I_{OFF} is suppressed that will be explained next, while I_{ON} remains the same in Piezo-FinFETs compared with their counterparts without piezo-layers.

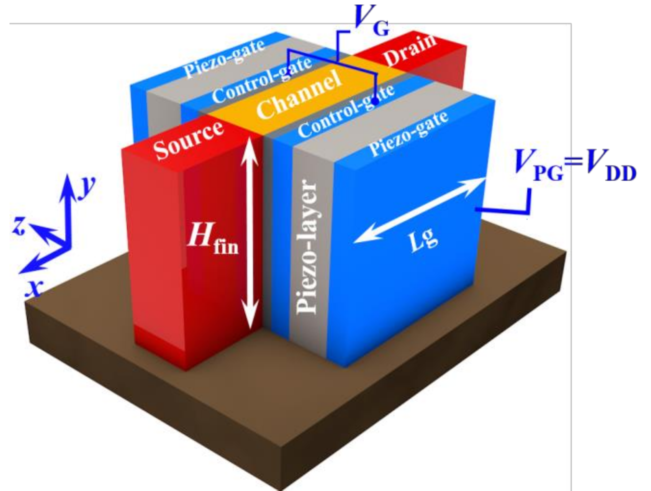

Fig. 1: Device structure of n-type GaAs Piezo-FinFETs. x is the transport direction, y is device height direction, and z is the confined and also periodic direction. The piezo-gate is set to supply voltage V_{DD}.

TABLE I. MATERIAL PARAMETER

Material	Thickness	Elastic compliance constant $\left[\frac{10^{-3}}{GPa}\right]$					Piezoelectric strain constants $[10^{-12}C/N]$
		S_{11}	S_{12}	S_{13}	S_{33}	S_{44}	d_{33}
GaAs	5 nm	11.6	-3.68	Negligible	Negligible	1.67	Negligible
GaSb	5 nm	15.8	-4.94	Negligible	Negligible	23.1	Negligible
PZT-5H	5 nm	16.5	-4.78	-84.5	20.7	4.35	593

B. Simulation approach

Some simplifying assumptions have been embraced in this work [7]: (i) T_{xx}, T_{yy} components have been assumed to be negligible compared to T_{zz} that results in a 1D stress model, because there is no directly applied stress in the x and y directions as shown in Fig. 1; (ii) the device structure repeats

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periodically in the z-axis, so that the outer PE-gates can be assumed to be mechanically firm; (iii) Stress induced by layers is uniformly distributed in the fin region. The 1D stress model is here used for simplicity, and we have previously shown that its results compare fairly well with 3D numerical simulations [7].

The gate tunable stress in the z-axis, T_{zz}, is analytically derived from the principle of piezoelectric effect as shown in Eq. (1) [7], where D→C is the rotation matrix from the Device Coordinate System (DCS) to the Crystal Coordinate System (CCS), and W and S is the abbreviation of width and elastic compliance constant respectively.

The 3D FinFETs structure is simplified to a quasi-2D one to save computation time. To further accelerate the simulation, asymptotic waveform evaluation (AWE) technique combined with complex frequency hopping (CFH) is used in this work. The accuracy and efficiency of this method have been demonstrated by simulation of a triple gate MOSFET in the presence of surface roughness [6]. Moreover, material parameters used in this work are listed in Table I [5], [8].

$$T_{zz} = -d_{33}V_{gs}\left[\frac{1}{0.5W_{fin}R_{D\to C}^{-1}S_{fin}R_{D\to C}+W_{ox}S_{ox,11}+W_G S_{G,11}+W_{pie}S_{pie,33}}\right]$$ (Eq.1).

III. RESULT AND DISCUSSION

A. OFF current suppression

The polarization direction of piezo-layers is chosen to introduce a large compressive strain along the z-axis to the channel in the OFF-state. The variations of gate-controlled stress (T_{zz}) and channel conduction band minimum (CBM) along with control-gate voltage are shown in Fig. 2. It is found that a compressive strain applied to the channel of n-type GaAs Piezo-FinFETs lifts its channel CBM and the variations of both stress and channel CBM reach their maximum in the OFF-sate, namely V_{GS} = 0 V. An upward shift of the channel CBM results in a raise of the top of the barrier for electron injection in the OFF-state, which causes an OFF current suppression.

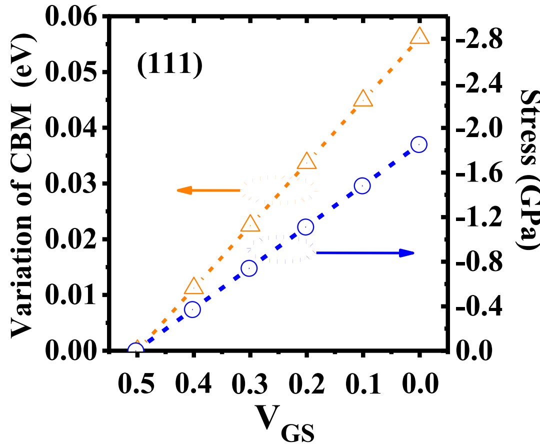

Fig. 2: the variations of stress introduced by piezo-layers and conduction band minimum (CBM) along with control-gate voltages (V_{GS}) for the optimal device orientation on the crystal surface (111).s

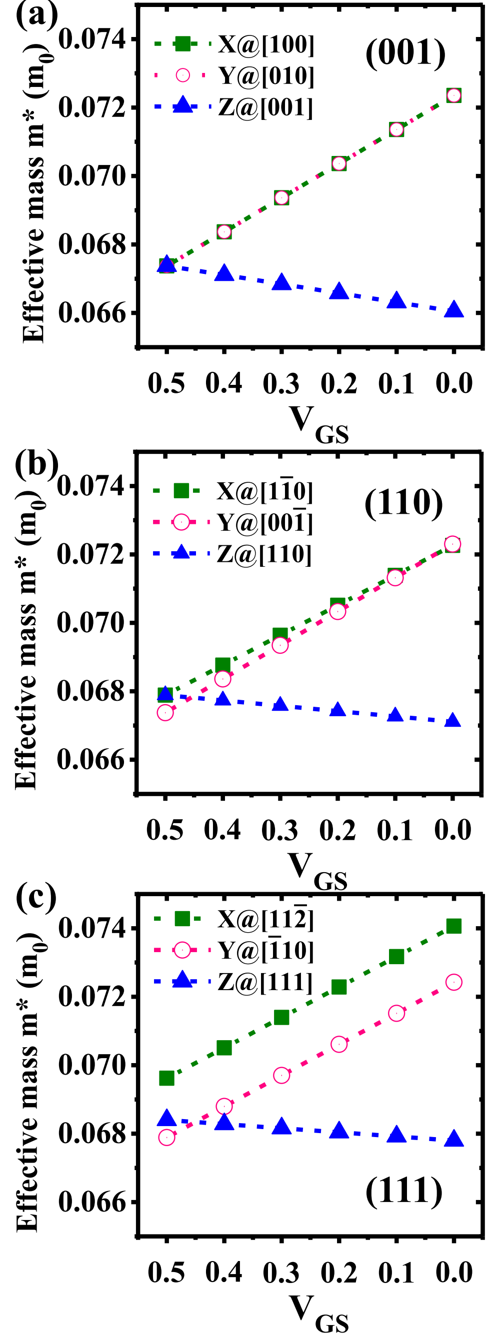

Fig. 3: The dependences on control-gate voltages (VGS) of Effective masses m∗ for different device orientations. (a): (001); (b): (110); (c): (111); Note that (001) means that the channel surface perpendicular to z-axis is the crystal surface (001) and the transport direction is along the crystal orientation [100].

The variations of effective mass (m*) along with control-gate voltages for different surface orientations are shown in Fig.3 (a), (b), and (c), where (001) indicates that the channel surface of n-type GaAs Piezo-FinFETs perpendicular to z-axis is the crystal surface (001), and the transport direction is along the crystal orientation [100]. What's more, the transport effective mass along the x-axis marked by solid green square increases for all three different surface orientations in the OFF-state, which also helps to reduce the OFF-state current.

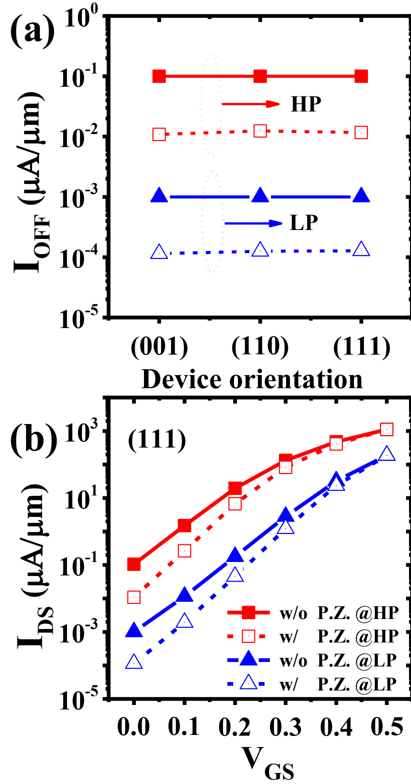

Fig. 4: (a) shows the OFF current of n-type GaAs Piezo-FETs (dash lines) and their counterparts without piezo-layers are compared (solid line). The OFF current of their counterparts without piezo-layers is fixed to 10^{-1} μ A/μm and 10^{-3} μ A/μm respectively for both high performance (red solid lines) and low power (blue solid lines) applications. $I_{DS} - V_{GS}$ curves of n-type GaAs Piezo-FinFETs (dash lines) for both high performance and low power applications are shown in (b), and their counterparts (solid lines) without piezo-layers are also compared. Note that the optimal device orientation on surface (111) is selected.

The OFF current suppression of n-type GaAs Piezo-FinFETs is shown in Fig. 4 (a) marked by dash lines, where the OFF current of their counterparts without piezo-layers is marked by solid lines and targeted at 10^{-1} μA/μm and 10^{-3} μA/μm respectively for high performance (HP) and low power (LP) applications.

Our results suggest that the n-type GaAs Piezo-FinFETs reduce the OFF current by an order of magnitude for both high performance and low power applications. The corresponding I_{DS}-V_{GS} curves are drawn in Fig. 4 (b) for the optimal device orientation on surface (111). It is obviously observed that n-type GaAs Piezo-FinFETs results in a large reduction of I_{OFF} and meanwhile a steeper SS.

B. Device orientation dependence

The subthreshold swing of n-type GaAs Piezo-FinFETs for different device orientations is shown in Fig. 5, where (a) is for high performance applications and (b) is for low power applications, and their counterparts without piezo-layers are also compared. The device orientation on surface (111) has the smallest SS for both HP and LP applications due to its largest transport effective mass shown in Fig. 3. However, n-type GaAs Piezo-FinFETs for LP applications suffer from a larger degradation of SS than for HP applications, and the SS improvement of n-type GaAs Piezo-FinFETs for HP applications is larger than for LP applications. Our simulations suggest that n-type GaAs Piezo-FinFETs achieve about 14 *mv/decade* SS improvement for HP applications and 10 *mv/decade* SS improvement for LP applications in the optimal device orientation on surface (111). Moreover, the influence of device orientations on OFF current is not so obvious.

IV. CONCLUSION

Piezo-FinFETs has been redesigned by simply changing the piezo-gate voltage to V_{DD} to introduce a large compressive into channel in the OFF-state. This gate-controlled compressive strain induced by expanded piezoelectric layers lifts channel conduction band edge and meanwhile increases the transport effective mass in the OFF-state, which suppresses the OFF current and meanwhile improves the SS of n-type GaAs Piezo-FinFETs. Our results show that n-type GaAs Piezo-FinFETs achieve an OFF current reduction by an order of magnitude and a SS improvement by 14 *mv/decade*. The device orientation on surface (111) has the smallest SS, While the influence of device orientations on I_{OFF} is very small.

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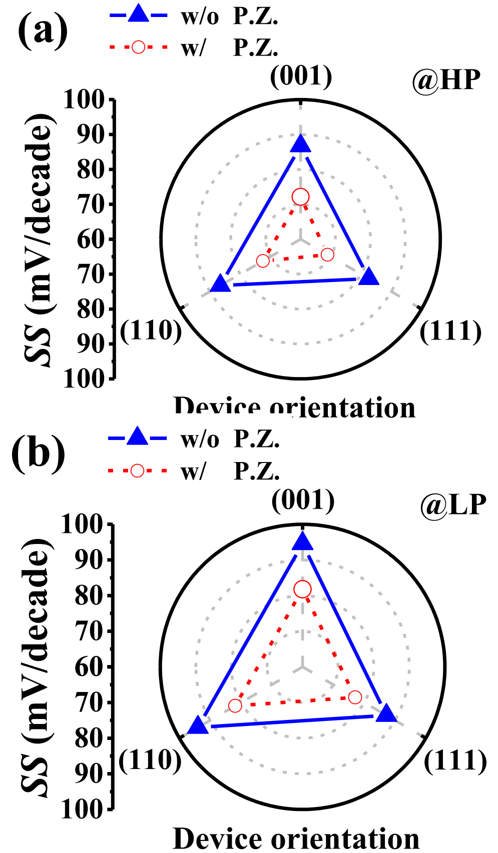

Fig. 5: The subthreshold swing (SS) of n-type GaAs Piezo-FinFETs (red empty circle) and their counterparts without piezo-layers (blue solid triangle). (a): for high performance applications; (b): for low power applications.

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