A New Computer-Aided Calibration Technique of Physics Based IGBT & Power-Diode Compact Models with Verilog-A Implementation

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***Abstract*—In this work, we present a new calibration technique of an IGBT and power diode compact model using a commercially available tool optiSLang™ [1]. We show that with such a computer-aided technique, we can get a accurate match in switching transients just by calibrating the static (transfer and output characteristics) and the gate charge curves. Furthermore, we present a Verilog-A implementation of a physics based IGBT and power diode compact model [2,3]. We demonstrate the benefits of a Verilog-A model by comparing the run time and convergence performance with a standard SPICE implementation.**

***Index Terms*—Verilog-A, compact-model, IGBT, power-diode, computer-aided calibration**

I. Introduction

It is often said that a model is only as good as its calibration. Hence, it is equally important to have a good calibrated model as the quality of the model itself. Compact model calibration can be a time consuming process. Manual calibration can be prone to error and also time consuming, often requiring multiple iterations. Computer aided techniques are therefore preferred to reduce manual effort and to ensure quick turnaround time. There are several approaches to this problem using Python, Matlab or other programming languages with varying levels of ease of use and final fit quality [4,5,6].
In this work, a new calibration technique is presented using a commercially available optimizer called optiSLang™ [1]. It supports the following optimization/evaluation routines:

1) Sensitivity analysis
2) Multi objective optimization
3) Robustness evaluation
4) Reliability analysis
5) Robust design optimization

In this work, we only use the first two routines. This tool, once set up as a template, is very easy to use. This can be useful when there are a lot of similar calibration tasks that need to be performed. optiSLang™ can be set up to launch a full set of simulations on circuit simulators like SIMetrix or PSpice depending on the objective criterion and the parameter input range. It can then iterate to a set of parameters which gives the best fit to the target curves.

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II. Verilog-A model Implementation

The Verilog-A compact model developed for this work is based on an existing sub-circuit SPICE model [1,2]. The Verilog-A model uses the same model equations for physical descriptions and parameters are identical or equivalently expressed as in the sub-circuit model. Consequently, this implementation produces the identical results as the sub-circuit SPICE model. This is illustrated in the next sub-section.

The physics-based IGBT and power diode models are based on the analytical solution of the one dimensional drift-diffusion equation. In this way, the model achieves acceptable run time in circuit simulations and at the same time ensures a short model development cycle. Since diodes are highly symmetrical in layout and vertical design, a single 1D layout is sufficient. For IGBTs, the description of the MOS capacitances accounts for 2D effects as well. Gauss's law is used to describe capacitive currents and charges including the p-n junctions. Once the electrostatics are defined, the drift-diffusion equation is solved to calculate the current densities.

In the sub-circuit model, auxiliary circuits are used to solve for the dynamic base charge, base resistance, space charge width etc. This results in a complex circuit description of the model equations. The Verilog-A implementation does not use auxiliary circuits. This results in a significant reduction of internal nodes.

A. Advantages of Verilog-A over SPICE

Verilog-A has been the modeling language of choice for compact model developers in the recent past. This is primarily because of the fact that it has many significant advantages over sub-circuit SPICE model implementation. Verilog-A provides advanced features like looping, conditional statements, arrays and much more. We have exploited this advantages of Verilog-A to have a faster running and better converging model.

Example of junction-width calulation

To illustrate the benefit of Verilog-A in solving implicit equations, here we show the example of the calculation of the p-n junction width (x_j) as it is applied to the diode and IGBT models.

$$x_j(V_j, x_j) = \frac{\Big((V_j - f(x_j)\Big) + x_j f'(x_j)}{f'(x_j)} \tag{1}$$

where $f(x_j)$ is given by equation (2) below and $f'(x_j)$ is the symbolic differentiation of $f(x_j)$.

$$f(x_j) = \int_0^{x_j} \Big(E(x_j) - E(z)\Big) dz \tag{2}$$

where $E(z)$ is the electric field. Equation (1) results from the approximate Taylor's series expansion (cut off after first derivative) of equation (2). It can be seen that the junction width x_j is an implicit equation depending on the voltage V_j across the space charge region and itself. In our SPICE model, the junction width needs to be evaluated using a self-iterating auxiliary circuit as shown in Fig. 1. This may lead to typical convergence problems in transient simulations. In Verilog-A, we can solve such a problem with a simple Newton-Raphson's algorithm using a do-while loop or as an implicit contribution statement as shown in equation (3).

$$V(x_j) \quad : \quad V(x_j) \quad == \quad f(x_j) - V_j \tag{3}$$

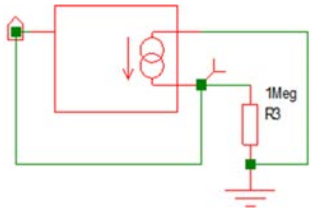

Fig. 1. Self-iterating circuit used for junction width calculation.

This results in less number of circuit equations and hence lower number of iterations are needed to reach convergence in case of Verilog-A as shown in Table I. Due to the lower number of circuit equations less transient/total iterations are needed for the full simulation. This results in a much faster run time with Verilog-A as shown in the following section.

TABLE I
NUMERICAL ITERATIONS AND CIRCUIT EQUATIONS.

	Sub-circuit	*Verilog-A*
Total iterations	4224	2009
Transient iterations	2331	1989
Circuit equations	155	30

B. Comparison with SPICE sub-circuit model

A simple chopper circuit shown in Fig. 2 was simulated to capture the collector current and collector-emitter voltage with respect to time during switching events. As shown in Fig.3, the results from Verilog-A (dashed line) and sub-circuit model (solid line) simulations are almost equivalent.

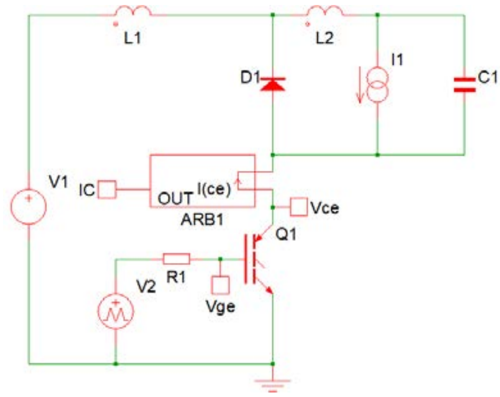

Fig. 2. Schematic of a chopper circuit used as an example.

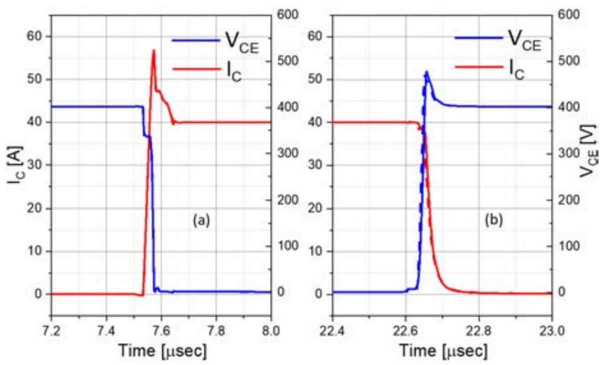

Fig. 3. Comparison of SPICE and Verilog-A simulation output in a chopper circuit (a) turn-on (b) turn-off

Minor differences come from the fact that Verilog-A uses a true time differential operator (ddt), whereas in the sub-circuit model, a resistor-capacitor network is used as an equivalent differentiator circuit. We now compare the run time of sub-circuit versus Verilog-A in Table II for different time steps in the same chopper circuit. As explained in the previous section, the reduced number of circuit equations results in much faster run time in Verilog-A. The speed differences are more noticeable for smaller time steps (<= 10ns).

TABLE II
COMPARISON OF RUN-TIME BETWEEN SUB-CIRCUIT AND VERILOG-A

	Sub-circuit	*Verilog-A*
300 ns time step	3.62 sec	0.78 sec
20 ns time step	4.48 sec	1.98 sec
10 ns time step	33.2 sec	5.05 sec

III. COMPUTER-AIDED CALIBRATION

A. Methodology

In a first step, we fit the static transfer and output characteristics for the IGBT and the forward characteristic for the diode at two different temperatures. Further, we use the best-fit IGBT model from this stage to calibrate the gate-charge

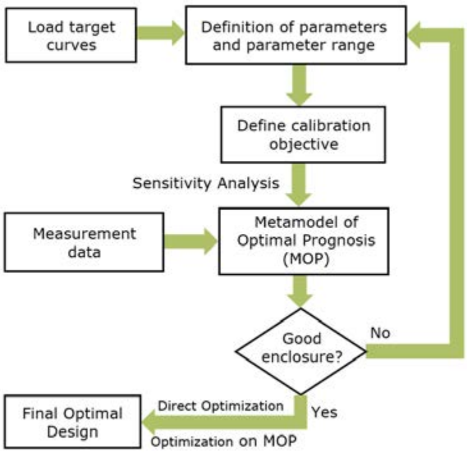

Fig. 4. Algorithm for the calibration methodology.

curve from transient simulations. The simulations are done in a commercially available circuit simulator supporting Verilog-A. Such a simulator can be easily coupled to optiSLang™ using windows command line interface. optiSLang™ designs the simulation runs, calls the simulator for the simulations, then reads back the results and thereafter tweaks the parameters and launches further set of simulations.

The overall process is summarized in a flow-chart in Fig. 4 and will be explained further on for the IGBT model. In the first stage, the compact model parameters to be optimized are identified in the model and their initial range of variation are determined. The target curves are divided into multiple segments (10-12 for our example) of equal length. The optimizer fits each of these discrete segment together in parallel. This approach has two advantages. Firstly, the segments of the target curves (measurements) where a good fit is important (for example threshold region in transfer characteristic) are identified and can be weighted higher if a higher accuracy is needed in that region. Secondly, as we will see later, this results in a meta-model of the system where each segments dependence on each parameter can be visualized in a convenient way.

In the next stage, the criterion for the optimization is defined. We use a quadratic difference method to compare the reference and simulation results. This method is basically the summation of the squared differences between each segment of the reference and simulation curves. The optimizer is then tasked to minimize this quadratic difference. A zero difference would mean that the target and simulations are overlapping.

B. Sensitivity analysis and meta-model generation

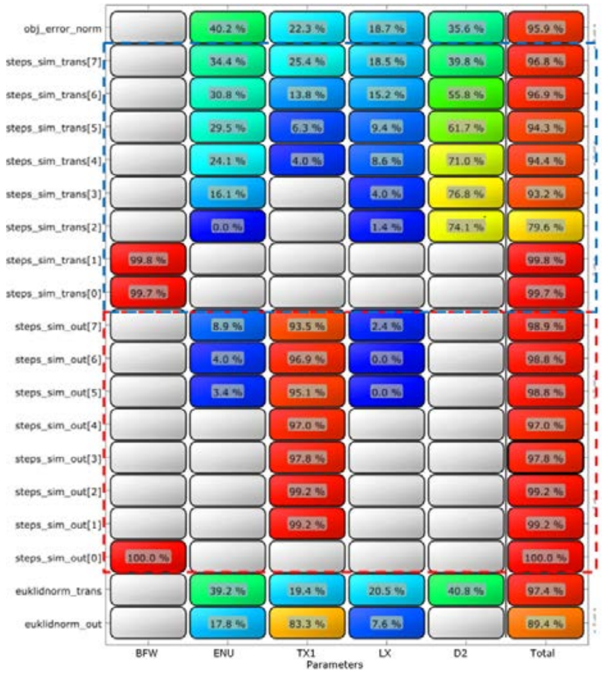

Fig. 6. Meta-model generated after the sensitivity analysis.

At this stage, the tool has all the required information about the reference curves and the compact model parameters to be optimized. The optimizer now does a sensitivity analysis to evaluate the dependence of each parameter on each section of the target curve. The number of total simulation runs are decided on the number of parameters varied and their

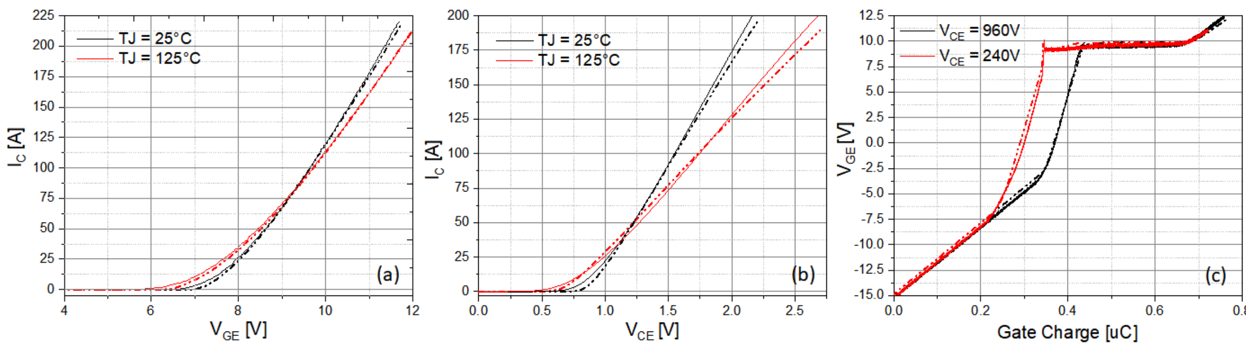

Fig. 5. Comparison of simulated and measured curves after final fit (a) transfer (b) output and (c) gate-charge characteristics.

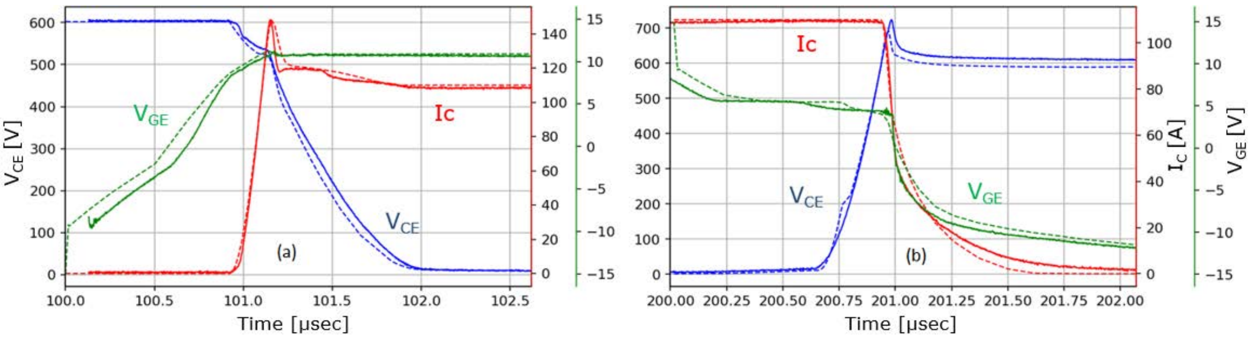

Fig. 7. Comparison of simulated and measured switching transient curves after final fit (a) turn-on (b) turn-off.

variation range. The optimizer can run a set of simulations, analyze the difference between the curves and then launch further simulations in the range where it estimates the objective criterion will be even lower.

As a result of the sensitivity analysis, a meta-model of prognosis (MoP) is created. This meta-model can be visualized as shown in Fig. 6. The five parameters being varied are on the x-axis and the discrete segments (0 being the first segment of the reference curve and 7 being the last) of the transfer and output curves are on the y-axis. The impact of each parameter on each segment of the target curves is shown with a color plot with red being the highest impact and blue the smallest. For example, parameter D2 has a strong impact in segments 2 to 4, which is the threshold region of the transfer curve. Greyed boxes have zero impact. The last two rows summarize this contributions into an overall score for the transfer and output characteristics. A higher score implies a higher confidence of the optimizer in representing the simulated curve.

Various steps can be taken to improve the overall score before going to the final optimization stage. This steps include, removing simulations from the design which have large deviation from the reference, redefining the parameter ranges or removing some parameter dependence from the system. The optimizer may also automatically neglect a certain parameter if it has negligible impact on the target curves. The tool checks if the family of performed simulations has a full enclosure of the target curve. If not, this would mean the parameter ranges were not correct to begin with. In this case, the sensitivity has to be repeated with corrected ranges until full enclosure is achieved.

C. Final optimization and best fit

In the final stage, a further optimization step is done. This can be achieved in the following two ways.

Direct optimization: Direct optimization method would run further simulations in a smaller or same parameter range using the best result of the sensitivity stage as a starting point.

Optimization on MoP: MoP optimization on the other hand, does not need to run new simulations. Instead, it uses the meta-model created from the sensitivity stage to evaluate a best combination of parameters, which results in the best fit of the simulation data to the measurements.

The final stage then gives the best-calibrated model to the reference curves. The results of the optimization process can be seen in Fig. 5 for (a) transfer (b) output and (c) gate-charge characteristic simulations (dashed line) compared to measurements (solid lines). With this best-fit model, we now check the transient switching behavior of the IGBT with a free wheeling diode. Fig. 7 shows that after such an optimization process, even switching transient simulations (dashed line) fit very well to measurements (solid line). This proves the quality of the physics based model approach.

IV. Conclusion

We have demonstrated a new computer-aided calibration technique applied to physics based compact models for IGBTs and power diodes. Just a good calibration of the static curves and the gate-charge curves leads to excellent match with measurements in switching transients as well. In addition, we have shown how Verilog-A compact models can significantly improve the run time and convergence over sub-circuit models.

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