Simulation of deep level transient spectroscopy using circuit simulator with deep level trap model implemented by Verilog-A language

Koichi Fukuda
National Institute Of Adivanced Industrial Science and Technology (AIST)
Tsukuba, Japan

Junichi Hattori
National Institute Of Adivanced Industrial Science and Technology (AIST)
Tsukuba, Japan

Hidehiro Asai
National Institute Of Adivanced Industrial Science and Technology (AIST)
Tsukuba, Japan

Mitsuaki Shimizu
National Institute Of Adivanced Industrial Science and Technology (AIST)
Tsukuba, Japan

Tamotsu Hashizume
Research Center for Integrated Quantum Electronics (RCIQE)
Hokkaido University
Hokkaido, Japan

***Abstract*— A modeling method of deep level transient spectroscopy (DLTS) using circuit simulation with a MOS capacitor compact model which takes into account influences of deep level traps is proposed. In the proposed method, DLTS measurement procedures are described by transient analysis of circuit simulation. Stable numerical convergence is obtained even for the case in which carrier traps with wide range of time scales are included. Through case studies, it is proved that this method is a robust and versatile theoretical tool to predict DLTS signals, which helps to understand DLTS results and to optimize DLTS measurement conditions. Furthermore, the method is applied to several capacitance measurement methods discussed in literatures concerning GaN MIS capacitors, which ensures the practical ability of the proposed simulation approach.**

Keywords—deep level transient spectroscopy, circuit simulation, compact model)

I. INTRODUCTION

Deep trap levels are still a major issue for power devices [1] and also a major technical barrier for two-dimensional materials [2]. Identification of trap species is important in order to overcome these deep trap level problems. Among various trap measurement methods, deep level transient spectroscopy (DLTS) is one of the most detailed physical measurement methods for traps [3]. Using DLTS, it is possible to separate out the information of traps with energy distributions and different time constants. On the other hand, quantitative modeling of the DLTS measurement is a problem in which various traps with a wide range of time constants are obstacles and therefore it is difficult to make them converged even using numerical simulation, and a versatile theoretical tool is strongly required. Recently, the authors used circuit simulation as an analysis tool of MOS capacitors containing various traps by implementing the physical behavior of traps in the Verilog-A language [4]. In this paper, a simple DLTS modeling approach using the circuit simulation with the MOS capacitor model is proposed, and its usefulness is shown through simulation case studies.

II. SIMULATION METHOD

The circuit simulation used for DLTS modeling utilizes the compact model of a MOS capacitor in which the influence of trap levels is taken into account [4]. In-side the compact model implemented using Verilog-A language [5], Poisson equation, current continuity equations, and one rate equation for each trap species are solved self-consistently by an iterative method for a time step given by the circuit simulator. The rate equation for each trap is as in (1),

$$\partial N_{TA} / \partial t = E_n N_{TA}^- - C_n n (N_{TA} - N_{TA}^-) \qquad (1)$$

where N_{TA} and N_{TA}^- are total and negatively charged acceptor-like traps, C_n is the electron capture rate, n is the electron concentration, and E_n is the electron emission rate as in (2),

$$E_n = \nu_{th} \sigma_n N_C \exp(-\Delta E / k_B T) \qquad (2)$$

where ν_{th} is the thermal velocity σ_n is the capture cross section, N_C is the effective density of states of the conduction band, and ΔE is the trap energy depth from the conduction band.

The schematic explanation of the trap dynamics is shown in Fig. 1 in which an example of acceptor type trap is explained. The acceptor trap fastly captures an electron and is negatively charged, but the captured electron is slowly emitted by obtaining the thermal energy corresponding to the energy depth from the conduction band. The negatively charged acceptor trap fastly captures a hole and becomes neutral charge condition. The equation (2) shows that the time scale of the trap behavior strongly depends on the trap energy depth. These set of equations are created for each trap, and solved self-consistently all in one device instance of the circuit.

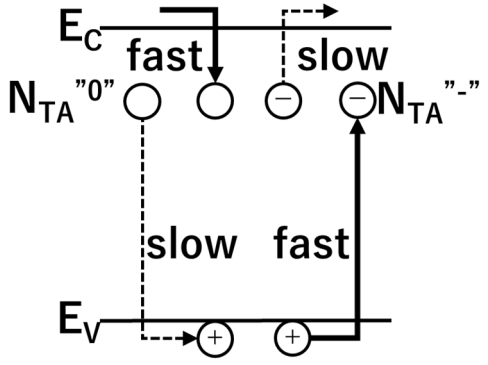

Fig. 1. A schematic explanation of the dynamics of the acceptor-like traps.

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The circuit simulator controls the time steps and manages the Newton convergence including the consistency with the other components of the circuit. This nested algorithm is shown as a flowchart-like viewgraph in Fig. 2. Poisson equation, carrier continuity equation and rate equations for each trap species are solved by decouple iterations in order to obtain the self-consistent solutions of all equations. The time step discretization is treated by the implicit method. The self-consistency with all other circuit components is automatically ensured by the convergence loop of SPICE. The Newton Jacobian matrices are automatically created by the Verilog-A language system.

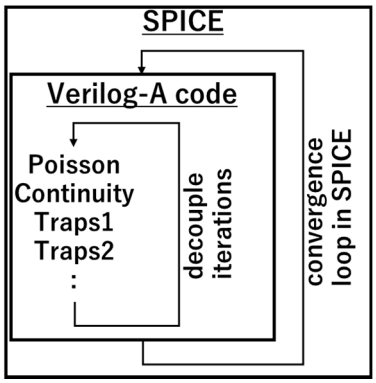

Fig. 2. A flow-chart like viewgraph of the proposed and implemented method. Poisson equation, carrier continuity equations, and rate equations of various traps are self-consistently solved in the internal decouple iterations written by Verilog-A language. The time steps are controlled by SPICE convergence loop governed by Newton-Raphson method.

All circuit simulations for *C-V* measurements and DLTS measurements are performed as transient mode analyses as shown in the schematic viewgraph Fig. 3. The control of time-dependent voltage is described in the input deck of the circuit simulator, and in particular, each capacitance measurement is performed by giving sine-curve signals with the given amplitude and frequency. The signal part of the simulation input deck can easily be obtained by using a shell script or a small program. The capacitance values are obtained from the time dependent gate currents which include time dependence of carrier concentrations in the semiconductor, trap charges at the insulator semiconductor interface, and also the displacement currents arising from the sinusoidal input voltages. Additionally, when the conversion is obtained for each time step, electron and trap charges are output to the standard output of the program, controlled by Verilog-A systems. This helps to differentiate the displacement current of the gate bias and charge current in the semiconductor. It should be mentioned that time steps differ by orders of magnitude depending on the input deck and conversion status, which is well managed by SPICE time step control. Compared with device simulation approach as in [6], input deck for circuit simulation is much simpler, because the purpose of the simulation is well focused.

III. Results and Discussions

A. A case study.

Fig. 4 shows the assumed GaN MOS capacitor with n-type substrate dopant density of 6.2×10^{16} /cm^3 and with acceptor type traps at the semiconductor-insulator interface. Two cases of assumed energy distribution of trap densities are shown in Fig. 5. Both cases consist of three density peaks at the energy depth from the conduction band of 0.2, 0.4, and 0.6 eV. For each peak, the accumulated trap density is 2×10^{12} /cm^2, which results in 6×10^{12} /cm^2 for each case. The difference of these two cases is the standard deviation of the trap energy, 10 and 40 meV for each peak. The circuit simulation is performed with Silvaco SmartSpice [7].

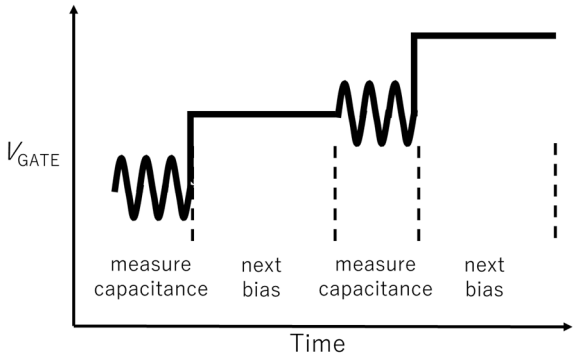

Fig. 3. Schematical description of time dependent bias control for both *C-V* and DLTS measuremets. Both are simulated by full transient analysis mode of the circuit simulator. Gate voltage is controlled through SPICE input decks.

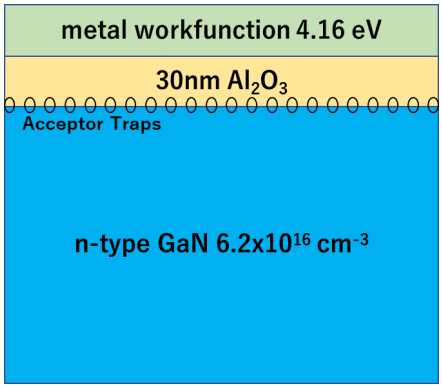

Fig. 4. Assumed device structure of GaN MOS capacitor with deep level traps at the semiconductor insulator interface.

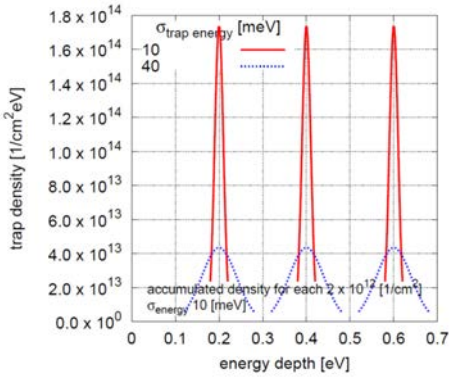

Fig. 5. Two trial cases of trap density energy distribution for demonstration. Three peaks at the energy depth of 0.2, 0.4, and 0.6 eV with accumulated trap density of 2 × 1012 /cm2 for each peak. Two cases are different in standard deviation of the trap energy, 10 and 40 meV.

Fig. 6 shows the C_G-V_G characteristics of assumed two cases for frequency of 1 MHz. Although the difference in energy distribution in these cases affects the *C-V* characteristics, the difference is minor and it might be difficult to determine the difference in the actual measurements. Fig. 6 shows the DLTS signal for these two cases. The DLTS signal is the difference of 1 MHz capacitance at 1 msec. and 10 msec. after the gate bias is changed from the initial gate bias of 3 V to the target gate bias of -1.5 V. In the case of energy standard

deviation of 10 meV, three peaks corresponding to 0.2, 0.4, and 0.6 eV are clearly observed, but for the case of 40 meV, the peaks for 0.4 and 0.6 eV are ambiguous. As easily imagined from the examples, the proposed method is an optimal tool to optimize the detailed measurement conditions.

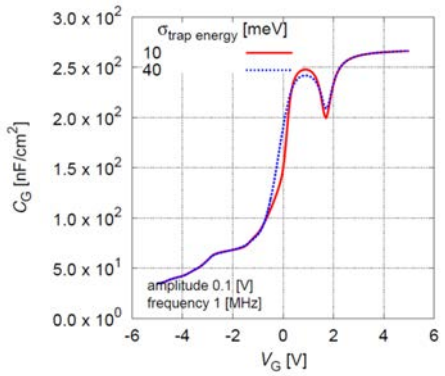

Fig. 6. *C-V* curves obtained for the two cases in Fig. 5. The frequency is 1 MHz. The circuit simulations are well converged even for trap energy distribution with wide range time scale.

B. Comparison with the literature

Comparison with experimental values in the literature is important to verify the usefulness of this method. We will focus on the article on GaN in particular as a semiconductor with various applications in the near future and suffering from trap behavior. In particular, Nakano and Jimbo have shown detailed and respectable measurement results regarding the GaN MIS structure [8], and we confirmed the usefulness of this method by simulating their conditions. The metal is Al, the insulator is sputtered 100 nm SiO_2, and the GaN is n-type with 6.8×10^{17} /cm^3 confirmed by secondary ion mass spectrometry.

They combined several measurement methods to characterize the MIS interface traps, the conventional *C-V*, the pulsed *C-V*, transient capacitance *C-t*, and deep level transient spectroscopy DLTS. Fig. 7 is the pulsed *C-V* curves for several delay time td conditions. The pulsed *C-V* is used to evaluate time dependence of charging and discharging at the SiO_2 / GaN interface.

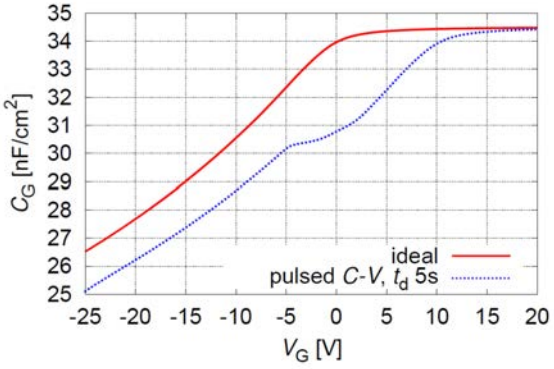

Fig. 7. Pulsed *C-V* characteristics for delay time of 1s, 5s discussed in [8]. The ideal *C-V* curve is also shown for comparison. This measurement is used to evaluate time dependence of charging and discharging at the SiO_2 / GaN interface.

Fig. 8 shows temperature dependence of measured *C-t* curves using transient capacitance measurement method as described in [8]. The method is used in order to examine the capacitance transient observed in deep depletion. The relaxation time for both capacitance transients becomes shorter in accordance with the rising of the temperature, which is in reasonable agreement with the theory of thermal carrier emission based on the Shockley–Read–Hall statistics, as discussed in [8]. Three types of traps are identified in [8], however detailed energy peak information is not available. In the simulations, three energy peaks of 0.55, 0.77 and 0.9 eV are assumed for trial. By comparing simulation results and measured results, it is possible to discuss more detailed information of the energy distributions of the interfacial traps. In addition, a capacitance transient with a fast relaxation time of 10^{-5} s is observed in the *C-t* curves at temperature higher than 330 K.

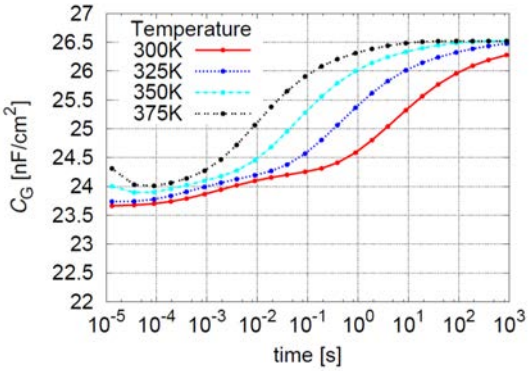

Fig. 8. Simulation results of temperature dependence of *C-t* curves for target V_G of -25 V obtained by the capacitance transient measurement method configured as in [8].

Fig. 9 shows the simulated DLTS curves for several t_1 / t_2 configurations of measurements in [8]. The detailed discussions of these dependences are realized by the present theoretical method ensured by sufficient accuracies of the simulations. The rate windows t1 (ms) / t2 (ms) = 4 / 8, 5 / 10, 8 / 16, and 10 / 20 correspond to the emission rates of 173, 139, 87, and 69 s^{-1}. The peak shift depending on the rate window enables the Arrhenius plot and the activation energy is extracted as 0.77 eV. In [8], other two peaks are also discussed but no detailed information is described. Therefore, only the main trap energy peak of 0.77 eV is assumed with accumulated trap area density of 2.2×10^{12} cm^{-2}.

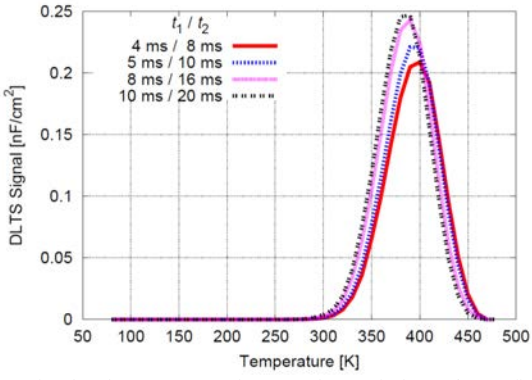

Fig. 9. Simulated DLTS curves for several rate window t_1 / t_2 configurations of measurements in [8]. The peak shift depending on the rate window include the information of the activation energy of the interface trap.

For the comparison to published measurement results, the proposed method covers not only the conventional C-V measurement, but also pulsed C-V measurements, transient C-t measurements, and DLTS measurements for MIS capacitors in order to characterize interface traps. These simulation

conditions can be managed changing only the transient input voltage sequences in the input deck of the circuit simulator SPICE. Through the simulation according to the configurations in [8], practical ability of the present method is sufficiently confirmed, and therefore it is expected that the method helps to overcome the trap issues in coming generation of novel semiconductor materials.

IV. Conclusions

The modeling method of deep level transient spectroscopy by circuit simulation is demonstrated which uses the compact model of the MOS capacitor considering the influence of the deep level traps. In the method, Poisson, carrier continuity equations and rate equations for all traps are self-consistently solved by the decouple method for one time-step of circuit simulation, which is implemented using Verilog-A language. All the measurement procedures are described by the transient input deck of circuit simulations. Through the case study, it has been verified that the *C*-*V* measurements, not only the conventional method but also the several types of methods, and the temperature dependence of the DLTS signals can be stably obtained. Influence of subtle differences in the trap level density distribution is quantitatively predicted. It is proved that this method is a strong theoretical tool of DLTS signals to optimize and to understand the measurements, and therefore it helps to overcome the trap issues which block to realize applications of novel semiconductor materials.

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