Electro-Thermal Analysis and Edge Termination Techniques of High Current β-Ga_2O_3 Schottky Rectifiers

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***Abstract*—The performance and limitations of β-Ga_2O_3 Schottky rectifiers is studied via simulation using the Florida Object Oriented Device and Process (FLOODS) TCAD simulator. The effect of forward bias and power is examined for various bulk and epitaxial layer thicknesses as well as for heat sink geometries. Thicker bulk/substrate results in higher maximum temperature values whereas a thinner epitaxial-layer results in higher forward currents and hence a higher maximum temperature values via Joule heating. A Cu finned heat sink geometry results in a 26.76% reduction in the maximum temperature. Edge termination techniques are examined for β-Ga_2O_3 Schottky rectifiers in order to maximize the breakdown voltage, identify the location of breakdown and mitigate the maximum electric field. Best results have been observed for Al_2O_3 as the dielectric material in a field-plate structure while the effect of field-plate dimensions is also studied.**

Keywords—Gallium oxide, semiconductors – II-VI, Rectifiers, electro-thermal, edge-termination

I. Introduction

Gallium oxide has recently emerged as the prime candidate for applications in power electronics due to its large bandgap, high electric breakdown strength, low on-resistance and low charge storage times [1][2][3]. The suitability of semiconductors as electronic power switches is evaluated by calculating various figure-of-merits (FOM). The large bandgap (~4.85 eV) of Ga_2O_3 translates into a high breakdown field (E_{br}) creflected by a high Baliga's figure-of-merit which is about 4-7 times higher than that for SiC, leading to lower conductance losses at a low manufacturing cost in comparison to 4H-SiC diodes [4]. Notably, the electric field breakdown strength (E_{br}) of Ga_2O_3 is more than double the theoretic limits of SiC and GaN.

Schottky rectifiers have been adopted for power electronics applications due to its fast switching speed, which is required to improve the efficiency of inductive motor controllers and power supplies [5][6] as well as low forward voltage drop and high-temperature operability. Along with the high E_{br}, Ga_2O_3 also possesses an on-state resistance value of over 10 times larger than conventional Si rectifiers.

An ongoing issue with Ga_2O_3 is its thermal conductivity (21 W/m.K) [7][8], which is an order of magnitude lower than its commercial counterparts, i.e. SiC and GaN. Recent studies [9][10][11] performed on vertical Schottky rectifiers have achieved high forward-currents and high breakdown voltages, due to the rapid progress in the epitaxial growth methods. These studies focus on the realization of large dimension devices; hence it is important to understand the rise and inefficient dissipation of heat from the channel resulting in a degradation of electron transport properties. The thermal properties of Gallium oxide devices have been studied recently with a focus on thermoreflectance-based thermography and imaging of Ga_2O_3 Schottky diodes [4][12], Ga_2O_3 Field effect transistors [13] and Ga_2O_3 MOSFETs [14]. Edge termination techniques for GaN and SiC devices to maximize breakdown voltage (V_{br}) have been well established [15][16][17][18][19]; however, such methods have not yet been fully developed for Ga_2O_3. One of the biggest challenges for Ga_2O_3 technology is the relative absence of p-type epitaxy or p-type doping which rules out the 'guard ring structure' method of edge termination [20][21]. This leaves methods like field plate structures [21][22] and high resistivity layers created by ion implantation [23] for edge termination.

In this paper, Ga_2O_3 Schottky diodes are examined to assess the limitations stated above and to improve the design considerations in terms of dimensions, structure, and the materials used. We report on the effect of dimensionality on the forward current and heat generation by modeling the current density and heat flow in the device. Edge termination techniques are also evaluated in a separate set of simulations.

II. Simulation Methods

The partial and total differential equations governing the physics of the electrical and thermal domains are solved self-consistently with the FLOODS TCAD simulator. FLOODS/FLOOPS is a partial differential equation (PDE) solver, written as an extension to the Tcl language for easy specification of PDEs and boundary conditions [24].

A. Device structure

The device structure as given in Fig. 1a is used as the reference for the study as a two-dimensional model and designed to achieve both high forward currents and good reverse breakdown characteristics [9]. The device consists of a lightly doped epitaxial layer grown on highly doped bulk β-Ga_2O_3 with [001] surface orientation and E-beam evaporated Ni/Au is used to form the Schottky (top) contact, while Ti/Au is used to form the Ohmic contact. In order to accurately model the electro-thermal profile the experimental IV curves are fitted via modeling [29]. The doping concentrations for the electro-thermal simulations are $1.3x10^{16}$ and $3.6x10^{18}$

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cm^{-3} for the epi and bulk layer respectively, and for the edge termination simulations are $2.8x10^{16}$ and $4.8x10^{18}$ for the epi and bulk layer respectively.

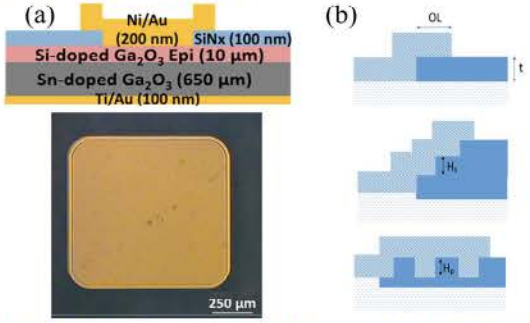

Figure 1. Schematic of a) vertical geometry Ni/Au Schottky structure (top) and top view with a contact area of 0.01 cm^{-2}, and b) field plate structures showing field plate overlap (OL), dielectric thickness (t), dielectric step height (H_S), and pillar height (Hp).

B. Electrical domain

Equations used the model include the common device equations [25] including the Poisson's, continuity and current density equations. By using the Boltzmann relation, the quasi-Fermi level from the current density equation can be related to the electrostatic potential. For the electric field analysis, the gradient of the electrostatic potential is then used to obtain the electric field, $|\vec{E}|$. Equation 1 describes the formulation of ionized donor trap density,

$$\frac{N_D^+}{N_{tot}} = \int \left(\frac{1}{1+2e^{\frac{E_F-E}{kT}}}\right)\left(\frac{1}{\nabla E\sqrt{2\pi}} e^{\frac{(E-E_T)^2}{2\nabla E^2}}\right) dE, \quad (1)$$

where N_{tot} is the total donor trap concentration, N_D^+ is the ionized donor density, E_F and E_T are the electron quasi-Fermi levels and trap levels, respectively, and ∇E is the energy spread of the traps. The total trap densities and energy levels of the traps associated with β-Ga_2O_3 [26] have been added into the above model. The mobility model used has been incorporated using the equations derived by Ma et al. [27].

Table 1. Material (electronic and thermal) properties of Ga_2O_3 vs other semiconductors.

	Si	4H-SiC	GaN (Wurzite)	Ga_2O_3
E_g (eV)	1.1	3.3	3.4	4.6-4.9
μ_n (cm^2/V-s)	1400	1000	1200	100-200
E_{cr} (MV/cm)	0.3	2.5	3.3	8
ε	11.8	9.7	9.0	10.0
Normalized BFOM	1	340	870	1100-2250
κ at 300K (W/m-K)	150	270	210	27 [010] 11 [100]

C. Thermal Domain

Using the electron and hole current densities, heat generation (Q) is incorporated into the model via Joule heating [28][29]. Heat transport is modeled as a function of heat generated and temperature change with respect to time and space via the following equation:

$$C\frac{\partial T}{\partial t} - \nabla \cdot K\nabla T = Q \quad (2)$$

where C is the specific heat capacity, T is temperature and K is the thermal conductivity. The thermal conductivity for Ga_2O_3 has been studied in detail, while Table I also shows the anisotropic nature of the thermal conductivity. Due to the surface orientation along the [001] direction and heat moving along the [001] direction, we assume an average value of 21 ± 2 W/mK. In coherence with previous thermal studies [31] an isotropic value for the thermal conductivity has been considered. However, future work with anisotropic thermal conductivity and the temperature dependence on the conductivity is ongoing. We use a convective heat transfer [32] equation as the boundary condition for heat transfer, given by Newton's law of cooling:

$$q' = hA(T_s - T_\infty) \quad (3)$$

where q' is the heat flux, h is the heat transfer coefficient, A is the area of the surface, T_s and T_∞ (300K) are the surface and ambient temperatures respectively. The heat transfer coefficient is expressed as a function of three dimensionless numbers, the Nusselt (Nu), Grashof (Gr) and the Prandtl (Pr) numbers.

$$Nu(Gr, Pr) = hL/k \quad (4)$$

$$Gr = \frac{g\beta (T_s - T_\infty)L^3}{\upsilon^2} \quad (5)$$

$$Pr = \frac{\mu C}{k} \quad (6)$$

In Eqs 4-6, L is the characteristic length, k is the thermal conductivity, g is the gravitational force, β is the volume coefficient of expansion (β = 1/T; for an ideal gas), μ and υ are the dynamic and kinematic viscosities. In order to get an expression for the heat transfer coefficient for different surfaces a simpler expression gives a better understanding:

$$\overline{Nu} = \frac{\bar{h}k}{L} = c(Gr\ Pr)^m \quad (9)$$

where c and m are constants, which depend on the type of surface in question (i.e., a vertical surface or a horizontal surface). A Dirichlet boundary condition is applied for the temperature at the bottom side of the wafer of T=300K, representing a perfect heat sink. While modeling the convective heat transfer from the top and sides of the device, Neumann boundary conditions have been set for the temperature.

III. Results and Discussions

A. Electro-Thermal management

The effect of forward (0-2.5 V) and power generation (0-5.5 W) is examined for the device structure. The effect of the voltage bias is reflected in heat generation in the drift region near the epi-metal interface and results in highest temperature values near this interface. A temperature profile is simulated in the device cross-section as seen in Fig 2a, and the effect of dimensionality is seen via this temperature profile and peak temperature (T_{max}) values. The bulk thickness is varied from 100 µm to 1000 µm while the epi-layer thickness and contact area were kept constant. This resulted in T_{max} values from 313 K for the 100 µm bulk to 417 K for 1000 µm bulk thickness. The rise in temperature also causes a drop in the electron mobility, while a thinner bulk also causes a higher effective heat dissipation via the bottom contact. Thinning the substrate thickness shows a significant reduction in heating in the device as seen in Fig 3.

Similarly, the epitaxial layer thickness was varied from 3 µm to 20 µm while the bulk-layer thickness and contact area

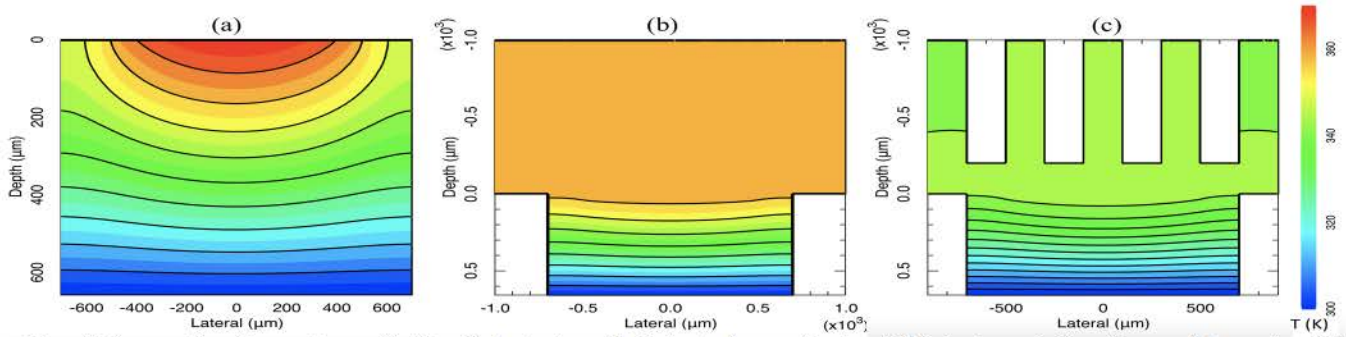

Figure 2. Cross-sectional temperature profile for a diode structure with free/natural convection from (a) device top and side surfaces peak temperature 369 K), (b) a copper top-side heat sink block (peak temperature 359 K), and (c) a copper top-side finned heat sink (peak temperature 344 K

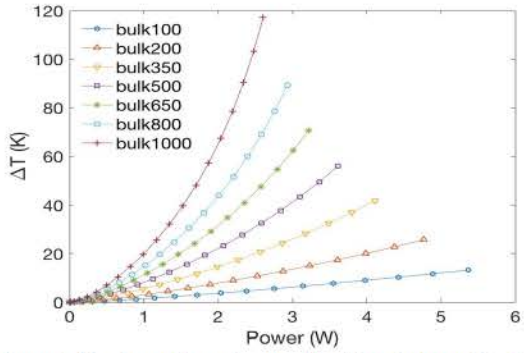

Figure 3. The temperature rises as a function of Power ($P=V^2/R$) while varying the bulk layer thickness from 100 μm to 1000 μm with epi-layer thickness constant at 7 μm.

were kept constant. As the epi-layer is thinned, the resistance decreases which results in higher currents in the device, (Fig 4); however, this results in a trade-off for peak temperature as the T_{max} ranges from 464 K for the 3 μm epi layer to 324 K for the 20 μm epi-layer thickness diode. The self-heating effects are evident, and the importance of efficient heat dissipation is realized.

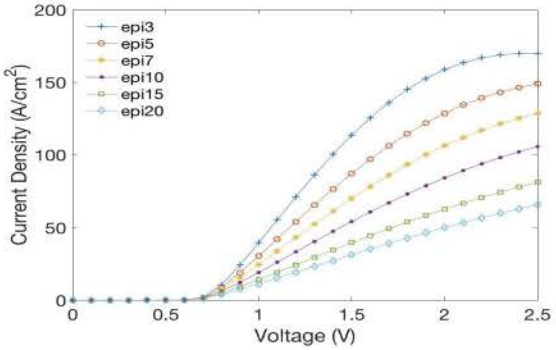

Figure 4. The dependence of the forward J-V characteristics on the epi-layer thickness from 3 μm to 20 μm with bulk thickness constant at 650 μm.

Initial studies show the importance of dimensions [4] and the simulations show considerable amounts of heat being dissipated from the Schottky (top) contact, a requirement for top-side passive cooling methods like nanocrystalline diamond capping layers and flip-chip hetero-integration. In electronics, copper is one of the most widely used material as a heat sink and different structures have been investigated thoroughly. Two top-side cooling cap heat-sink designs have been considered: a solid copper block and a finned copper structure. Heat loss from the heat sinks to the atmosphere is modeled as free convection via a steady flux. Fig 2 shows the temperature profile for three test simulations: a) natural convection with bulk thickness of 650 μm and epi thickness of 7 μm, b) the same device structure with a 1 mm thick solid Cu heat sink block with a width of 2 mm on top, c) the same device structure with a 1 mm thick finned copper heat sink and 200 μm fin thickness. As seen in the figure, the solid heat sink reduces the T_{max} value by ~10 K, while the finned heat sink reduces T_{max} by ~25 K compared to the device with no heat sink. The reduction is device temperature causes the mobility to increase which results in higher forward currents.

B. Edge termination techniques

The field plate (FP) structural variance is shown in Fig 1b. The electric field distribution is simulated and breakdown locations are observed which helps in concluding where the device is breaking down. Traditionally device breakdown happens near the contact edges due to field crowding near the edge, and edge termination is important to mitigate these effects. The electric field is mapped out as a function of reverse voltage and the breakdown voltage is noted as the critical electric field of the material is reached. The simulations are performed for each structure using the same mesh and the same technological parameters in order to maintain homogeneity in the results. Four dielectric materials have been studied as the FP dielectric; SiN_x (ε=7.0, E_{br}=6.7 MV/cm), SiO_2 (ε=3.9, E_{br}=10 MV/cm), Al_2O_3 (ε=8.0, E_{br}=8.68 MV/cm), and HfO_2 (ε=15.5, E_{br}=5.3 MV/cm). Figure 1.(b) shows the different FP structures used in the

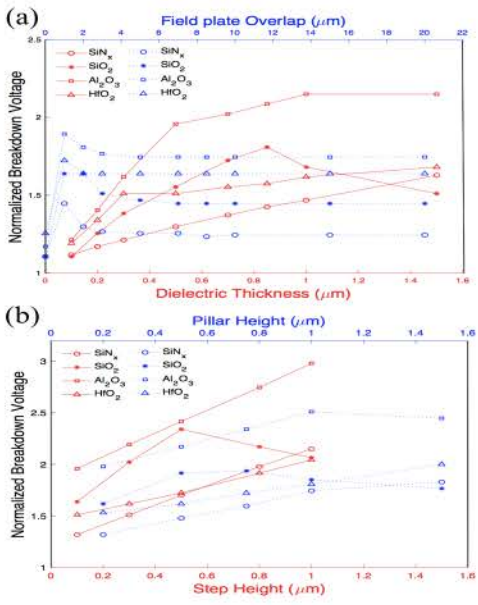

Figure 5. Plots showing the normalized breakdown voltage as a function of (a) field plate overlap (blue) and dielectric thickness (red), and (b) dielectric pillar height (blue) and dielectric step height (red).

simulations and denotes the variables in our simulations, i.e. dielectric layer thickness, filed plate overlap, step height, and pillar height. The results have been represented in Fig 5, the best results have been achieved for Al_2O_3 due to its high critical field strength and high relative permittivity, with a normalized breakdown field (V_{Nbr}) of more than 2 for the dielectric thickness equal to or greater than 0.5 µm. Furthermore, using Al_2O_3 dielectric step FP structure, a V_{Nbr} or more than 3 is achieved, while an Al_2O_3 pillar height of 1 µm achieves the highest V_{Nbr}. Future work on ion implantation to create highly resistive area near the contact is currently being developed.

IV. CONCLUSIONS

This paper conducted a thorough investigation via simulations into the effect of device design on β-Ga_2O_3 Schottky rectifiers to aid device optimization. Two pressing concerns of Ga_2O_3 as a power-electronics materials are addressed and the results predict efficient design considerations. Industry desires devices that generate high power and low self-induced heating. The results predict that a thin epitaxial layer and a thin substrate would achieve the desired result. The simulations predict a significant amount of heat being dissipated neat the Schottky contact and warrant the requirement of top-side passive cooling. In order to maximize the breakdown voltage, edge termination techniques were investigated and field plate designs and dielectric materials were studied.

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