Quantum Transport Simulations of the Zero Temperature Coefficient in Gate-all-around Nanowire pFETs

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Abstract— **We present a full quantum transport study of the zero-temperature coefficient (ZTC) point for sub-10 nm gate-all-around nanowire p-type field effect transistors (GAA NW pFETs). The phonon scattering effects are included through the self-consistent Born approximation in the non-equilibrium Green's function framework. The main findings are that the ZTC point can be present in GAA NW pFETs in sub-10 nm regime and the gate voltage at the ZTC point shows an opposite trend and has an upper limit at a certain gate length. This is due to the interplay between the ballisticity ratio and the ballistic current ratio, which can be explained only by the quantum transport simulations.**

Keywords—zero-temperature coefficient (ZTC), quantum transport, non-equilibrium Green's function (NEGF), k·p method, gate-all-around (GAA) nanowire field effect transistor

I. Introduction

Zero-temperature coefficient (ZTC) point has attracted attention to design devices immune to process, voltage, and temperature variation [1]. The ZTC point, corresponding to the bias voltage where current-voltage (I-V) characteristics show little variation with temperature, can play an important role in designing thermally stable CMOS integrated circuits [2]. For example, the current reference circuit exploiting bias voltages near the ZTC point has an advantage with low temperature coefficient [3]. For memory application, 1T-DRAM biased in the ZTC point shows a stable memory window over a wide range of temperature [4].

There are numerous works on the ZTC point for multi-gate structures such as double-gate ultra-thin-body field effect transistors (FETs) [5] and triple-gate FinFETs [6]. These studies have demonstrated the existence of the ZTC point for the FETs with several tens of nanometer. However, few works have been done on the ZTC point for gate-all-around nanowire (GAA NW) FETs with sub-10 nm feature size. In order to utilize the property of the ZTC point, it is necessary to evaluate the behavior of the ZTC point in sub-10 nm scale GAA NW FETs where the thermal reliability is a critical issue in particular. At such small dimensions, quantum effects such as tunneling and confinement strongly affect the device performance. Since it is insufficient to analyze the ZTC point in sub-10 nm scale through classical drift-diffusion transport model, quantum transport simulation should be considered to correctly investigate the behavior of the ZTC point for GAA NW FETs in sub-10 nm size.

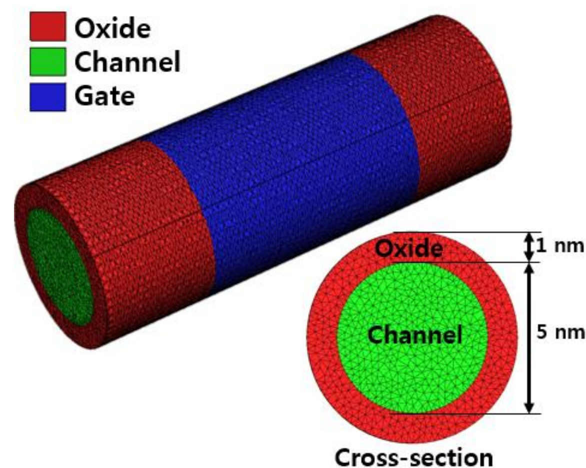

Fig. 1: Schematic structure of Si GAA NW and the circular cross-section with the FEM mesh configuration.

In this paper, we present a theoretical study of the ZTC point for Si GAA NW p-type FETs (pFETs) using a full three-dimensional (3-D) quantum transport simulation. To the best of our knowledge, it is the first time to study the ZTC point through the quantum transport simulations. We investigate the behavior of the ZTC point for a small size GAA NW pFETs and the scaling effects of L_g on the drain current (I_d) and the gate voltage (V_g) at the ZTC point.

II. Simulation Method

We have simulated NWs with a circular cross-section as shown in Fig. 1. The diameter of the NWs is 5 nm, which are surrounded by an oxide layer with an equivalent oxide thickness of 0.5 nm. L_g is scaled from 32 nm to 3 nm and the current flows along [100] direction. The channel is undoped and the source and drain are p-type doped with a concentration of 1×10^{20} cm^{-3}. All the simulations are conducted in the temperature range of 200-400 K with a supply voltage of 0.4 V.

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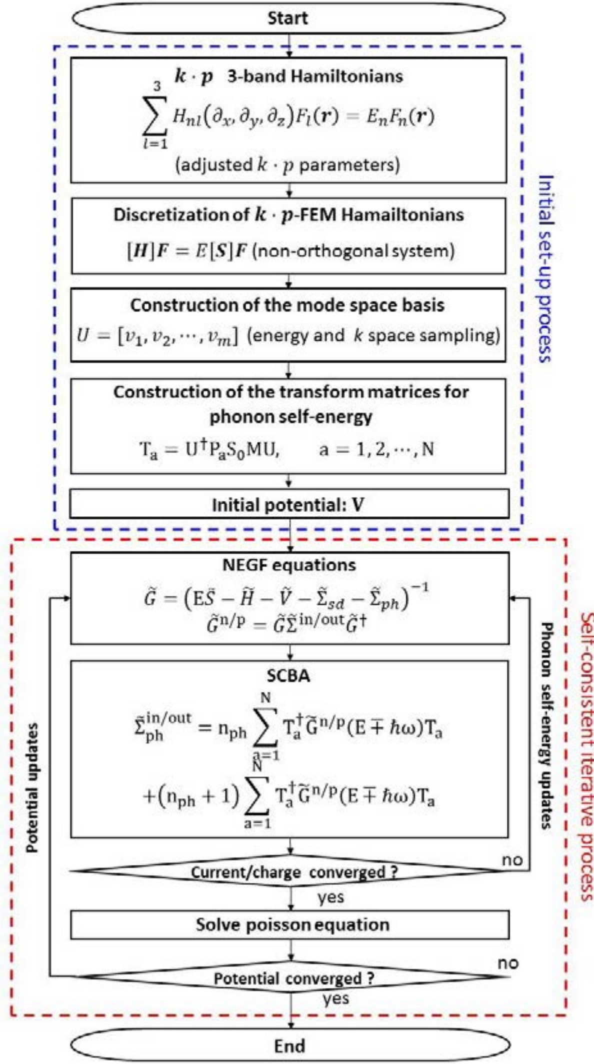

Fig. 2: Flowchart of the overall simulation procedure. m and N are the number of modes and FEM nodes, respectively. P_a is the orthogonal projection onto the subspace spanned by the $k{\cdot}p$ basis vectors of the ath node. S_0 is the overlap matrix and $n_{ph}(\omega)$ is the Bose-Einstein distribution of the phonon with frequency ω. The tilde represent the mode space quantities. In this work, 39 modes are used.

Fig. 2 shows the overall simulation flow chart. To faithfully represent a circular cross-section of the NWs, we have employed the finite element method (FEM) for 3-D discretization of the $k{\cdot}p$ Hamiltonians and the Poisson equation (see Fig. 1). The 3-band $k{\cdot}p$ model has been used to describe the valence bands. Since the bulk $k{\cdot}p$ parameters are inadequate to describe the band structure of the NW with a diameter of 5 nm, we used the adjusted $k{\cdot}p$ parameters in [7] to calculate the $k{\cdot}p$ Hamiltonians, whose the band structure matches well with tight-binding ones.

We have solved 3-D Poisson equation self-consistently with the non-equilibrium Green's function (NEGF) equations. As the ZTC point results from mutual compensation of mobility and threshold voltage (V_{th}) temperature effects [8], scattering mechanisms such as phonon scattering, surface roughness scattering, and Coulomb scattering should be included in the NEGF framework. Since, however, the most dominant scattering mechanism is the phonon scattering above 77 K [9], we have only considered phonon scattering in this work. The hole-phonon interaction has been rigorously treated through the self-consistent Born approximation (SCBA). We have assumed bulk phonon scattering as the mobility variation due to phonon confinement is weak for NWs with diameters larger than 5 nm [10]. The optical and acoustic deformation potential parameters are taken from [11]. For efficient NEGF simulations, we have reduced the size of the $k{\cdot}p$ Hamiltonians using the mode space method [12] where the Bloch modes are sampled in energy and k space. We have developed an efficient scheme to calculate the hole-phonon scattering self-energy in the mode space, which greatly reduces the computational cost of SCBA.

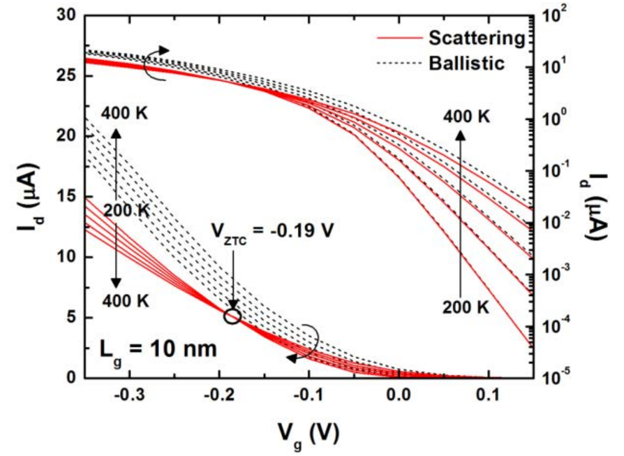

Fig. 3: I-V characteristics of the ballistic and the phonon scattering transport for L_g of 10 nm. V_{ZTC} is V_g at the ZTC point. The ballistic current was calculated using the electrostatic potential converged in the phonon scattering transport simulation.

III. RESULTS AND DISCUSSION

The GAA NW pFET with L_g of 10 nm was simulated to investigate the ZTC point for a small size FET. Fig. 3 shows the I-V curves for the ballistic and scattering transport. It is noted that I_d is insensitive to temperature variation at V_g = -0.19 V, indicating the ZTC point even in a small size FET. In order to clearly understand the ZTC point, we have compared the ballistic transport with the phonon scattering transport. We calculated the ballistic transport using the electrostatic potential of the scattering transport to exclude an artificial band edge shift [13].

Fig. 3 shows that in the subthreshold region, a similar trend is observed for ballistic and dissipative cases, where I_d is increased with the temperature and consequently V_{th} is decreased. This is due to the injection of carriers at high energy states, excited by the broadening effect of the Fermi-Dirac distribution. However, in the high V_g region, I_d of the scattering transport is decreased as the temperature increases, while I_d of the ballistic transport follows the same increasing trend as in the subthreshold region. The reason for the former is that the strength of the phonon scattering is enhanced at the elevated temperature. We therefore note that the ZTC point occurs even in sub-10 nm scale GAA NW FETs by the phonon scattering effects and the broadening effect of the Fermi-Dirac distribution.

In order to investigate how the scaling of L_g affects the ZTC point, we calculated the V_g (V_{ZTC}) and I_d (I_{ZTC}) at the

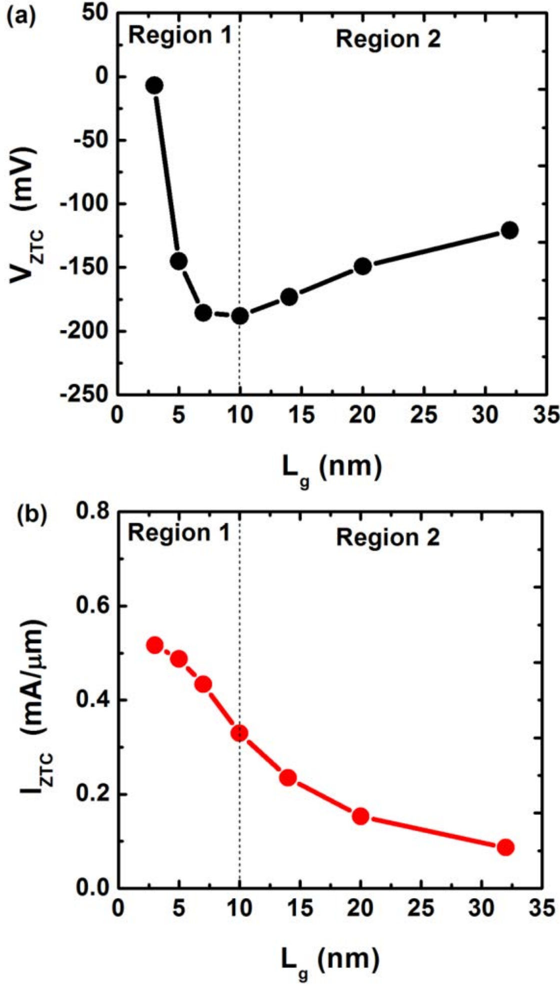

Fig. 4: V_{ZTC} (a) and I_{ZTC} (b) as a function of L_g, where V_{ZTC} and I_{ZTC} are V_g and I_d at the ZTC point, respectively. L_g of GAA NW FETs are 32, 20, 14, 10, 7, 5, and 3 nm.

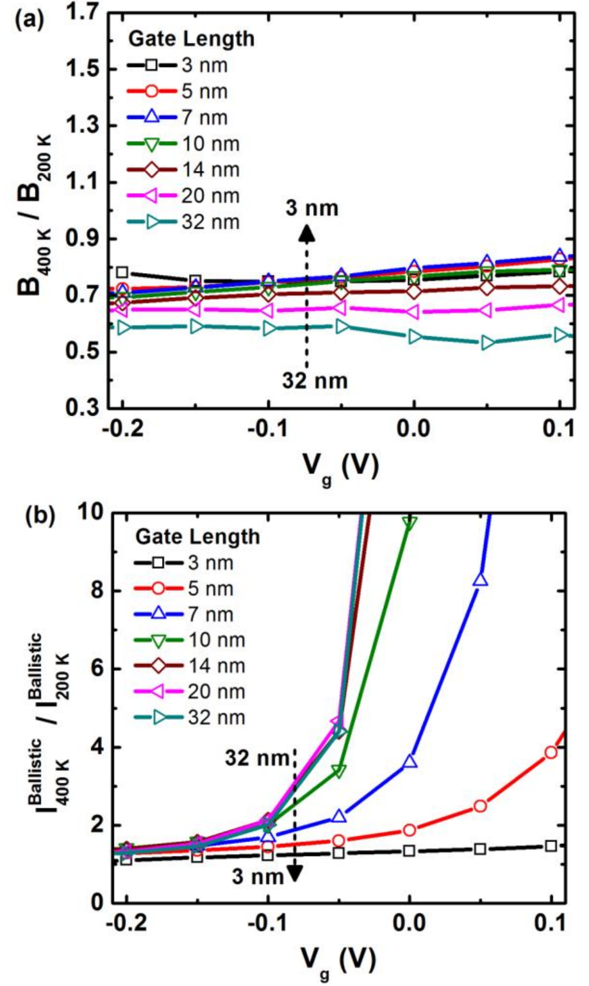

Fig. 5: Ballisticity ratio ($B_{400\,K}$ / $B_{200\,K}$) (a) and ballistic current ratio ($I^{Ballistic}_{400\,K}/I^{Ballistic}_{200\,K}$) (b) as a function of V_g. The ballisticity ratio represents the dependence of scattering strength on the variation of temperature. The ballistic current ratio reflects the intensity of source-to-drain direct tunneling (SDDT) current and the gate controllability.

ZTC point for various L_g from 32 to 3 nm as shown in Fig. 4. It is interesting to note that the $|V_{ZTC}|$ shows an opposite trend about a specific L_g and has a maximum value as illustrated in Fig. 4(a). As L_g scales down from 32 to 10 nm (see region 2 in Fig. 4(a)), the $|V_{ZTC}|$ is moderately increased by about 67 mV. On the other hand, when L_g shrinks down from 10 to 3 nm in region 1, the $|V_{ZTC}|$ is rapidly decreased by approximately 181 mV. The trend of the $|V_{ZTC}|$ in the region 2 is compatible with that for n-type FDSOI devices [14] where the $|V_{ZTC}|$ monotonically increases as gate length decreases from 69 to 29 nm. What is notable is the inverted trend of the $|V_{ZTC}|$ below L_g of 10 nm. For the case of I_{ZTC}, it has a different trend with the $|V_{ZTC}|$ as shown in Fig. 4(b). As L_g decreases, I_{ZTC} monotonically increases.

The contrary trends of the $|V_{ZTC}|$ can be explained by ballisticity and ballistic current, which are useful for describing the behavior of the $|V_{ZTC}|$ as it is determined by the interplay between those two values. The ballisticity is defined as the ratio of the scattering current to the ballistic current, expressing the strength of backscattering. Since the ZTC point occurs when I_d of 400 K ($I_{400\,K}$) is the same as I_d of 200 K ($I_{200\,K}$), the following equation (1) is satisfied at the ZTC point,

$$\frac{I_{400\,K}}{I_{200\,K}} = \frac{B_{400\,K}}{B_{200\,K}} \times \frac{I^{Ballistic}_{400\,K}}{I^{Ballistic}_{200\,K}} = 1, \qquad (1)$$

where B and $I^{Ballistic}$ are the ballisticity and the ballistic current, respectively.

Fig. 5 shows the ballisticity ratio ($B_{400\,K}$ / $B_{200\,K}$) and the ballistic current ratio ($I^{Ballistic}_{400\,K}/I^{Ballistic}_{200\,K}$) for GAA NW FETs with varying L_g in a range of 3 to 32 nm. It is helpful to describe the scaling dependences of these two ratios, before moving on to the analysis of the V_{ZTC} and I_{ZTC} variation. In Fig. 5(a), the ballisticity ratio is smaller than one for all devices simulated, meaning that the phonon scattering is enhanced at high temperature. It is noted that while the ballisticity ratio is moderately increased as L_g decreases from 32 to 10 nm, a further decrease of L_g does not significantly change the ratio. It is because the L_g is too short for the backscattering to take effect except the source/drain extension region.

Unlike the ballisticity ratio, the ballistic current ratio is larger than one as illustrated in Fig. 5(b). It is because of the broadening effect of the Fermi-Dirac distribution. We note that the ballistic current ratios of devices with L_g from 32 to 14 nm show almost similar behavior over V_g. The reason is that the thermionic current is dominant over source-to-drain

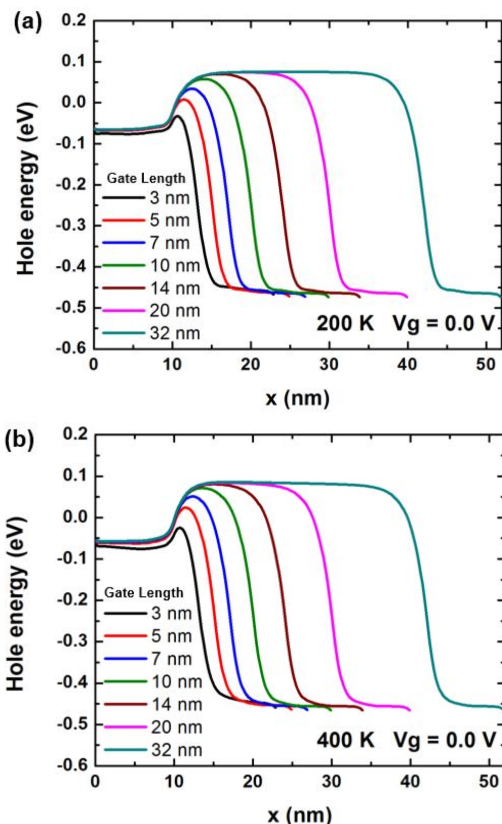

Fig. 6: Valence band edge profiles for 200 K (a) and 400 K (b) at Vg = 0.0 V.

direct tunneling (SDDT) current. When L_g is large enough for the SDDT current to be negligible, the ballistic current ratio is mainly determined by the difference of the amount of injected carriers over the band edge. Fig. 6 shows the valence band edge profiles at Vg = 0.0 V for the temperatures of 200 K and 400 K. In Fig. 6, for L_g from 32 to 14 nm, the valence band barrier heights are nearly same for all temperatures. Thus, the Fermi-Dirac broadening factor solely determines the ballistic current ratio. However, as the SDDT becomes dominant and the gate controllability degrades with reduction of L_g, the ballistic current ratio is rapidly decreased (see Fig. 5(b)).

As mentioned above, the trend of the $|V_{ZTC}|$ with L_g is easily described by examining the tendencies for the ballisticity ratio and the ballistic current ratio. For the devices with $L_g < 10$ nm, as L_g decreases, the ballisticity ratio is not significantly changed in Fig. 5(a). By contrast, the ballistic current ratio rapidly decreases with L_g in Fig. 5(b). Thus, to satisfy (1), the $|V_{ZTC}|$ should sharply decrease with L_g. In case of $L_g > 10$ nm, the trend of the $|V_{ZTC}|$ can be explained in the same manner but with the roles interchanged. As L_g decreases, the ballistic current ratio slightly changes as shown in Fig. 5(b). However, the ballisticity ratio increases so that the $|V_{ZTC}|$ is moderately increased.

When it comes to I_{ZTC}, it is attributed to the increase of the SDDT and the degradation of the gate controllability. Fig. 6 confirms this behavior. As L_g decreases, the tunneling length is decreased and the valence band barrier height is reduced. This enhances the SDDT and thermionic current, leading to the larger I_{ZTC}.

IV. Conclusion

In this paper, we have investigated the ZTC point of GAA NW pFETs by using the quantum transport simulations. We theoretically demonstrated that the ZTC point can appear in sub-10 nm scale. We discussed the L_g scaling effects on the ZTC point. It is found that as L_g decreases, $|V_{ZTC}|$ has an inverted trend at a specific L_g, where $|V_{ZTC}|$ moderately increases for $L_g > 10$ nm and rapidly decreases for $L_g < 10$ nm. Unlike the trend of $|V_{ZTC}|$, I_{ZTC} is monotonically increased with L_g. The results will help design the thermally stable CMOS circuit using GAA FETs with future technology nodes.

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References

[1] A. R. Mohamed, M. Chen, and G. Wang, “Untrimmed CMOS Nano-Ampere Current Reference with Curvature-Compensation Scheme,” 2019 IEEE International Symposium on Circuits and Systems, pp. 1-4, May. 2019.

[2] M. A. Alim and A. A. Rezazadeh, “Device behaviour and zero temperature coefficients analysis for microwave GaAs HEMT,” Solid State Electron., vol. 147, pp. 13-18, Sept. 2018.

[3] P. Toledo et al., “MOSFET ZTC condition analysis for a Self-biased current reference design,” Journal of integrated Circuits and Systems, vol. 10, no. 2, pp. 103-112, Dec. 2015.

[4] K. R. A. Sasaki, L. M. Almeida, J. A. Martino, M. Aoulaiche, E. Simoen, and C. Claeys, “Temperature influence on UTBOX 1T-DRAM using GIDL for writing operation,” 2012 International Caribbean Conference on Devices, Circuits and Systems, pp. 1-4, Mar. 2012.

[5] S. K. Mohapatra, K. P. Pradhan, and P. K. Sahu, “Temperature dependence inflection point in Ultra-Thin Si directly on Insulator (SDOI) MOSFETs: An influence to key performance metrics,” Superlattices Microstrut., vol. 78, pp. 134-143, Feb. 2015.

[6] C. W. Lee, et al., “High-Temperature Performance of Silicon Junctionless MOSFETs,” IEEE Trans. Electron Devices, vol. 57, no. 3, pp. 620-625, Mar. 2010.

[7] M. Shin, S. Lee, and G. Klimeck, “Computational Study on the Performance of Si Nanowire pMOSFETs Based on the k · p Method,” IEEE Trans. Electron Devices, vol. 57, no. 9, pp. 2274-2283, Sept. 2010.

[8] I. M. Filanovsky and A. Ahmed, “Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits,” IEEE Trans. Circuits Syst. I. Fundam. Theory Appl., vol. 48, no. 7, pp. 876-884, Jul. 2001.

[9] S. I. Takagi et al., “On the universality of inversion layer mobility in Si MOSFET's: Part I-effects of substrate impurity concentration,” IEEE Trans. Electron Devices, vol. 41, no. 12, pp. 2357-2362, Dec. 1994.

[10] E. B. Ramayya et al., “Electron transport in silicon nanowires: The role of acoustic phonon confinement and surface roughness scattering,” J. Appl. Phys., vol. 104, no. 6, p. 063711, Sept. 2008.

[11] N. Neophytou and K. Kosina, “Large enhancement in hole velocity and mobility in p-type [110] and [111] silicon nanowires by cross section scaling: an atomistic analysis,” Nano Lett, vol. 10, no. 12, pp. 4913-4919, Nov. 2010.

[12] M. Shin, W. J. Jeong, and J. Lee, “Density functional theory based simulations of silicon nanowire field effect transistors,” J. Appl. Phys., vol. 119, no. 15, p. 154505, Apr. 2016.

[13] M. Luisier and G. Klimeck, “Atomistic full-band simulations of silicon nanowire transistors: Effects of electron-phonon scattering,” Phys. Rev. B, vol. 80, no. 15, p. 155430, Oct. 2019.

[14] T. Nicoletti, et al., “The impact of gate length scaling on UTBOX FDSOI devices: The digital/analog performance of extension-less structures,” 2012 13th International Conference on Ultimate Integration on Silicon, pp. 121-124, Mar. 2012.