A SPICE Compatible Compact Model for Process and Bias Dependence of HCD in HKMG FDSOI MOSFETs

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***Abstract*— A SPICE compatible model is developed for the time kinetics of linear drain current drift (ΔI_{DLIN}) under Hot Carrier Degradation (HCD) stress in 28 nm Fully Depleted Silicon On Insulator (FDSOI) n-channel FETs having High-K Metal Gate (HKMG) gate stack. The impact of varying the drain (V_D), gate (V_G) and body (V_{BB}) biases is modeled. The framework is also capable of modeling the channel length (L_{CH}) and gate-oxide thickness (T_{OX}) variations. Impact of Self-Heating Effect (SHE) has also been taken into consideration during ΔI_{DLIN} modeling.**

Keywords—HCD, FDSOI, HKMG, SHE, gate-oxide thickness, body bias

I. INTRODUCTION

FDSOI MOSFETs are gaining interest for use in IoT and 5G applications. The adaptive body biasing in FDSOI devices can be utilized for dynamic power-performance control [1]. After a brief hiatus, HCD has once again emerged as one of the important and crucial aspects of MOSFET reliability and it impacts both FinFET and FDSOI devices [2]-[9]. HCD causes local damage towards the drain side of the transistor leading to device parametric degradation. Accurate modeling of HCD time kinetics is necessary to extrapolate short time accelerated stress data to determine the HCD magnitude at End-OF Life (EOL) under operating condition. Unlike typical stress condition where V_G and V_D are held fixed, in actual digital circuit V_G and V_D are varied from 0 to V_{DD}. Thus, it is necessary to model the HCD time kinetics under full V_G/V_D space [10]. Unlike FinFET, the FDSOI devices use adaptive V_{BB} to optimize performance and power consumption [1], which also impacts HCD [9] and needs to be modeled. Finally, SHE needs to be carefully modeled in more electrostatically confined architectures (like FinFET and FDSOI) where thermal resistance is much higher than the bulk counterparts [11]. Note that unlike classical HCD, degradation in modern devices show positive temperature (T) activation (increase at larger T) [3]-[5]. The compact model should be SPICE compatible, where the transistor degradation should only depend on V_G, V_D, V_{BB}, T and time, and not on any device parameter (like I_D or saturation drain bias (V_{DSAT}) etc.). Our previous work has shown, using Eq.(1), the model struggles to predict the measured time kinetics across wide V_D and time ranges. Fig.2 (a) plots the prediction of V_D (using Eq.(1)) dependent I_{DLIN} degradation in time from [13]. Therefore, to improve accuracy, the basic Eq.(1) is modified using a time varying *m* Eq.(2). Fig 1(b) and Fig. 2 shows the modeled time kinetics using the modified equation for planar [10] and Fig. 3 for FinFET [12] devices. The framework is robust to model different probes as V_T, I_{DLIN}, I_{DSAT} and CP. Fig. 2 plots the model prediction [10] of time kinetics probed by using (a, b) V_T, (c, d) I_{DSAT} and (e, f) I_{DLIN} methods in shorter L_{CH} planar devices [14]. The V_D dependence at various V_G/V_D combinations is studied in different L_{CH} at room and higher T. The P is listed, which is device and probe specific. Fig. 3 shows the time kinetics of ΔV_T during HCD stress at different V_G and V_D conditions in SiGe channel p-FinFETs measured by an ultra-fast method and explained using the SPICE compatible compact model.

II. SCOPE OF WORK

The developed compact model for planar and FinFET devices [10, 12] is suitably modified for FDSOI MOSFET. It can model the ΔI_{DLIN} time kinetics under full V_G / V_D / V_{BB} space and also model the L_{CH} and T_{OX} dependence. In particular, the impact of L_{CH} and T_{OX} on the V_G dependence of HCD can be modeled. The model is validated against measured data from published reports on 28 nm FDSOI technology [6]-[8] and the parameters are listed.

III. FRAMEWORK

The schematic of a FDSOI MOSFET is shown in Fig. 4 along with localized defects induced by HCD stress in the channel and near drain junction, gate-drain overlap and spacer regions. Threshold voltage and mobility are affected due to the defects in channel, and defects in the overlap and spacer regions impact series resistance. Therefore, defects in all the regions impact drain current. The compact model equations are listed in Table-I. Eq.(1) shows the self-saturating empirical equation to model the HCD time kinetics with a time-varying slope, Eq.(2). Eqs. (3)-(9) govern the modeling of the time-constant (τ) that takes into account all the process parameters (L_{CH} and T_{OX}) and the stress conditions (V_G, V_D, V_{BB}, and T). Eq.(10) is used for SHE. Fig. 5 shows the measured and modeled time kinetics of ΔI_{DLIN} for various V_G/V_D conditions for thin gate oxide at room temperature (25˚C).

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IV. BODY BIAS DEPENDENCE

In FDSOI structure, forward body biasing can be done to switch the transistor faster. Fig. 6 (a) and (b) show the measured and modeled forward body bias effect on HCD time kinetics in a device having L_{CH} of 0.30 µm and thin gate oxide. Fig. 6 (a) shows the time kinetics with varying V_{BB} and keeping V_G and V_D constant. It is observed that degradation increases with increase in V_{BB}. Fig. 6 (b) shows the fixed time degradation with varying V_G. It can be modeled using a consistent set of parameters, which are also used in Fig. 7 (a).

V. CHANNEL LENGTH DEPENDENCE

Fig. 7 models the impact of L_{CH} variation on the V_G dependence of measured ΔI_{DLIN} (V_D is held fixed) at a fixed stress time for thin and thick oxide devices. Note that the V_G dependence is different for thick and thin oxide devices. Fig. 7 (a) shows the V_G dependence changes from bell shape to monotonic with decreasing L_{CH} for thin gate oxide. However, in Fig. 7 (b) the effect is reversed with L_{CH} for thick gate oxide. It can be seen that the model is capable of explaining both trends with consistent model parameters, which are listed in Table-II. Note that the difference in V_G dependence of ΔI_{DLIN} for thin and thick oxide devices is due to difference in V_G dependence of the sub-components of time constant (τ) as shown in Fig.8 (a) and (b): τ_A monotonically reduces while τ_B increases first and later reduces as V_G is increased and they control the overall τ and HCD lifetime. For thick gate oxide device, τ_A is dominant till V_G=V_D/2 while for thin gate oxide it is significant till V_G= V_D, which are the well-known worse case conditions for each cases [10]. Also, the model helps to explain the L_{CH} scaling keeping same gate process. Model parameters are listed in Table-II.

VI. OXIDE THICKNESS

Measured HCD data from different T_{OX} devices are modeled using a consistent set of parameters at a fixed L_{CH}. Fig. 9 shows the measured and modeled data for gate oxide thickness variation at 0.15 µm channel length. Thus, the model can help in providing the complete modeling and thus helps in the study of gate-oxide scaling as well.

VII. CONCLUSION

A compact HCD time kinetics model is proposed and validated using measured data from 28 nm FDSOI devices. The model is fully SPICE compatible, as it only uses terminal voltages and T, and does not depend on any internal transistor parameter. It can model data over the full V_G/V_D spectrum (for V_G <, = and > V_D); different T (including SHE as applicable), V_{BB}, and can also handle technology parameter (L_{CH} and T_{OX}) changes. In particular, it is observed that L_{CH} scaling results in different V_G dependence of measured ΔI_{DLIN} at fixed time for thick and thin T_{OX} devices, which is explained. The model can be incorporated in a SPICE simulator to model HCD in actual circuits under different mission profiles.

VIII. REFERENCE

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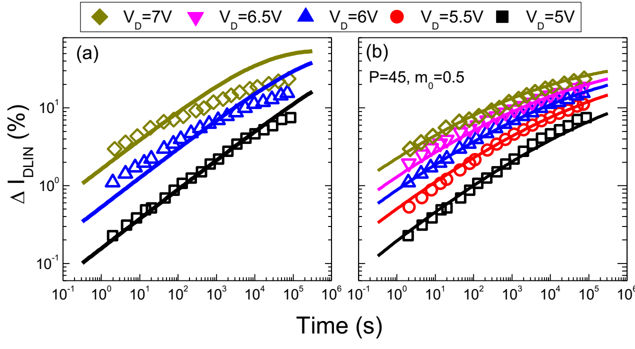

Fig.1. Modeling of measured ΔI_{DLIN} time kinetics at different V_D for on-state HCD stress (data from [13]) using standard and modified compact models. Further details [10].

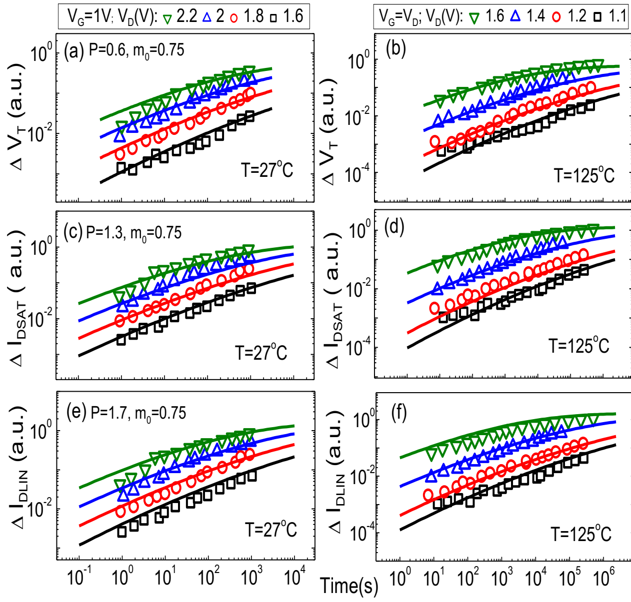

Fig.2. Modeling of V_D dependence of measured (a, b) ΔV_T, (c, d) ΔI_{DSAT} and (e, f) ΔI_{DLIN} time kinetics at (a, c, e) room and (b, d, f) high T from planar devices at low V_D stress [14]. Further details [10].

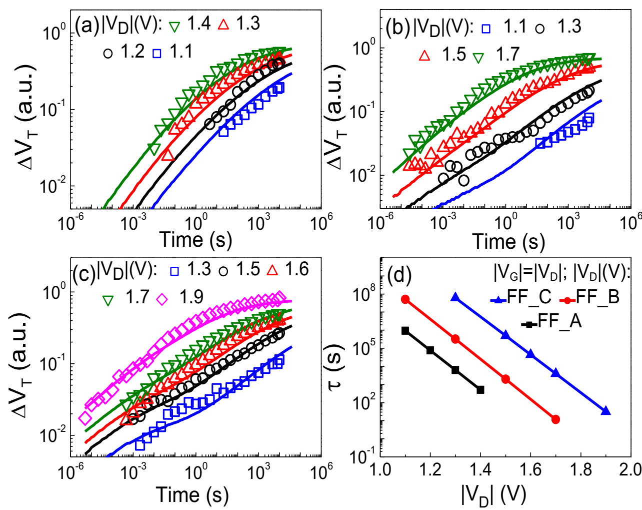

Fig.3. Time kinetics of measured and modeled ΔV_T at different stress V_D but for $|V_G| = |V_D|$ condition in SiGe devices (a) FF_A (Low N%, L_{CH}= 20 nm), (b) FF_B (High N%, L_{CH}= 20 nm) and (c) FF_C (High N%, L_{CH}= 60 nm) devices. Symbols: data, lines: model. In (d), the V_D dependence of the parameter τ (see Eq. (1) and Eq. (2), Table-I) is identical for all three devices. Further details [12].

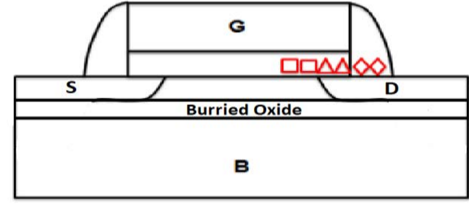

Fig 4. Schematic of a FDSOI MOSFET showing regions along the channel that get degraded during HCD: square (channel), triangle (gate/drain overlap) and diamond (spacer).

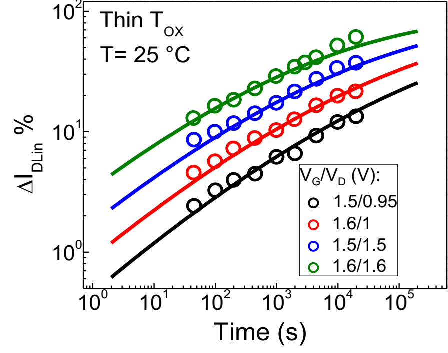

Fig. 5. Time evolution of experimental ΔI_{DLIN} (in %) for DC stress, with model prediction at different V_G and V_D

TABLE I. COMPACT MODEL EQUATIONS

$$\Delta P = P\left[1 - e^{\left\{-\left(\frac{t}{\tau}\right)^{m}\right\}}\right] \quad (1)$$

$$m = m_0 e^{\left[-\left(\frac{t}{\tau_m}\right)^{k}\right]} \quad (2)$$

$$\tau = (\tau_A + \tau_B) \quad (3)$$

$$\tau_A = \frac{A}{e^{\Gamma_{A2}(V'_D)}} e^{\Gamma_{A1}(V'_D - \alpha V_G)} \quad (4a)$$

$$\tau_B = \frac{B}{C} e^{\Gamma_{B1}(V_G - \beta V'_D)} \quad (4b)$$

$$C = \left[1 + C_1 e^{\Gamma_{C1}(V_G - \sigma V'_D)}\right] e^{(\Gamma_{C2} V'_D)} \quad (5)$$

$$V'_D = V_D + (\chi * V_{BB}); \quad (6)$$

$$\alpha = \alpha_0 * T_{ox}; \quad (7a)$$

$$\Gamma_{B1} = \Gamma_{B10} * e^{-(Tox*s1)}; \quad (7b)$$

$$\Gamma_{C1} = \Gamma_{C10} * T_{ox}^{(s2)}; \quad (7c)$$

$$A = A_1 e^{\left(\frac{-Ea_A}{kT}\right)},\ B = B_1 e^{\left(\frac{-Ea_B}{kT}\right)} \quad (8)$$

$$A_1 = A_2\, L_{CH}^{(\lambda_A)},\ B_1 = B_2\, L_{CH}^{(\lambda_B)},\ C_1 = C_2\, L_{CH}^{(\lambda_C)} \quad (9)$$

$$T = T_{SHE} + T_{CHUCK},\ T_{SHE} = \Theta V_G V_D \quad (10)$$

ΔP: device parameter shift,
P: Model parameter related to maximum degradation,
t: stress time, τ : related to bond dissociation rate,
m: governs the kinetics at early time before the onset of saturation

TABLE II. MODEL PARAMETERS

Fixed Parameters:
m_0= 0.5; τ_m (s) = 1e4; k = 0.036; χ = 0.08;
s1 = 0.1; s2 = 0.5; Γ_{A1} (V^{-1}) = 4.5; Γ_{A2} (V^{-1}) = 17.6;
E_{A_HC} (eV) = 0.4; β = 0.5; E_{B_HC} (eV) = 0.4; σ = 1;
Γ_{C2} (V^{-1}) = 6.96;

Adjustable Parameters:

	Fig 4a	Fig 4b	Fig 5
A2*	1	0.4	1e-5
α/α_0	2	2.5	0.027
B2*	1	1e3	1e-1
Γ_B / Γ_{B0} (V^{-1})	2	1.7	60
C2*	1	10	10
Γ_{C1}/Γ_{C10} (V^{-1})	6	5.8	35

*values are normalized to thin gate oxide parameters. Data for thick and thin oxide are normalized to different values in referenced paper.

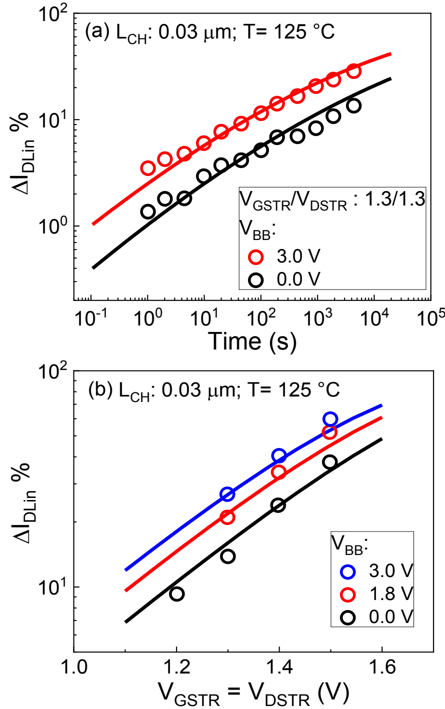

Fig. 6. Modeling of V_{BB} stress impact over I_{DLIN} drift in thin gate-oxide (a) time kinetics over classical HCI stress with FBB stress for (b) over voltage stress where V_G=V_D with and without FBB at fixed time.

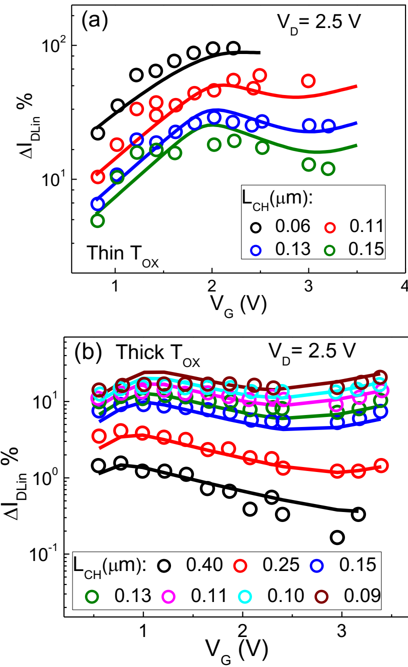

Fig. 7. Modeling of channel length dependence. (a) thin gate-oxide and (b) thick gate oxide. (a, b) shows varying channel length across V_G. Parameters are shown in Table II.

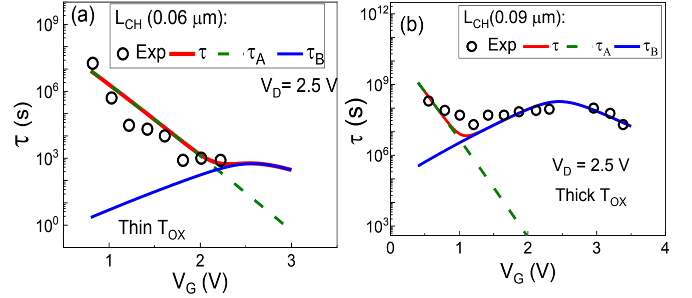

Fig. 8. Contribution from different τ subcomponents. (a) thin gate-oxide and (b) thick gate oxide. (b) shows varying channel length across VG. Parameters are shown in Table II.

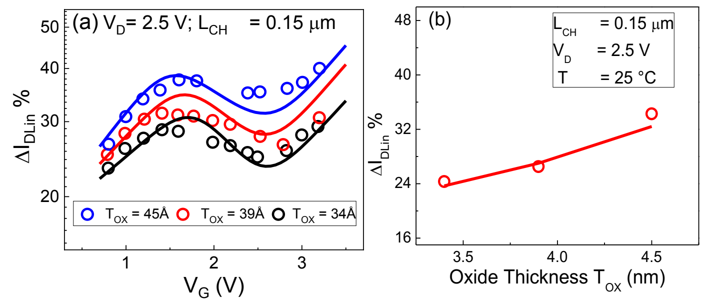

Fig. 9. I_{DLIN} drift modeling over gate voltage stress for (a) several gate-oxide thickness at fixed channel length (b) several gate-oxide thickness at fixed condition V_G=V_D.