

Simulation of Statistical NBTI Degradation in 10nm Doped Channel pFinFETs

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Abstract— *In this paper, by means of simulations, we have studied the impact of Negative Bias Temperature Instability (NBTI) in bulk silicon FinFETs suitable to the 10nm CMOS technology generation. Different levels of channel doping are considered in controlling the threshold voltage and the leakage of the FinFETs for SoC applications. The interplay between the initial statistical variability introduced by random discrete dopants, line edge roughness and metal gate granularity and the statistical variability introduced by different level of trapped charges resulting from NBTI degradation is studied in details. Results related to the time dependent variability and the correlation of key transistor figures of merit are also presented.*

Keywords—Atomistic doping; NBTI; FinFETs; statistical simulations; statistical variability; MOSFET FOMs correlations

I. INTRODUCTION

Performance limitations and increasing statistical variability [1][2] have prompted the end of bulk planar MOSFET scaling at 28/20nm CMOS technology generation [3]-[5]. FinFETs, with improved electrostatic integrity, that tolerate low channel doping, have been introduced by Intel at the 22nm CMOS technology generation [6] to sustain the benefits from increased power/performance with the continuation of CMOS scaling and to reduce the statistical variability. The rest of the industry follow suit at 14/16nm CMOS and now 10nm and 7nm FinFET CMOS are in production.

The low channel doping that FinFETs tolerate improves the performance due to reduced impurity scattering in the channel and steeper subthreshold slope (SS) [7][8] and could almost completely eliminate the random discrete dopant (RDD) induced variability in the threshold voltage (V_T) [9]. However, for System on Chip (SoC) design FinFETs with different V_T will be needed [10]. Gate work-function engineering via gate implantation or different metal spices can be used to deliver different V_T 's at low channel doping, but at 14/16nm and in some 10 nm CMOS implementation doping is used for tuning V_T [11].

Simultaneously Negative Bias Temperature (NBTI) related time dependent statistical variability has been highlighted as a critical issue at 45/40nm CMOS [12]. However, with the further scaling of the bulk CMOS technology the relative importance of the NBTI induced statistical variability has been reduced due to the increasingly dominate role of RDD induced statistical variability associated with the necessary increase in channel doping with scaling. However, the possibility to reduce the

channel doping and the related variability in FinFETs brings back the concerns about the NBTI induced statistical variability [9].

In this paper we study and compare statistical NBTI effects associated with the trapping of individual discrete charges in bulk FinFETs designed to meet the requirements of the 10nm CMOS technology generation. Transistors with various level of channel doping, needed to control the V_T and leakage for different aspects of SoC applications, are investigated.

II. DEVICE DESIGN AND SIMULATION METHODOLOGY

The 'template' p-channel FinFET adopted in this study is representative for 10nm technology generation bulk FinFETs introduced by major foundries in 2017 and are close to the FinFETs introduced by Intel in their 14nm CMOS offering [13]. The gate pitch is 64nm, the fin pitch is 40nm, the channel length is 28nm, the spacer is 8nm thick, fin height is 44nm and fin width is 8nm. The device design was initially targeted for high performance applications with leakage current (I_{OFF}) of 100nA/ μm using low channel doping of 10^{17}cm^{-3} and work function (WF) engineering. Then the channel doping of $2 \times 10^{18}\text{cm}^{-3}$ and $4.5 \times 10^{18}\text{cm}^{-3}$ has been introduced to shift V_T and to reduce I_{OFF} to 10nA/ μm and 1nA/ μm respectively. Detailed description of the FinFET template can be found in [14]

To predict accurately the transistor performance, full band (FB) Ensemble Monte Carlo (EMC) simulations are carried out using the EMC module of GARAND [15]. In order to study the statistical variability and reliability effects, drift diffusion (DD) simulations using the DD module of GARAND were calibrated to the results of the EMC simulations.

The resolution of the individual discrete dopants in the random discrete dopants (RDD) simulations employs fine meshing in conjunction with density gradient quantum corrections. This prevents artificial charge trapping in the sharply resolved Coulomb wells of the ionized dopants and avoids acute mesh-spacing sensitivity [16]. Line edge roughness (LER) is modeled based on the assumption that it follows a Gaussian autocorrelation function [17] with three times root-mean-square (Δ) deviation of the gate edge position of $\text{LER}=3\Delta=2$ nm and a correlation length $\Lambda=30$ nm. Identical LER parameters are used to model both gate edge roughness (GER) and fin edge roughness (FER). The modeling of metal

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gate granularity (MGG) assumes a TiN metal gate with two major grain orientations leading to a WF difference of 0.2 V, with a probability of 0.4/0.6 for the lower/higher WF respectively, and an average grain diameter of 5 nm [18].

Five levels of NBTI degradation corresponding to trapped charge densities ranging from $N_T = 1.0 \times 10^{11} \text{ cm}^{-2}$ to $N_T = 2.0 \times 10^{12} \text{ cm}^{-2}$ are considered. The random trapped charges are introduced at the channel/gate dielectric interface using the methodology described in [19] resulting in random numbers and positions of traps in each individual transistor. The low drain bias statistical current voltage characteristics the highly doped channel FinFETs with $4.5 \times 10^{18} \text{ cm}^{-3}$ are illustrated in Fig. 1 as fresh devices (a) and after NBTI degradation (b) resulting in average trapped charge density of $2 \times 10^{12} \text{ cm}^{-2}$. We would like to make some observations based on Fig.1 before proceeding with the detailed analysis of the simulation results at various degradation conditions in the next section. It is clear that the virgin low channel doping FinFET has lower statistical variability compared to virgin high channel doping FinFET. Simultaneously the same level of NBTI degradation resulted in significant increase in the variability in the low channel doping FinFET and much smaller increase of the variability in the high channel doping FinFET.

It has been shown previously that the continuous doping TCAD simulations differ from the average of the atomistic simulations yielding progressively erroneous results in the subthreshold with the reduction of transistor dimensions [20]. The problems in the case of FinFET simulations increase with the increase of the channel doping. Here we investigate to what extent the discrepancy between the continuous doping and the average ‘atomistic’ simulation is exacerbated with the increase in the average trapped charge density. First we investigate the V_T lowering properties of these devices.

Fig. 2 illustrates the continuously doped device, average and median V_T dependences on the average trapped charge at low channel doping of 10^{17} cm^{-3} and at the highest $4.5 \times 10^{18} \text{ cm}^{-3}$. Clearly the increase of the channel doping results in higher threshold voltage lowering particularly at high drain bias. Simultaneously the increase of the average trapped charge density contributes to a relatively small increase in threshold voltage lowering at both channel-doping concentrations. To study further this effect, we present in Fig. 3 uniform, average and median threshold voltage shift dependence on the average trapped charge at low channel doping of 10^{17} cm^{-2} . There is a clear lowering in the threshold voltage shift (ΔV_T) which is

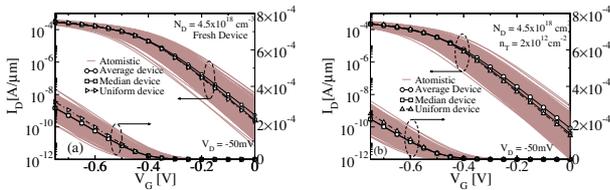


Fig. 1: Statistical I_D - V_G of the highly doped FinFET without trap (a), and when interface traps of $N_T = 2 \times 10^{12} \text{ cm}^{-2}$ are considered in the simulation (b).

more pronounced at low drain and can reach more than 5 mV at $N_T = 2 \times 10^{12} \text{ cm}^{-2}$. This newly reported ΔV_T -lowering phenomena reduces the average threshold voltage shift associated with charge trapping compared to the results from uniform simulation.

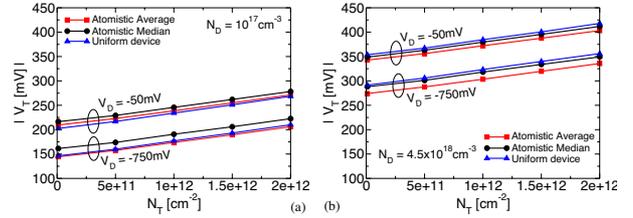


Fig. 2: Uniform, average and median V_T dependence on N_T at $N_D = 1 \times 10^{17} \text{ cm}^{-3}$ and $N_D = 4.5 \times 10^{18} \text{ cm}^{-3}$.

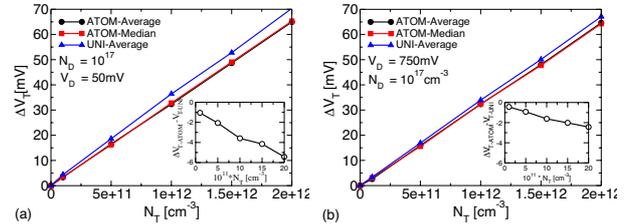


Fig. 3: Uniform, average and median ΔV_T dependence on N_T at $N_D = 1 \times 10^{17} \text{ cm}^{-3}$ (a) $N_D = 4.5 \times 10^{18} \text{ cm}^{-3}$ (b)

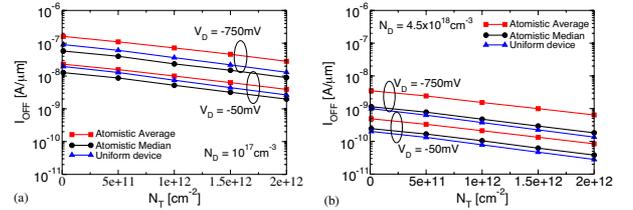


Fig. 4: Uniform, average and median gate leakage dependence on N_T $N_D = 1 \times 10^{17} \text{ cm}^{-3}$ and $N_D = 4.5 \times 10^{18} \text{ cm}^{-3}$.

Figure 4 illustrates the dependence of the uniform, average and median leakage current on the average trapped charge density at low (10^{17} cm^{-3}) and high ($4.5 \times 10^{18} \text{ cm}^{-3}$) channel doping. We notice that the percentage discrepancy between the uniform and the average leakage current increase with the increase trapped charge. The effect is stronger at high drain bias and at channel doping of 10^{17} cm^{-3} . The discrepancy increases from 100% to 130% when the trapped charge increases from zero to $2 \times 10^{12} \text{ cm}^{-2}$. At channel doping of $4.5 \times 10^{18} \text{ cm}^{-3}$ the discrepancy increases from 300% to 380% when the trapped charge increases from zero to $2 \times 10^{12} \text{ cm}^{-2}$.

It is well understood that the statistical DD simulation accurately captures the statistical variability in the subthreshold region but can underestimate the on state variability, particularly associate with transport variation due to scattering with random discrete dopants and trapped charges [21]. Simultaneously the average on current is lowered due to certain amount of charge trapping in the Coulomb well of individual dopants, even after the introduction of density gradient quantum corrections [16]. Therefore, in the next section we analyze in great details the statistical variability in the subthreshold region.

III. RESULTS AND DISCUSSION

A. Threshold Voltage Variability

In the simulations we have considered two scenarios for the initial statistical variability of the FinFETs. In the first scenario, combined sources of variability, RDD, GER, FER and MGG are considered. In the second scenario we assume that sidewall deposition definition is used for the fin, which results in correlated FER with little impact on statistical variability, and therefore only RDD, GER and MGG are taken into account. The resulting threshold voltage distributions at low drain bias and at different levels of doping and different degrees of degradation are presented in Fig. 5. The corresponding values of the σV_T are plotted as a function of the channel doping concentration in Fig. 6.

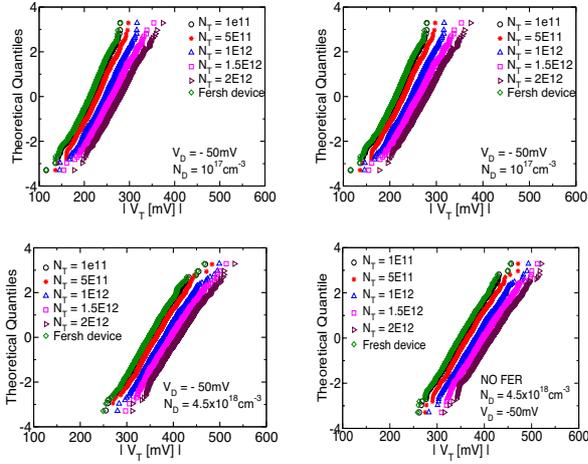


Fig. 5: V_T distribution for two cases of SV at $V_D = -50$ mV. Figures in the left column are for all variability sources while in the right column FER is excluded assuming sidewall Fin definition.

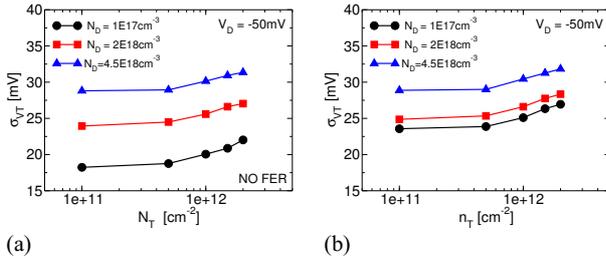


Fig. 6 Dependence of the standard deviation of the threshold voltage on the areal density of the trapped charge showing all sources of SV without FER (a) and with (b)

From the visual inspection of Fig. 5 and Fig. 6 it is clear that the trapping of discrete charges in the progressive NBTI degradation result not only in average threshold voltage shift, but also in increase of the statistical variability captured by σV_T . The NBTI induced increase of σV_T at a particular stage of degradation, determined by the areal density of the trapped charge depends on the level of variability in the fresh FinFETs. The impact of the degradation is stronger in the FinFETs with low channel doping and more pronounced in the case without FER at low drain bias conditions. In this case trapped charge of 2.0×10^{12} cm^{-2} increases σV_T from 17.8 mV in the fresh

transistors to 22.2 mV in the degraded one, which is approximately 25% increase.

At high channel doping of 4.5×10^{18} cm^{-3} and all sources of variability present the increase of σV_T is from 28.6 mV to 31.5 mV, which is approximately 10% increase. Also at high drain bias the initial variability is higher due to the LER induced effects and the relative impact of the trapped charge is smaller in all cases. It is clear that the virgin low-doped FinFETs, particularly in the absence of FER variability offer almost 60% improvement in σV_T compared to the highly doped FinFETs. However, this improvement is reduced to 40% after heavy degradation.

B. Subthreshold Figures of Merit Variability

It is also interesting to investigate the impact of the degradation on other important transistor figures of merit like the drain induced barrier lowering (DIBL), SS and I_{OFF} . Fig. 7 illustrated the trapped charge density dependence of the DIBL (a) and SS (b) of the lightly doped (10^{17} cm^{-3}) and the heavily doped (4.5×10^{18} cm^{-3}) FinFETs in the presence of RDD, FER, GER and MGG. The DIBL distribution strongly departs from a normal distribution, which should be represented by a straight line in Fig. 7 (a). It is clear that the charge trapping has a very little impact on the DIBL distribution. However, it should be noted that both in the low and high doped FinFETs the DIBL distribution is very broad, ranging from 30 to 180 mV/V and that the addition of channel doping does not improve DIBL. The SS distribution is also strongly non-Gaussian and has significant upper tail in the case of the heavily doped FinFETs, which are also strongly affected by the charge trapping. The high drain bias trapped charge density dependence of the I_{OFF} is illustrated in Fig. 8 for the lightly doped and the heavily doped FinFETs in the presence of RDD, FER, GER and MGG. Please note that the simulations do not include band-to-band tunneling.

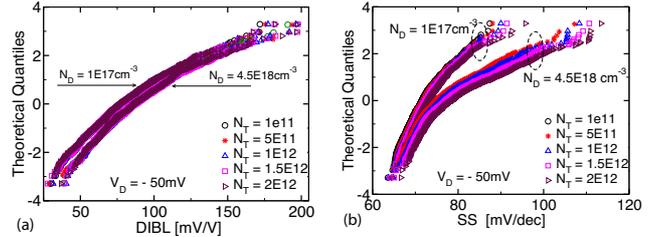


Fig. 7: N_T dependence of the DIBL (a) and SS (b) with $N_D = 1 \times 10^{17}$ cm^{-3} and $N_D = 4.5 \times 10^{18}$ cm^{-3}

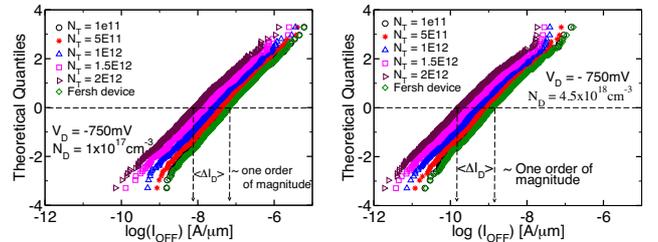


Fig. 8: N_T dependence of the I_{OFF} for $N_D = 1 \times 10^{17}$ cm^{-3} (a) and $N_D = 4.5 \times 10^{18}$ cm^{-3} FinFETs.

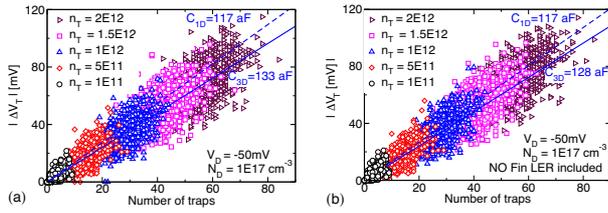


Fig. 9: Fractional ΔV_T as a function of the number of trapped charges at different levels of degradation. The left column is with all relevant variability sources including RDD, GER, FER and MGG (a) and where FER has been excluded by assuming sidewall Fin definition (b). The dashed line represents an ideal capacitance (C_{ID}) from a planar capacitance and the ‘effective’ capacitance (C_{3D}) derived from the slope of the average curve.

As expected, the progressive charge trapping reduces the average leakage due to the corresponding average increase of the threshold voltage but increases the leakage voltage spread. Analogous to the spread in the V_T the spread in the leakage current increases faster with trapping in the lightly doped channel FinFET.

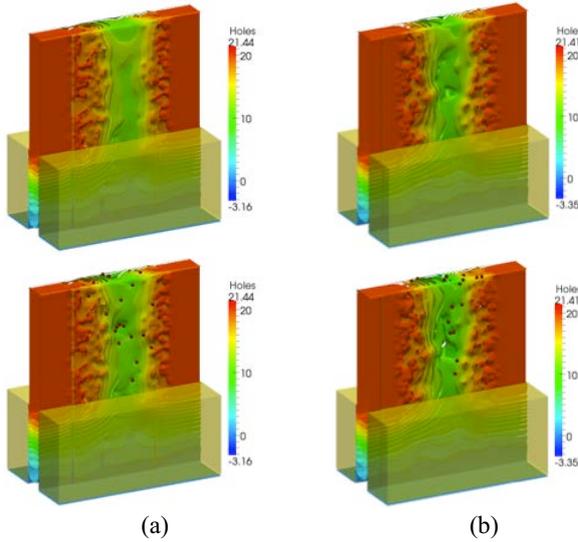


Fig. 10: 3D distribution of hole concentration of two extreme transistors in the tail of the distribution. The left images are for $N_D = 1.0 \times 10^{17} \text{ cm}^{-3}$ with $\Delta V_T = 71.9 \text{ mV}$. The right images are for $N_D = 8.5 \times 10^{18} \text{ cm}^{-3}$ with $\Delta V_T = 69.5 \text{ mV}$.

IV. CONCLUSIONS

The trapping of discrete charges as a result of a progressive NBTI degradation in the investigated 10 nm CMOS technology FinFETs results not only in average ΔV_T , but also in increase of

the statistical variability captured by σV_T and by other important transistor figures of merit. The NBTI induced increase of σV_T at a particular stage of degradation is dominated by the areal density of the trapped charge and depends also on the level variability in the fresh FinFETs. It is higher in the FinFETs with low channel doping and more pronounced in the case without FER at low drain bias conditions. The progressive charge trapping also results in a progressive increase in the discrepancy between the continuous doping and the average results of the ‘atomistic’ simulations. The charge trapping also results in a decorelation between the key transistor FOM, particularly in the case of low virgin variability associated at low channel doping and in the absence of FER.

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