Impact of BEOL Design on Self-heating and Reliability in Highly-scaled FinFETs

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***Abstract*— This paper investigates the impact of BEOL design on device and backend reliability – HCI, BTI, EM – due to dependence of self-heating on BEOL in highly-scaled FinFETs. Our analysis indicates that due to poor thermal coupling to substrate – in the thin fin body devices – a large part of heat flows out of BEOL. This makes self-heating, and thus device (FEOL) temperature, very sensitive to BEOL design. The heat flow through BEOL also significantly increases the metal and via temperatures. The increased temperature negatively affects the overall reliability, and one of the ways to mitigate device degradation is optimization of BEOL design.**

Keywords*— *Impact of BEOL design, Self-heating effect, Aging, HCI, BTI, EM, Reliability, FinFET

I. Introduction

Bulk FinFETs started replacing planar CMOS at 22nm because of its superior electrical characteristics [1]. Self-heating is one of the major reliability concerns in FinFETs [2], and continued scaling is only going to aggravate this issue. The large self-heating in FinFETs compared to planar devices is attributed to poor thermal coupling and reduced thermal conductivity in highly-scaled FinFETs – arising from the effects of size and surface roughness [3]. Lower thermal conductivity of thin silicon due to size effects significantly inhibits the thermal conduction to substrate, and back-end-of-line (BEOL) offers relatively lower resistive path. This means the dominant heat dissipation path is through the BEOL from the device to ambient. Because BEOL serves as a thermal path, the reliability mechanism of the device is affected by the BEOL configuration, even if it is thought to be independent. In this paper, we analyze the impact of BEOL design variation on self-heating in sub-10nm FinFETs. Our analysis indicates that BEOL design has strong impact on both device and backend temperature. And this also affects the device aging due to BTI (Bias Temperature Instability), HCI (Hot Carrier Injection) and EM (Electro-Migration).

II. Methodology

A. Device-Level Simulation

Well-calibrated TCAD and 3D FEM solver (Sentaurus Interconnect) were used to simulate SH in FEOL and BEOL. In nano-scale devices, most of the heat is generated deep inside the drain junction [4], and location of maximum heat generation is quite important to calculate accurate temperature rise. To accurately estimate the location of maximum heat generation, spherical harmonics expansions (SHE) solver of Boltzmann transport equation (BTE) was used in the device simulation. [5]

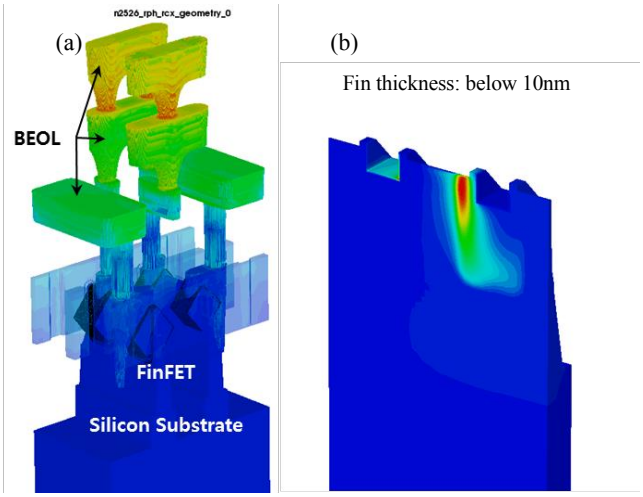

Fig. 1. (a) SI structure with BEOL (b) TCAD device structure

Moreover, in highly-scaled FinFETs, the thermal conductivity of Fin is significantly lower than its bulk counterpart due to phonon confinement [3], and thus a thickness-dependent thermal conductivity model was also employed. Fig. 1 illustrates one of the generated TCAD structures. The analysis present in this paper is for a large inverter cell – multi-fin and multi-finger inverter – at high bias values. The structure was simulated with three different top metal levels – M1, M2, and M3. Dirichlet boundary condition of T=300K was assumed at top-metal and substrate.

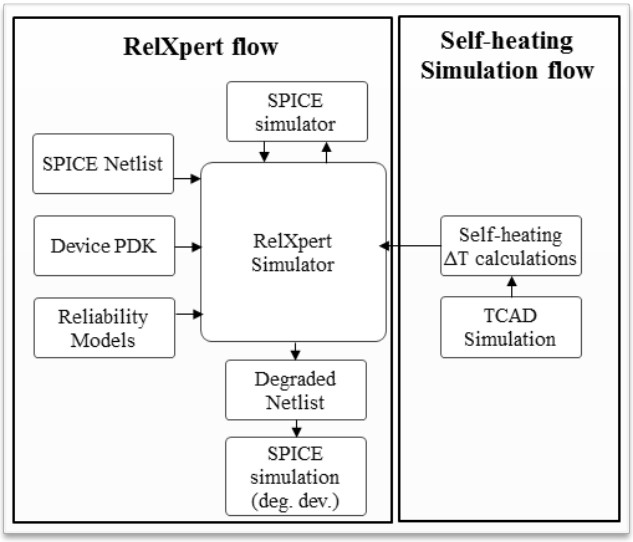

Fig. 2. Cadence-RelXpert simulation flow with self-heating.

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B. Circuit-Level Simulation

As the circuit ages, the performance degrades at some point until unacceptable. Therefore, it is important to evaluate the end-of-life (EOL) of the circuit during the initial circuit design to enable design optimization. To analyze the impact of self-heating on device aging (BTI and HCI), Cadence-RelXpert was used with modified simulation flow. Fig. 2 shows the RelXpert's simulation flow [6] augmented with self-heating simulations.

III. BEOL Impact and its Implications

A. BEOL Impact : self-heating effect in device temperature

This study focuses on highly-scaled FinFETs as shown in Fig. 1 where the heat flows over backend. Heat dissipation happens mainly by conduction of metal interconnect. A significant point is that heat transfer efficiency from the device to the top metal level is dominated by on the differences in the number of vias. Fig. 3 illustrates the 2D device temperature profile in metal-via plane. Fig. 4 shows the variation of average device temperature with number of vias (normalized), for three different top metal levels. The result shows that the device temperature exponentially increases with decreasing the number of vias. As an example, we observed a 33% reduction of device temperature by increasing the number of vias seven times. It also observed a 20% reduction while changing top metal level.

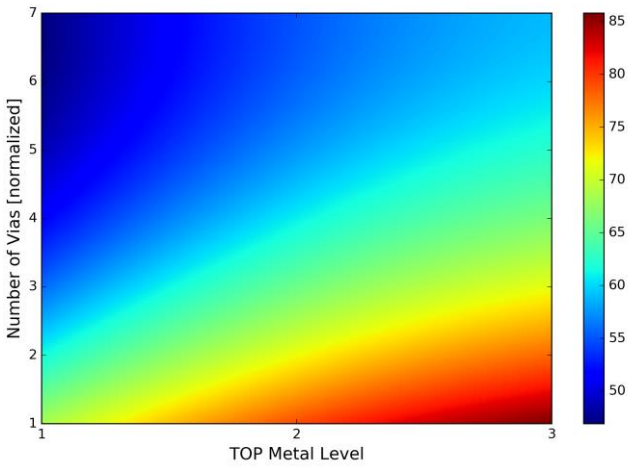

Fig. 3. Temperature profile. Surface plot of 2D thermal gradient.

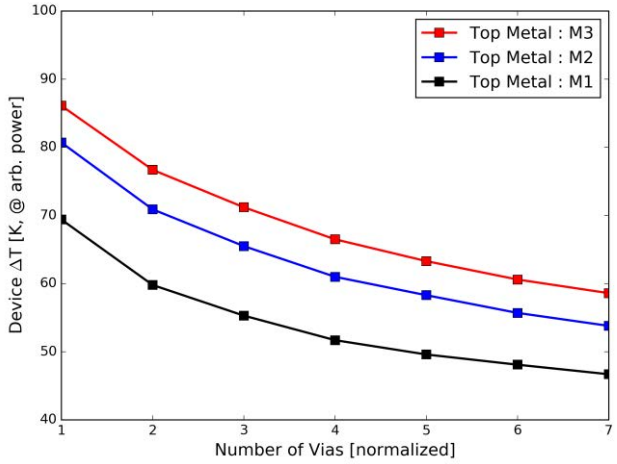

Fig. 4. Temperature with number of vias for three top metal levels.

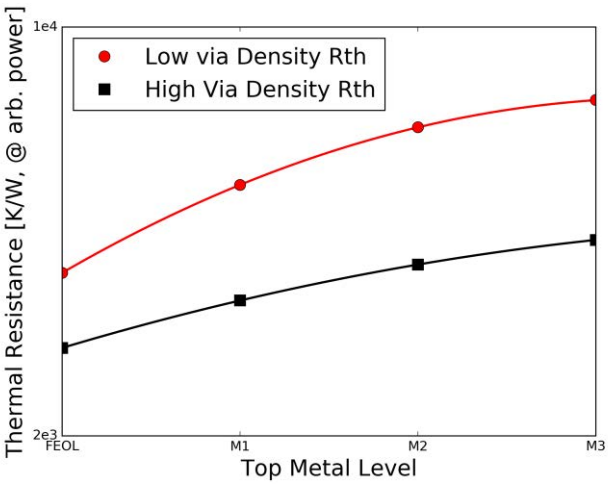

Fig. 5. Thermal resistance for three top metal levels

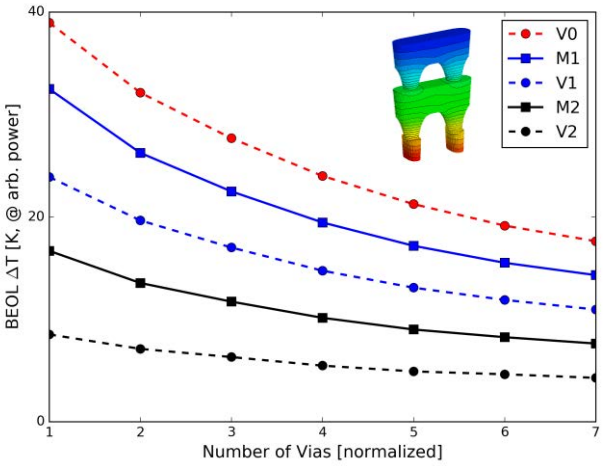

Fig. 6. BEOL Temp. of Mx and Vx layers with number of vias.

Fig. 5 shows the extracted thermal resistance value according to the stacked BEOL layer and via density, which will be used in circuit simulation. As evident from the figure, self-heating significantly reduces with number of vias and increases with top metal level. As aforementioned (in introduction section), device scaling significantly reduces the thermal conductivity of Silicon and thus heat flows mainly through BEOL since it offers lower thermal resistance. Adding additional metal layer increase the thermal resistance while increasing the via number results in the its reduction. Our analysis indicates that vias have very significant impact on self-heating, and a substantial reduction in device temperature is possible by increasing via density in the design. Since inter-layer-dielectric (ILD) has very low thermal conductivity, in highly-scaled FinFETs, vias will become "thermal-bottleneck".

B. BEOL Impact : self-heating effect in backend temperature

In addition, to studying the vertical variations in temperature at a certain inverter in the 3D structure, the temperature gradients were analyzed at different vias, as shown in Fig. 6. This figure shows the variation of average temperature of metal and via layer with number of vias. Due to heat flow through backend, metal and via temperatures also increase with increase in self-heating.

C. BEOL Impact : reliability

The most widely used method for the degradation of metal wire is Mean-Time-To-Failure (MTTF), which in case of electro-migration is modeled by Black's law:

$$MTTF = \frac{A}{J^n}\exp\left(\frac{E_a}{kT}\right) \quad (1)$$

Therefore, increase in backend temperature can lead to serious issues, since MTTF due to electro-migration exponentially decreases with increase in BEOL temperature [7]. According to (1), Fig. 7 shows that MTTF increases with increase in via density. It is thus evident that the reduction in BEOL thermal resistance is imperative for the mitigation of electro-migration.

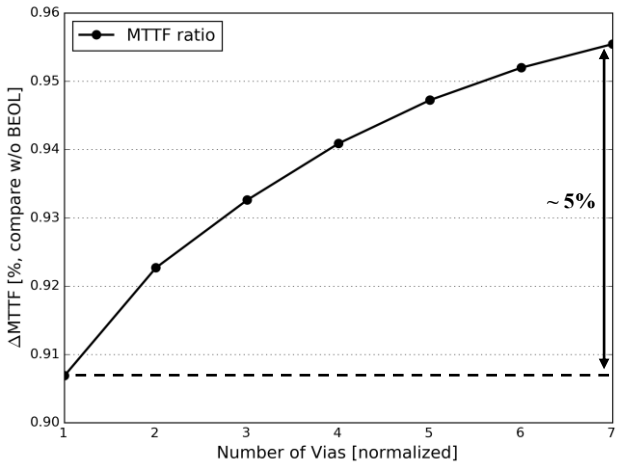

Fig. 7. MTTF degradation with number of vias for M1.

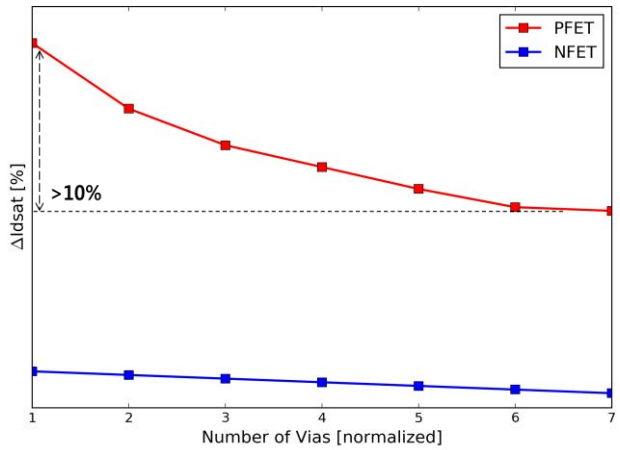

Fig. 8. Idsat degradation variation due to BEOL. NFET shows negligible variation.

Increase in temperature due to self-heating is also detrimental to device aging due to BTI and HCI. Since the device temperature is dependent upon BEOL, we studied the impact of BEOL on device aging Cadence-RelXpert [6]. Fig. 2 shows the RelXpert flow used for the simulation, the self-heating simulation results for different BEOL configurations were fed to RelXpert. The aging simulation was done for both BTI and HCI and the simulation was done for 1 year at room temperature. The temperature rise was only due to self-heating. Ideally, BEOL variations wouldn't impact the device-level reliability. But since the device temperature varies strongly with backend variation, so does the device degradation. As evident from Fig.8, more than 10% reduction in PFET drain-current degradation is possible by increasing vias in the design. For NFET, the variation is insignificant due to much lower degradation as compared to PFET.

D. BEOL Impact : self-heating effect in circuit temperature

From a thermal point of view, the main difference between the D.C. and A.C. operations is the power consumption of the internal device of the circuit, which allows the different temperature ranges with respect to the frequency. Fig. 9 and Fig. 10 show the SH simulation results of an inverter chain. The solid lines represent the device temperature with via density and the dotted lines represent the M1 temperature with via density. So, by increasing the via density and kept the top metal to M3 as shown in Fig. 10, we observed that the device temperature and M1 temperature decreased. The self-heating during A.C. circuit operation is much lower than SH during D.C. operation due to finite thermal capacity. Notice that D.C. means that current continues to flow on the device. However, heat accumulation still raises the device and backend temperature. From the figure, it's evident that the device temperature and metal layer temperature during the AC operation depends upon BEOL design.

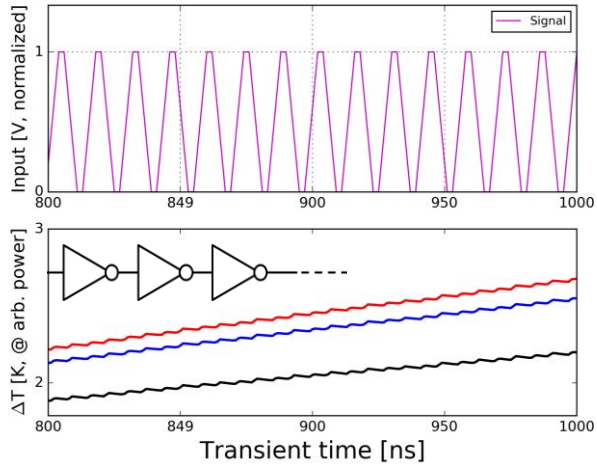

Fig. 9. Variation of the AC and self-heating over time at the inverter.

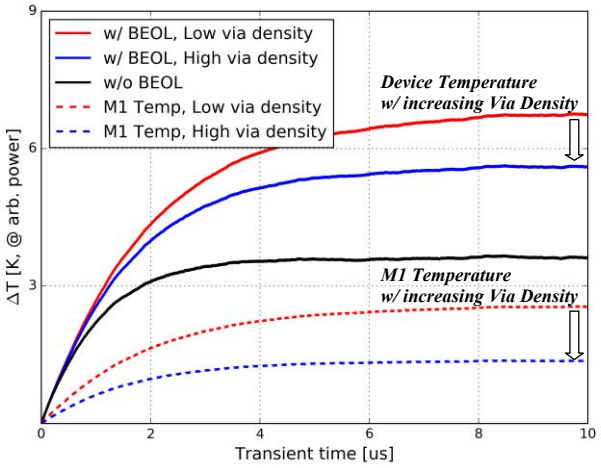

Fig. 10. Self-heating of the inverter. NFET.

IV. Conclusions

We have shown the importance of BEOL optimization for self-heating reduction in highly-scaled technologies. Our analysis indicates that significant portion of heat generated due to self-heating flows through vias and large via density is important for reduction of device temperature. We also presented that the reduction of backend thermal resistance is important for mitigation of electro-migration. Finally, we have analyzed the impact of BEOL dependent self-heating on device aging due to BTI and HCI. Thus, one way to effectively suppress increasing temperatures to improve reliability is to increase via density. As discussed earlier, the optimization of BEOL designs increases the reliability margin.

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