Scaling-aware TCAD Parameter Extraction Methodology for Mobility Prediction in Tri-gate Nanowire Transistors

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Abstract—In the simulation framework for the study of aggressively scaled CMOS transistors, it is mandatory to capture the dependence of the model parameters on the physical structure of the devices in order to perform predictive device simulations. TCAD models typically have tunable parameters to characterize physical phenomena that ultimately determine different measurable electrical quantities. In this work, we extract the density gradient quantum correction parameters and Monte Carlo scattering parameters in order to fit the C-V characteristics and the low field mobility to experimental data in the case of Tri-gate nanowire transistors, which are of high importance for the semiconductor industry. Once the relevant parameters are calibrated, we have obtained a good agreement between the experimentally measured mobility and the predictions from the Monte Carlo module of the Synopsys TCAD tool Garand.

Index Terms—Density Gradient; Monte Carlo; Remote Coulomb Scattering; Phonon Scattering; Surface Roughness Scattering; Capacitance - Voltage characteristics; Mobility; Tri-gate MOSFETs

I. INTRODUCTION

Physical models that determine the macroscopic behaviour of the field-effect transistors (FETs), such as the carrier mobility, in TCAD simulations do not scale properly with device geometry in the nanometer regime. Therefore, it is critical to capture the scaling dependence of TCAD model parameters that allow for predictive device simulations [1], [2]. After the appropriate calibration, simulation models become indispensable tools to explain the underlying physics behind the impact of scaling on FETs [3].

In this work, we present a methodology to obtain the correct mobility in Monte Carlo (MC) TCAD simulations by capturing the evolution of relevant parameters that affect the electrostatics and carrier scattering with scaling. The strategy considered combines: *(i)* the accurate device structure generation following the fabrication process; *(ii)* the density gradient (DG) based quantum correction model in three dimensional (3D) MC simulations to capture the Capacitance - Voltage (C-V) characteristics; *(iii)* the impact of the most important scattering mechanisms in fitting the experimental electron mobility. Tri-gate MOSFETs are considered in this study, as they are expected to become the transistor architecture of choice for the forthcoming CMOS technology generations [4].

The aim of this work is to show the methodology and the importance of the parameter calibration in order to capture the experimental mobility of tri-gate MOSFETs in the nanometer regime. General discussion of the device generation methodology is provided in Section II. Section III summarizes the calibration of the DG parameters to replicate the gate voltage dependence of measured inversion charge. The mobility calibration approach together with the details of the relevant scattering mechanisms implemented in the 3D MC module of Garand are given in Section IV. The comparison between

the experimental and the simulation results for the C-V characteristics and the mobility are reported in Section III and IV, respectively, including the parameter dependence on the tri-gate MOSFETs width and orientation. Finally, conclusions are drawn in Section IV.

II. METHODOLOGY

In this work, we have used the DG parameters and the MC scattering parameters for fitting the experimental results of n-type Tri-Gate nanowire transistors (NWTs) provided by CEA-LETI (Fig. 1) [5]. Initially, we have focused on the impact of the NW width (W) ranging from 8nm to 38nm, while the height (H) and the channel orientation are fixed to 11nm and [110], respectively. The rest of the technological parameters remains constant. Then, the impact of the device orientation on the electron mobility has also been studied.
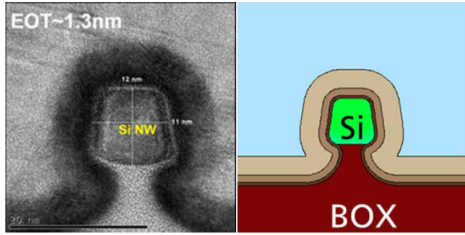

Fig. 1. Cross-sections of experimental (left) and simulated (right) Tri-gate nanowire transistor. The process simulation sequence was calibrated against TEM images provided by CEA-LETI.

Fig. 2 shows the different steps involved in this study as well as the simulation tools used at each stage. Device structures have been generated with Sentaurus Process [6] following the experimental process sequence described by Coquand et al. for Tri-gate NWT [7]. The simulated technology uses SOI substrates and features high-k/metal gates and epitaxially-grown raised S/D contacts. The process simulation sequence has been calibrated against TEM images provided by CEA-LETI, as shown exemplary in Fig. 1. Then, we have performed the C-V and mobility simulations with Garand [8] which is part of the TCAD to SPICE tool chain from Synopsys. In order to connect the device structure generated and the simulation tool, it is necessary to translate the mesh of the device to a rectilinear grid suitable for Garand through the use of the Synopsys tool SNMesh. We have curve fitted all extracted parameters to interpolate their values for any arbitrary cross-sectional width. Since the experimental data has been obtained from devices with 10 μm gate length, the long channel approximation has been adopted in the C-V and mobility simulations. It allows us to simulate only a single slice in the center of the device with periodic boundary conditions in the transport direction.

III. CAPACITANCE VOLTAGE SIMULATIONS

The main objective of this simulation has been to replicate the experimentally measured gate voltage dependence of the inversion charge. For this task, we have used drift-diffusion (DD) simulations with DG quantum corrections [9] with
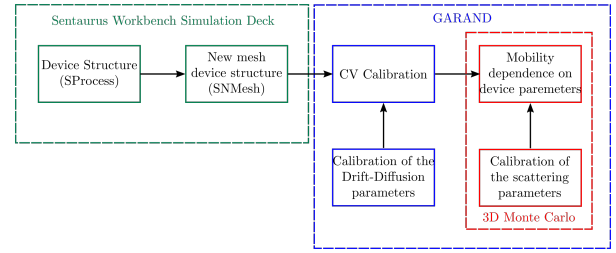

Fig. 2. Flowchart of the steps involved in the comparison between the experimental Tri-gate devices and TCAD simulations: the device structure is generated with Sentaurus Process [6]; then, the C-V and mobility simulations are performed with Garand [8] which is part of the TCAD to SPICE tool chain from Synopsys.

scaling dependent DG parameters that change with the device cross-section. The gate workfunction has been calibrated for the widest device, whereas the two density gradient masses in the confinement plane (Fig. 3(a)), and gate insulator (hafnia) permittivity (Fig. 3(b)) have been calibrated as a function of the device width. The fitting curves for each parameter as well as the equation that follows the curve are also shown. Fig. 4 illustrates the results of the C-V calibration for the devices with different cross-sectional widths showing an excellent match between the experimental data and TCAD simulations.
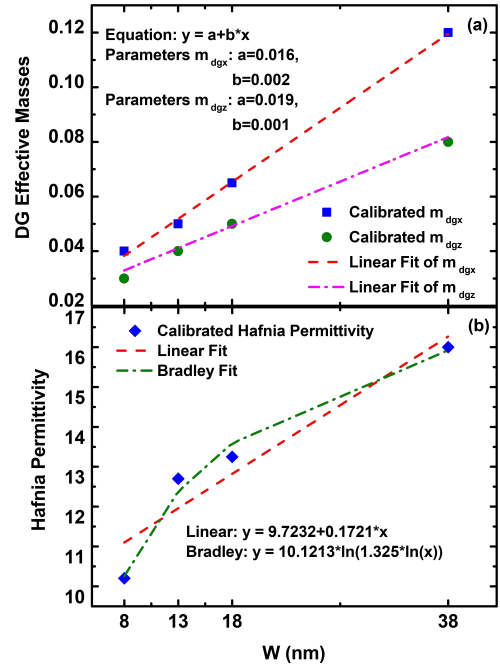

Fig. 3. Calibrated parameters for the CV simulation as a function of the Tri-gate device width (W) with [110] channel orientation: (a) density gradient effective masses, and (b) hafnia permittivity. m_{dgx} and m_{dgz} correspond to DG effective masses along the the NW height and width directions, respectively.

IV. MOBILITY CALCULATIONS

In the long channel simulations [10], the channel is assumed to be infinitely long and the electric field in the transport
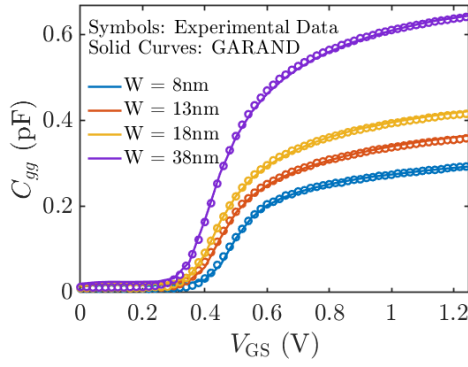
Fig. 4. Comparison of C-V curves obtained from experiments and TCAD simulations with [110] channel orientation.

direction is fixed to a low value (1kV/cm in this work). Long channel simulations provide a convenient framework for assessing low-field electron mobilities in devices with strong confinement effects, such as NWTs or FinFETs. The mobility is computed from the average velocity of the particles obtained from the MC simulations and the corresponding electric field.

We have calibrated each scattering mechanism for the particular inversion charge region in which it dominates. The following scattering mechanisms have been considered in the simulations (their detailed models as well as their expressions can be found in [8]):

- *Remote coulomb (RC) scattering* has been calibrated at low inversion charge density. This model is a general treatment of the Coulomb scattering mechanism described in [11], which assumes a metal/high-k/oxide gate stack. It simplifies the models by considering only trapped charges at the material interfaces instead of their distribution throughout the gate dielectrics. In this mechanism, the charge centroid depth (Z_D) and the trap density at the Si-SiO$_2$ have been calibrated as a function of the width. The trap density at the SiO$_2$/HfO$_2$ interface remains fixed at 1.4×10^{13} cm^{-2}.

- *Acoustic (Ac) and the optical (Op) phonon scattering* limit the maximum mobility. The Ac model treats this scattering within the elastic approximation and intra-valley transitions considering a single phonon branch [12]. In this case, we have calibrated the longitudinal and transverse Ac deformation potential ($D_{AC,Long}$=12.5eV and $D_{AC,Trans}$=9.5eV, respectively) for the widest Tri-gate device considered in the 3D MC simulations (W=38nm) and the same channel orientation as for the CV calibration [110]. We have considered Garand's default values for the 3 f-type and the 3 g-type processes for the inter-valley Op phonon parameters.

- *Surface roughness (SR) scattering* is responsible for the mobility decrease at high inversion charge density. This model is treated elastically and in the plane of the rough surface. In this mechanism, the correlation length (C_L) has been calibrated at the Si-SiO$_2$ interface as a function

of the device width and orientation, whereas the root mean square (Δ_{RMS}) has been fixed to 0.43nm.

For the studied Tri-gate transistors, we have considered that the scattering mechanisms at the top surface (001) are not affected by the reduction of the width, whereas the parameters at the sidewall interface (-110) have stronger impact with the width reduction. In particular, Fig. 5 shows the scattering parameters obtained as a result of the calibration as a function of the device width as well as the fitting curves for each parameter and the equation that follows the curve.
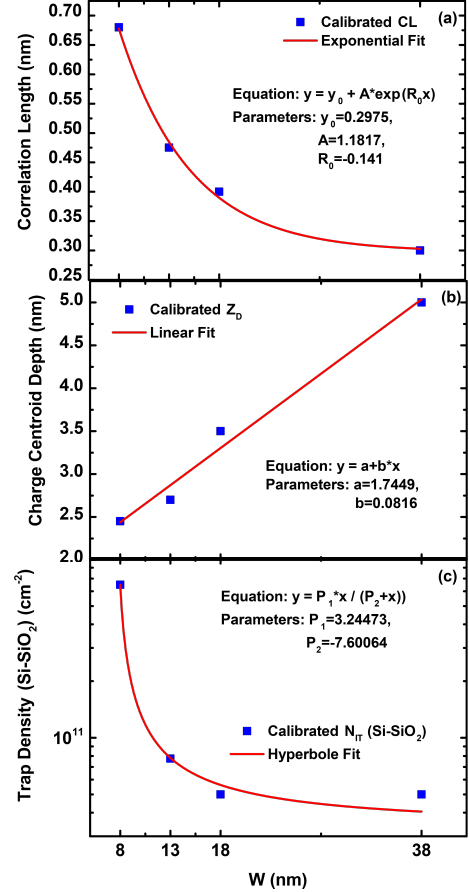

Fig. 5. Calibrated parameters for the mobility simulation as a function of the Tri-gate device width (W) for the sidewall interface and with [110] channel orientation: (a) correlation length (C_L) included in surface roughness scattering, (b) charge centroid depth (Z_D) and (c) trap density (N_{IT}) at the Si-SiO$_2$ interface included in remote coulomb scattering mechanism.

The comparison between the electron mobility as a function of the inversion charge (N_{inv}) obtained from the simulations and the experimental data for the four considered widths is depicted in Fig. 6. The inversion charge per unit area is normalized with respect to the perimeter W_{eff} of the SiNWs: W_{eff}=W+2H.

Finally, the dependence of the electron mobility on the device orientation has been investigated. In the 3D MC simulator Garand, the quantum confinement model by default takes only into account a change in the electrostatics (DG model). There is no valley splitting, and as a result, the density of
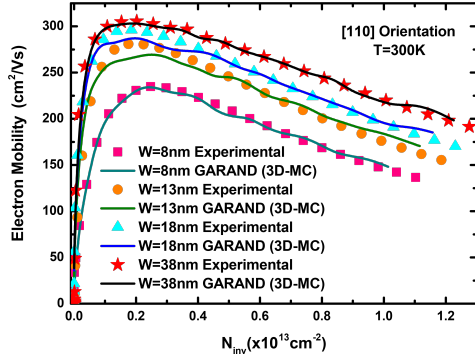
Fig. 6. Electron mobility from simulation and experiment as a function of the inversion charge (N_{inv}) for Tri-gate devices with [110] channel orientation.

Fig. 8. Electron mobility from simulation and experiment as a function of the Tri-gate device width (W) at $N_{inv}=8\times10^{12}\mathrm{cm}^{-2}$ for two channel orientations: [110] and [100].

states applied to the scattering mechanisms is unaffected by the change in orientation. Therefore, the scattering models by default are not modified in any way by a change in orientation.

Nevertheless, as the change in the crystal orientation has direct impact on the interface roughness, we have studied the modification of the C_L parameter (Fig. 7) when the channel orientation changes from [110] to [100]. Despite the identical top interface for both channel orientations, the orientation of the sidewall interface is now aligned with the principal axis changing from [-110] to [010], respectively. The rest of the scattering parameters have remained constant during this comparison.
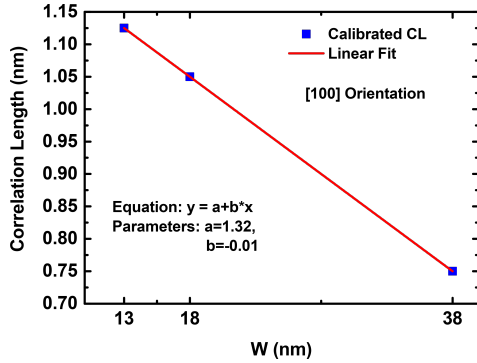

Fig. 7. Calibrated correlation length (CL) parameter included in surface roughness scattering mechanism for the mobility simulation as a function of the Tri-gate device width (W) for the sidewall interface with [100] channel orientation.

Fig. 8 shows the electron mobility enhancement for the [100] channel orientation in comparison to [110] orientation. Moreover, the mobility curve has an exponential behavior for the [110] channel orientation, and a linear behavior for the [100] orientation. This change in the calibrated C_L as a function of the channel orientation is also shown in Fig. 5(a) and Fig. 7, respectively.

V. CONCLUSIONS

In this work, based on comprehensive calibration, we have obtained width scaling dependent empirical expressions for
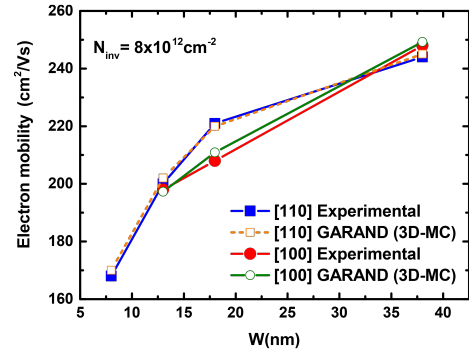
effective gate insulator permittivity, density gradient effective masses, and Monte-Carlo surface roughness and remote coulomb scattering parameters which accurately match the measured C-V characteristics and carrier mobility. The expressions can be used to predict these parameters and hence carrier mobilities in scaled Tri-gate devices with arbitrary widths and for different substrate orientations.

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