Impact of MOL/BEOL Air-Spacer on Parasitic Capacitance and Circuit Performance at 3 nm Node

Ashish Pal, Sushant Mittal, El Mehdi Bazizi, Angada Sachid, Mehdi Saremi, Benjamin Colombeau, Gaurav Thareja, Samuel Lin, Blessy Alexander, Sanjay Natarajan and Buvna Ayyagari

Applied Materials, Santa Clara, USA

***Abstract*— Impact of air-spacer at MOL and BEOL on circuit performance at 3nm technology node is studied. Our modeling results show that by introducing air-spacer at MOL and BEOL, parasitic capacitance can be reduced by 18% and circuit performance as simulated on a 31-stage ring oscillator can be improved by 6%. Other advanced parasitic improvement technologies, such as Ruthenium, also show similar performance improvement. Finally, we show that best circuit performance is achieved when these 2 technologies are combined, yielding to a circuit performance boost of 16%.**

Keywords—Air-Spacer, FinFET, ring oscillator, middle-of-line, back-end-of-line

I. INTRODUCTION

Air-spacer, also known as air-gap is an attractive option for logic technology to reduce parasitic capacitance (C_P) and increase circuit performance. Various simulation and experimental research have demonstrated air-spacers in the front-end-of-line (FEOL) transistor to improve circuit performance [1]. However, because of the presence of numerous materials, and the complexity of etch selectivity between these materials at FEOL level, semiconductor industry still has not been able to adopt the air-spacer technology at FEOL level. To utilize the concept of air-spacer, while still maintaining the integrity of other materials around it, one approach can be to introduce it at MOL (middle-of-line) and BEOL (back-end-of-line) level, where the size of the materials-set exposed to the air-spacer etch is comparatively small. Intel has already introduced air-spacer at M4 and M6 level in their 14nm technology node [2]. In this paper, we proceed one step further, introducing the air-spacer at MOL, M0 and M1 level and by studying its impact on circuit performance.

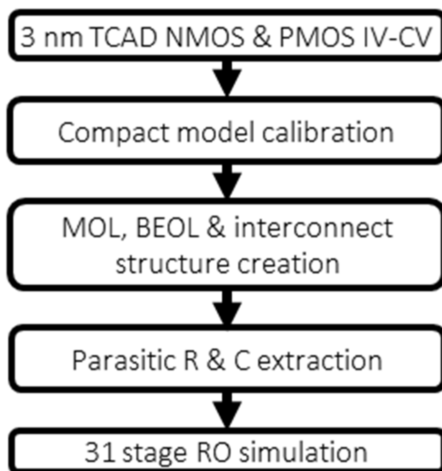

Fig. 1. Framework for 31 stage ring oscillator simulation

II. DESCRIPTION OF APPROACH

31-stage ring oscillator (RO) is used as a representative circuit to investigate the impact of air-spacer at MOL/BEOL for 3 nm technology node. The RO simulation framework is described in figure 1. First, TCAD simulations are performed for individual n-channel and p-channel FEOL FinFET devices (shown in figure 2) using typical 3nm node parameters (shown in figure 3). Then BSIM-CMG compact model is calibrated with TCAD generated current-voltage and capacitance-voltage characteristics, as shown in figure 4.

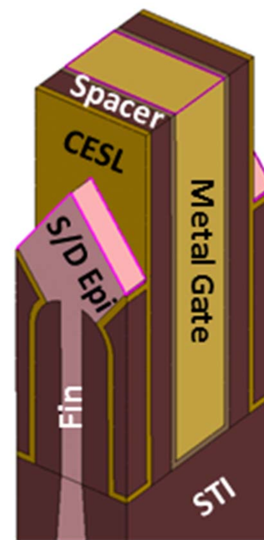

Fig. 2. FEOL FinFET structure for individual NMOS and PMOS TCAD device simulations

Parameter	Value	
Gate Pitch	45 nm	
Fin Pitch	26 nm	
Fin Width	5 nm	
Fin Height	60 nm	
Gate Length	15 nm	
Parameter	**NMOS**	**PMOS**
I_{ON}(mA/µm)	2.1	1.9
SS(mV/dec)	70.7	71.6
DIBL(mV/V)	47.4	47.9

Fig. 3. Typical FEOL dimensions used for 3 nm node FinFET, together with short-channel characteristics and on-current (at 10 nA/µm off-current).

978-1-7281-0940-4/19/$31.00 ©2019 IEEE

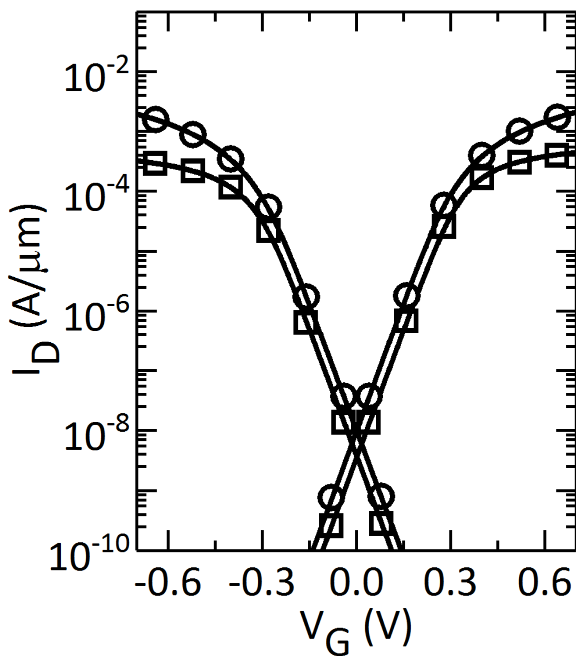

Fig. 4. Transfer characteristics of NMOS and PMOS devices from TCAD and BSIM-CMG compact model, showing the goodness of fit between those.

To model the interconnect of an inverter, a 3D structure comprising sub-contact SC or contact-plug, MOL (contact-trench CT & contact-gate CG and surrounding dielectrics) and BEOL (via-0, M0, via-1, M1 and surrounding dielectrics) is constructed, using a 3 nm inverter layout (shown in figure 5a), FinFET process flow (shown in figure 5b) and currently established material system for foundry 7nm node. The industry standard FinFET process flow is modified by inserting air-spacer modules at different levels of MOL & BEOL.

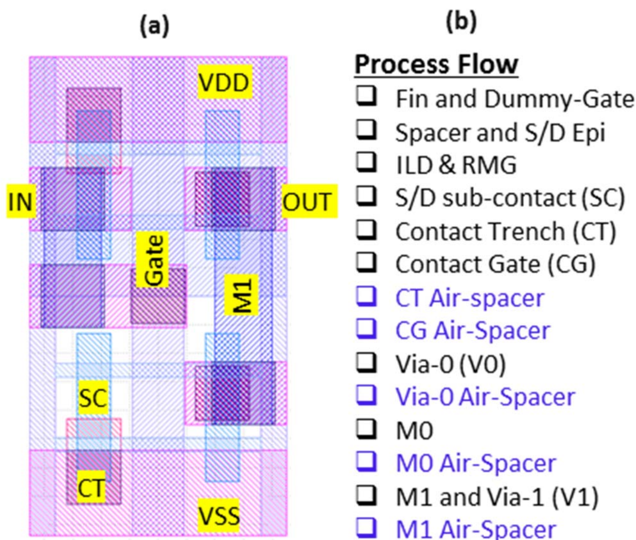

Fig. 5. (a) Inverter layout created with extrapolated 3 nm design rules. 2(b) FinFET process flow used to create 3D structures. Different air-spacer modules shown in blue font are optional.

The baseline 3D-structure (without air-spacer) is shown in figure 6. The 3D structure is used to extract interconnect parasitic resistance (R_P) and parasitic capacitance (C_P) of an inverter. For RO simulations, similar 3D structures are formed separately to model the interconnect between inverters, whose length is assumed to be 90 nm (2 gate pitch). Finally, transient simulations of RO are performed by combining 31 connected inverters as active elements, the calibrated BSIM-CMG compact model and interconnect R_P & C_P components. Stage delay of the ring oscillator is extracted and used as performance metric.

Figure 7 is a pie-chart, showing RO delay contribution of FEOL, sub-contact C_P, combined C_P and R_P of BEOL and MOL. Figure 7 does show that after FEOL device, the sub-contact C_P has maximum contribution to circuit performance, therefore justifying the effort of research community on investigating air-spacer at FEOL device.

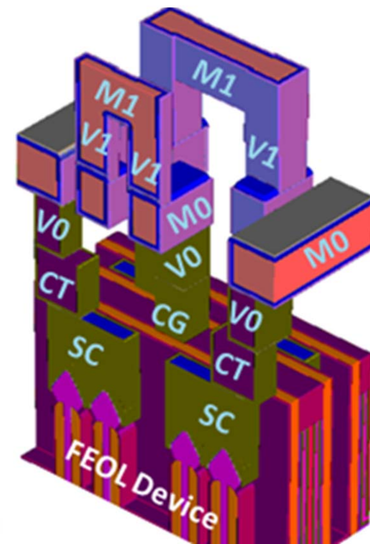

Fig. 6. Example of a 3D-structure with different layers annotated. The 3D-structure is built using the layout in and the process flow as described above. BEOL and MOL parasitic resistance and capacitances are extracted from this 3D-structure

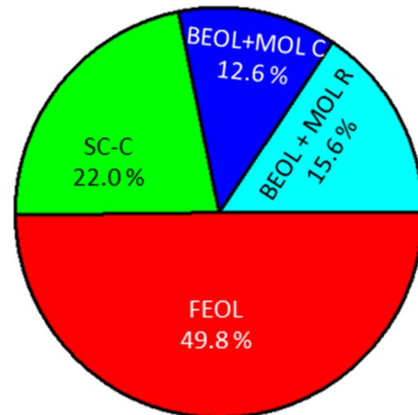

Fig. 7. Pie-chart distribution showing contribution of different elements to 31-stage ring-oscillator delay: FEOL device, sub-contact parasitic capacitance, BEOL & rest of MOL parasitic capacitance and BEOL & MOL parasitic capacitance.

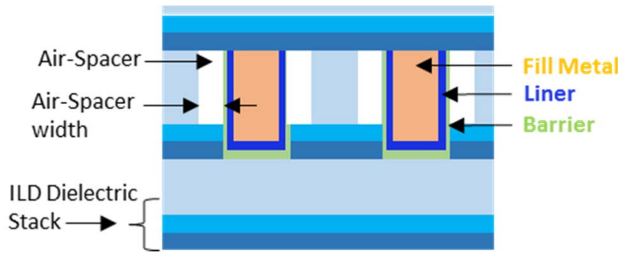

Fig. 8. Simplified air-spacer structure used in the simulations.

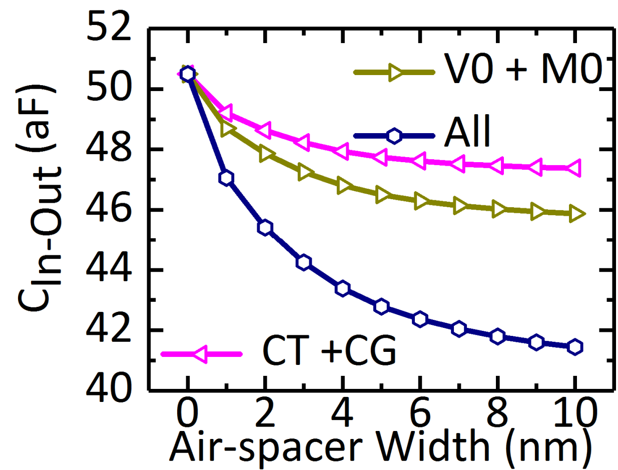

Fig. 10. Parasitic capacitance between input and output port of an inverter as a function of air-spacer width, when it is introduced at multiple locations

III. Discussions and Results

Currently significant effort is dedicated to reduce the R_P of MOL & BEOL by introducing new conductors - liners, barriers and fill metals. However, the pie-chart in figure 7 shows that MOL/BEOL C_P contributes almost equally to circuit performance, when compared to MOL/BEOL R_P. This indicates that air-spacer at MOL/BEOL can bring similar performance benefit as of advanced MOL/BEOL conductor related innovations.

For illustration, an air-spacer structure of constant spacer width is assumed, as shown in figure 8. In real fabrication process, the air-spacer might be of larger width at top and tapered at bottom. Typically, an ILD stack would consist of 3 layers, where the topmost layer, also called ULK (ultra-low K) layer is the thickest and with lowest dielectric constant. In our process emulation of air-spacer, we etch this ULK layer, selectively to the 2nd layer of the ILD stack. To understand impact of air-spacer on CP at different locations of MOL & BEOL, air-spacer is introduced separately at different stages (CG, CT, V0, M0 and M1) of the process flow, as shown in figure 5b. For each case, the air-spacer width is varied between 0 to 10nm and the parasitic capacitance between inverter's input and output port (C_{In-Out}) is extracted. Introduction of air-spacer at V0 has the largest benefit, reducing C_{In-Out} by 6% (figure 9). Air-spacer at CG and CT can reduce C_{In-Out} by 5%. On the other hand, air-spacer at M0 and M1 has relatively lower impact on C_{In-Out}, reducing it by 3%. By inserting air-spacer at multiple locations, the benefits can also be combined as shown in figure 10. Implementation of air-spacer at both V0 and M0 can reduce C_{In-Out} by 9%, whereas insertion of air-spacer at both CG and CT yields a reduction of 6%. When deployed at all MOL and BEOL level, C_{In-Out} can be reduced by about 18%, as shown in figure 10. Figure 11 shows the impact of air-spacer on RO performance, when air-spacer is introduced separately at different MOL & BEOL locations. Similar trend in RO stage delay is found as of C_{In-Out}. With air gap only at V0, RO delay can be improved by about 1.9%, whereas air-spacer at CG, CT and M0 can reduce RO delay each by 1.3%. Similar to C_{In-Out}, RO performance benefit can be further boosted by inserting air-spacer at multiple locations as shown in figure 12. With air-spacer inserted at all locations, RO delay can be reduced by about 6%.

Finally, to emphasize the performance benefit of air-spacer at BEOL technology, we compare it with other MOL/BEOL parasitic reduction technology. Among different conductors, ruthenium has shown most promises because of it lower resistivity at lower critical dimensions. Our RO simulation results (figure 13) show that when Ruthenium (with 2nm barrier) is introduced at all MOL and BEOL levels, the RO delay reduces by about 5.6%, a similar performance improvement figure as of air-spacer. Furthermore, we show

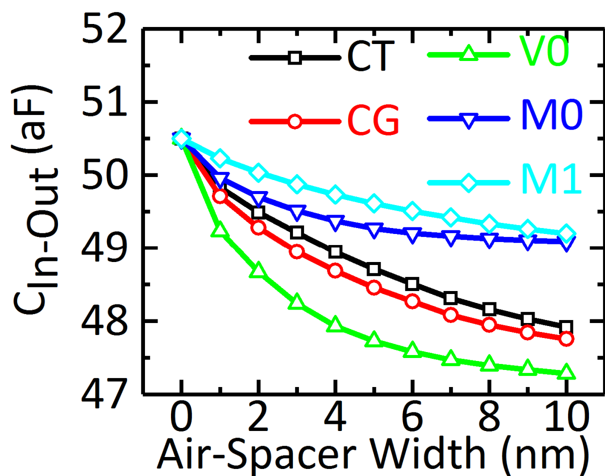

Fig. 9. Parasitic capacitance between input and output port of an inverter as a function of air-spacer width, when it is introduced at only at one location

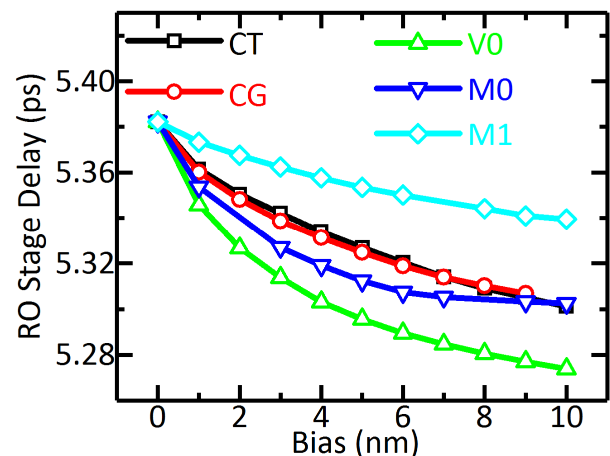

Fig. 11. Ring-Oscillator delay as a function of air-spacer width when air-spacer is introduced only at one location.

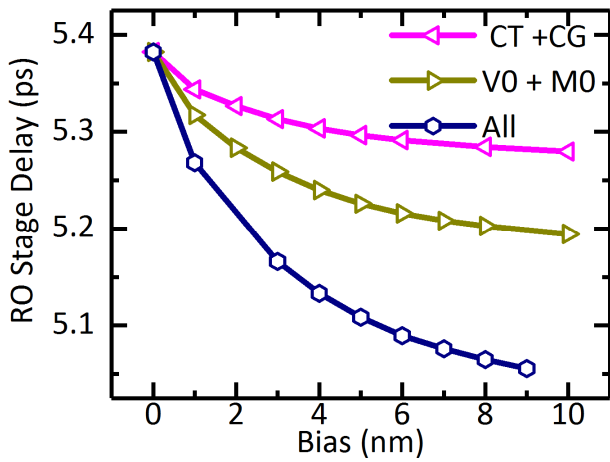

Fig. 12. Ring-Oscillator delay as a function of air-spacer width when at multiple locations of the FinFET process flow

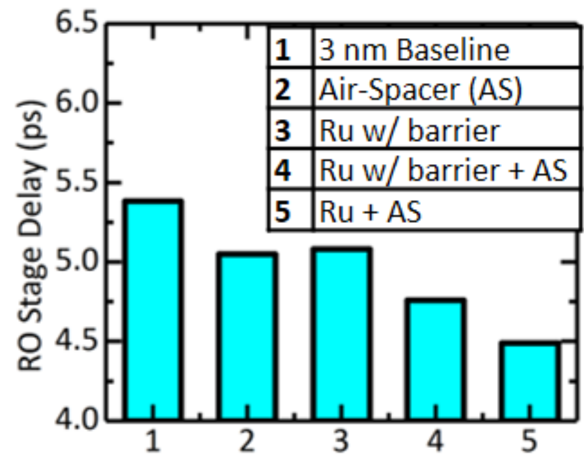

Fig. 13. Comparison of RO performance with air-spacer (AS) technology and Ruthenium (Ru)-based systems. Ru and air-spacer technology, when combined give best circuit-level performance. An air-spacer width of 10nm is used for these simulations.

that Ru and air-spacer technologies can be combined to reduce both MOL/BEOL R_P and C_P, achieving a circuit performance benefit of about 11%. The circuit performance can be further boosted by using air-spacer and eliminating the barrier for Ru, as demonstrated recently [3], since because of the air-spacer, Ru cannot diffuse in surrounding ILD dielectric. Combining barrier-less Ru and air-spacer technology, a maximum circuit performance benefit of about 16% can be achieved, which is difficult to obtain just by using Ruthenium technology alone.

References

[1] K. Cheng et al, "Air spacer for 10nm FinFET CMOS and beyond", in IEEE International Electron Devices Meeting (IEDM), pp. 17.1.1 – 17.1.4, Dec 2016

[2] S. Natarajan et al, "A 14nm Logic Technology Featuring 2nd-Generation FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588 µm² SRAM cell size," in IEEE Internaional Electron Device Meeting (IEDM), pp. 3.7.1 – 3.7.3, Dec 2014

[3] K. Croes et al, "Interconnect metals beyond copper: reliability challenges and opportunities," in IEEE Internaional Electron Device Meeting (IEDM), pp. 5.3.1 – 5.3.4, Dec 2018