Leakage Performance Improvement in Multi-Bridge-Channel Field Effect Transistor (MBCFET) by Adding Core Insulator Layer

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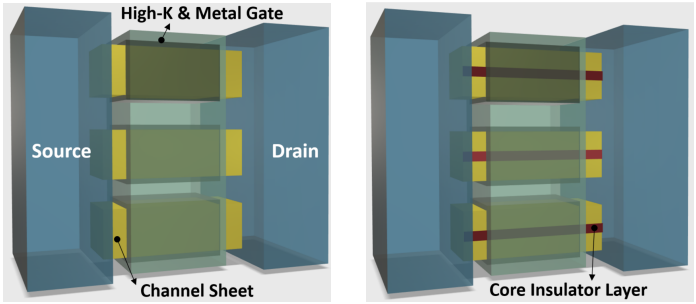
***Abstract*—Altering from existing planar devices to FinFETs has revolutionized device performance, but demands of leakage and gate controllability are increasing relentlessly. Gate all around field effect transistor (GAAFET) is expected to be the next-generation device that meets these needs. This paper suggests a way to improve the gate electrostatic characteristics by adding an oxidation process to the conventional multi-bridge-channel field effect transistor (MBCFET) process. The main advantage of the proposed method is that a device with ultimate electrostatic properties can be implemented without changing the complex and expensive photo-patterning. In the proposed device, the immunity of short channel effects is enhanced in a single transistor. And the performance of ring oscillator (RO) and SRAM was confirmed to be improved by Sentaurus technology computer aided design (TCAD) mixed-mode simulation.**

***Index Terms*—Gate-all-around FET, Transistor leakage, Insulator, Gate controllability, Electrostatic potential, MBCFET.**

I. INTRODUCTION

Although changes from planar 2D devices to FinFET have revolutionized device performance, demands of leakage and gate controllability are growing more rapidly. So recently, FinFET faces many challenges, such as high cost of scaling, performance limitation, process variation immunity, process difficulty for steep fins [1-3]. While operating voltage should continue to decrease for longer battery times, nevertheless the performance of the product should be superior to that of the existing product. Almost all of the FinFET problems are expected to be dramatically solved with gate all around field effect transistor (GAAFET) [4-5]. However, as FinFET did in the past, GAAFET will face limitations that cannot satisfy the demands of better properties. Therefore, it is still mandatory to improve leakage and electrostatic characteristics. This paper proposes a method to improve the leakage and gate electrostatic characteristics of the device by adding an oxidation layer to multi bridge-channel-field effect transistor (MBCFET) which is the most promising next-generation device. The proposed method in this study can be applied to existing MBCFET processes with less effort and can improve the electrostatic properties without tuning the complex and expensive photo-patterning process.

978-1-7281-0940-4$31.00



(a) (b)

Fig. 1: Structure comparison. (a) Conventional MBCFET, (b) Core insulator MBCFET.

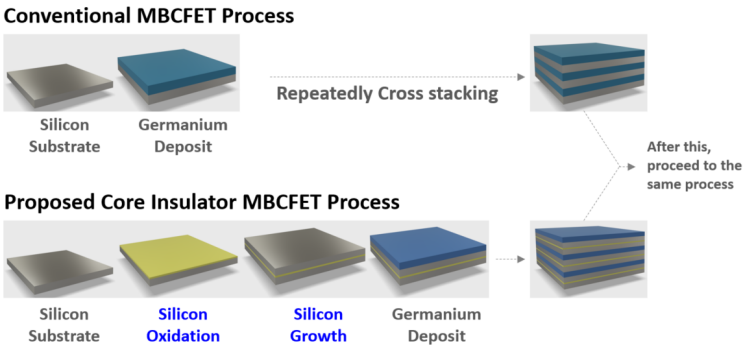
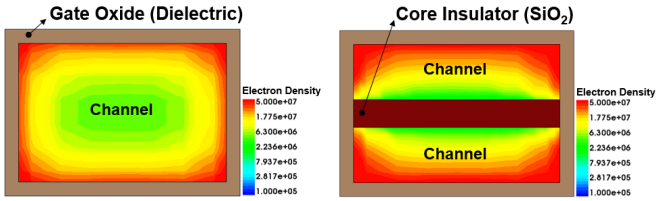


Fig. 2: Process flow comparison.

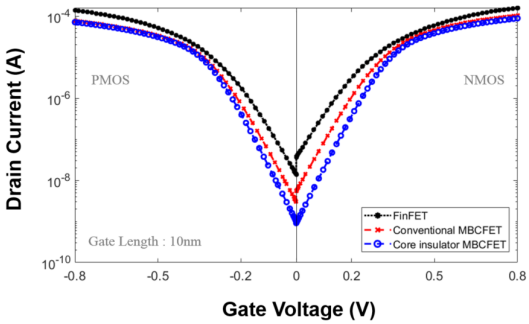
II. DEVICE STRUCTURE AND SIMULATION APPROACH

Fig. 1 (a) shows the conventional MBCFET and fig. 1 (b) shows the proposed core insulator MBCFET. Compared to



(a) (b)

Fig. 3: Channel cross-sectional view of electron current density. (a) Conventional MBCFET. (b) Core insulator MBCFET.



(a)

Fig. 4: Comparing the I_d-V_g curves of NMOS and PMOS.

the conventional MBCFET, the proposed device has a thin oxidation layer in the core of the channel. And equally, the HfO_2 gate oxide and metal gate surround the channel on four sides, including the core oxide layer [6]. Fig. 2 is a process sequence for implementing this MBCFET structure. The conventional MBCFET is created through cross-stack silicon and silicon-germanium (SiGe) and implements channel by removing only the SiGe layer using the selective etching ratio between two layers [7-8]. Then a thermal oxidation step is added in the middle of this process to create an insulating layer between silicon and silicon. Increasing the distance from the gate electrode reduces the effect of gate bias on the channel, which degrades gate controllability and leakage characteristics. Fig. 3 (a), cross-sectional view of electron density in the conventional MBCFET, shows that the closer the gate electrodes, the higher the electron density, and the farther away the less the effect of the gate biases. Fig. 3 (b) is the same view of the proposed core insulator MBCFET. The core insulator MBCFET improves electrostatic properties by effectively removing poor gate control area. Creating the channel very thin for device characteristics increases device variation with the damage of silicon when SiGe is etched [9]. As the process continues to scale, it is becoming much more difficult to form a very thin channel. By inserting the insulator in the core of the channel, it can have the effect that a very thin channel is implemented. This improved method is difficult to use in the FinFET process. The reason is that it is quite difficult to etch a very thin fin core that has already been formed by the shallow trench process [10]. On the other hand, in the MBCFET process, which forms channels later through selective etch after cross-stacking of silicon and SiGe, it is easy to insert another layer in the middle.

TABLE I: Parameters of transistors

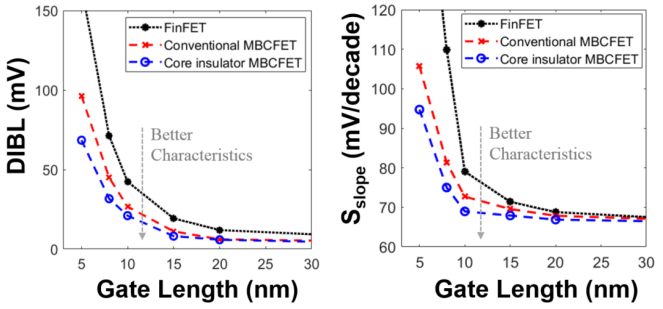
	FinFET	Normal MBCET	Core Insulator MBCFET
Gate Length	5-90nm	5-90nm	5-90nm
Channel Height (Fin Width)	10nm	10nm	10nm
Channel Width (Fin Height)	45nm	15nm	15nm
Gate Oxide Thickness	2nm	2nm	2nm
Operating Volatage	0.8V	0.8V	0.8V
Channel Doping Concentration	5e17	5e17	5e17
S/D Doping Concentration	2e20	2e20	2e20
Workfunction of NMOS	4.45eV	4.45eV	4.45eV
Workfunction of PMOS	4.85eV	4.85eV	4.85eV

Based on this idea, technology computer-aided design (TCAD) simulation was conducted with MBCFET, which will be used in of 3nm process and lower. TCAD simulator was used with various physics models to electrically analyze the characteristics of transistors ; Trap-assisted Auger recombination model was applied to analyze the electrical characteristics of highly doped devices and the Shockley-Read-Hall (SRH) model was applied to estimate the carrier generation and recombination mechanism for estimating doping-dependent device characteristics [11]. The physical and electrical specifications of the device used for the simulation are given in Table 1. In order to analyze to short channel effects immunity, it is used as a characteristic indicator of drain induced barrier lowering (DIBL) and subthreshold slope (S_{slope}).

III. Single Transistor Simulation Results

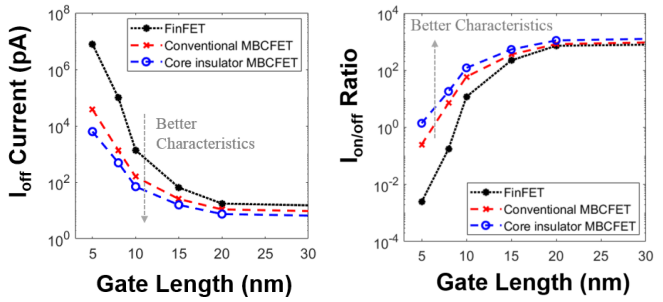
Fig. 4 shows the correlation between the gate bias (V_g) and the drain current (I_d). The left side shows the characteristics of the PMOS and the right side shows the that of the NMOS. The steeper the curve of the I_d-V_g, the better electrostatic properties. Analysis of the data shows that the core insulator MBCFET has the best switching characteristics. In order to analyze short channel effects immunity in detail, we compared DIBL and S_{slope} characteristics according to gate length as shown in fig. 5. Fig. 5 (a) shows the DIBL according to the gate length and fig. 5 (b) is that of the S_{slope}. The proposed core insulator MBCFET has 29.5% better DIBL compared to the conventional MBCFET, 55.5% improvement compared with the FinFET and S_{slope} improvement is 5.9% compared to the conventional MBCFET and more than 40% compared to FinFET at 8nm gate length. The immunity of short channel effects, represented by the DIBL and S_{slope}, improved at the proposed device because it effectively removed the poor gate control area by using an insulating. Because short channel effects increase exponentially as the gate length is shortened, the advantages of the proposed device are increased significantly. It means that even if the gate length is shortened, the device can have robust and mass-productive properties [12].

As shown in fig. 6, leakage characteristics also be improved by inserting a core insulator. Fig. 6 (a) shows the relationship



(a) (b)

Fig. 5: Gate length dependency of short channel effects characteristics. (a) DIBL. (b) S_{slope}.



(a) (b)

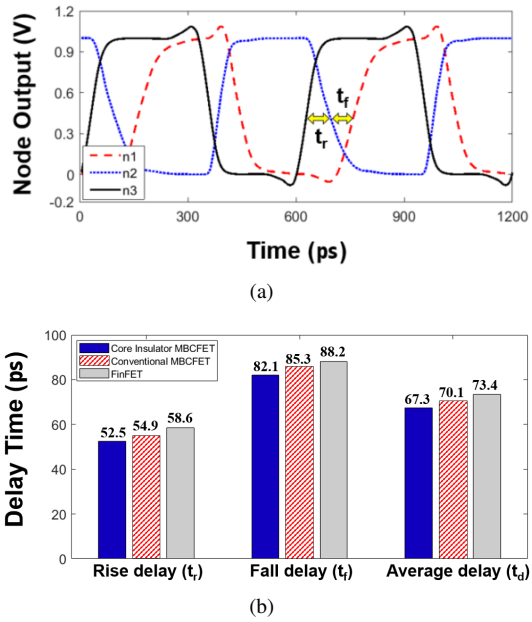
Fig. 6: Leakage characteristics. (a) I_{off}-L_g dependency. (b) $I_{on/off}$-L_g ratio dependency.

between gate length and leakage current (I_{off}), and fig. 6 (b) shows the ratio on drive and leakage current ($I_{on/off}$) for checking the risk of I_{on} reduction. In fig. 6 (a), although leakage current (I_{off}) increased exponentially at short gate lengths in the three devices in common, I_{off} of the proposed device increases less extremely than that of other devices. Also, as shown in fig. 6 (b), the $I_{on/off}$ characteristics of the proposed device were superior to that of other transistors. The main components of the transistor leakage are subthreshold leakage due to minority carrier diffusion, gate leakage from dielectric tunneling and junction leakage due to reverse bias. The reason for the good result of the $I_{on/off}$ in the proposed device is that it reduces the area of the channel with the insulator to lower the subthreshold leakage. At the same time, it increases the sensitivity to the gate bias, thus suppressing the reduction of I_{on} as much as possible.

IV. Mixed-mode Simulation Results

A. Ring Oscillator Simulation Results

In this subsection, we analyzed the improvement of logic circuit composed of NMOS and PMOS using TCAD mixed-mode simulation. First, we compared the performance of ring oscillator (RO) which is the basis of design in a lot of applications. The experiment consisted of a 3 stage RO



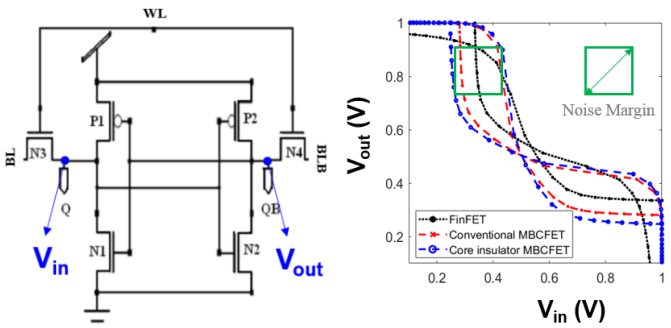
(a) (b)

Fig. 7: RO simulation results. (a) Time domain output waveform. (b) Delay comparisons.

consisting of three transistors, respectively, to analyze the change in delay. Fig. 7 (a) is a graph of the output waveform of RO configured with the proposed device. The rise delay (t_r) and fall delay (t_f) were measured based on 0.5 * VDD and the average delay (t_d) was calculated as t_d = (t_r + t_f) / 2 [13]. Fig. 7 (b) compares the delay times between the three devices. The average delay of the core insulator RO is improved by 4.0% compared with the conventional MBCFET RO and 8.3% improved compared with the FinFET RO. The reason for this improvement is that the leakage of off-state transistors improves the overall switching performance of the inverter.

B. SRAM Simulation Results

Static random access memory (SRAM) is a logic circuit that is as important as an RO in an actual logic integrated circuit chip. Since the SRAM carries out its role as a cache memory in the application processor requiring a high-speed operation, the speed of the memory itself is very important for the performance of the entire product. SRAM is generally implemented with four NMOS and two PMOS devices as shown in fig. 8 (a). When the word line (WL) enable signal is applied to read or write data, the current flows from the precharged bit line (BL) to the SRAM bit cell [14]. If the current from this BL cannot be sent to the ground sufficiently, the existing cell data can be flipped. This failure mechanism is called disturb fail. And SRAM noise margin is a indicator that tests and extracts at this environment. SRAM noise margin is measured by a butterfly curve resulting from sweeping V_{in} and V_{out} across the half-cells of the SRAM. The higher the



(a) (b)

Fig. 8: SRAM simulations. (a) Circuit schematic of SRAM. (b) Comparison of SRAM noise margin.

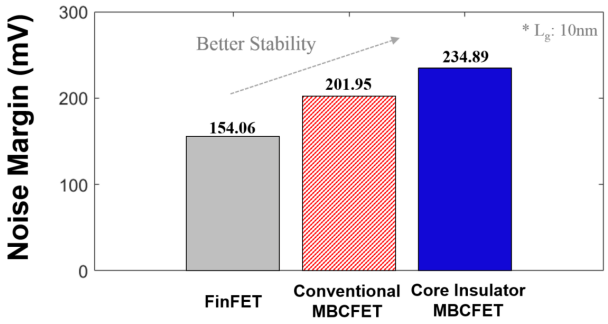


Fig. 9: Noise margin comparison in SRAM.

noise margin value, the more stable the cell can store data. Fig. 8 (b) shows the superposition of the butterfly curves of SRAMs made with three devices. In order to obtain a superior noise margin, the switching characteristics should be improved, and the leakage current in the off state have to be suppressed. Fig. 8 (b) shows that SRAM with the proposed device has better noise margin. For a more quantitative analysis, fig. 9 shows a 16.3% improvement in the SRAM implemented using the core insulator compared with conventional MBCFET SRAM and more than 40% improved compared with the FinFET SRAM. Higher tolerance to the disturb failure can significantly improve the overall memory speed because fewer redundancy repair circuits are used in the event of a memory failure.

V. Conclusions

The electrostatic and leakage properties of the GAAFET is expected to be further improved, but the relentless requirement demand will exceed the performance limit of general GAAFET device. So, the needs for research on better electrostatic performance are never reduced. Most applications are designed with a combination of devices with a high drive current or good leakage control. Generally, these types of devices are implemented by diversifying the gate length by tunning the photo-patterning process. Tuning the patterning involves increasing process complexity and costs. In this paper, it was confirmed that the leakage and electrostatic characteristics were improved through simple oxidation process addition. The most attractive point is that it can achieve better device performance through a simple oxidation without changing a difficult photo-patterning. Furthermore, as the device continues to scale, the proposed device can get higher resistance to process variation than photo-patterning method in terms of controlling the short channel effects. It is also meaningful to verify progress in composite devices such as RO and SRAM. In this study, we concluded that the proposed method can suppress leakage current without significantly reducing the driving current through the core insulator.

VI. Acknowledgement

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. NRF-2017R1A2B2003240). The TCAD tools were supported by the IC Design Edu-cation Center (IDEC).

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