Modeling of Temperature-Dependent MOSFET Aging

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***Abstract*—We have modeled MOSFET-device aging based on the trap-density increase, which is included in the Poisson equation to consider aging explicitly and physically correct. To preserve consistency, the Poisson equation is solved iteratively. Measured temperature dependence of aged *I-V* characteristics are well reproduced with implementation of this aging model into the industry-standard model HiSIM. The extracted physical device quantities with the developed model from measurements have been investigated to characterize the aging features. It is observed that the activation energy E_a as a function of V_{gs} is nearly identical for non-aged and aged devices. This concludes that the temperature dependence of aging originates mostly from the temperature-dependent electrostatic potential, resulting in negligible temperature dependency of extracted trap density N_{trap}. To generalize the conclusion, 2D-device simulation is investigated for a double-gate (DG) MOSFET with increased stress-induced trap density. The same results as obtained from measurements are achieved, namely the activation energy is nearly identical for either non-aged or aged cases. This concludes that the temperature dependence of device aging can be accurately predicted using the temperature-dependent *I-V* characteristics of non-aged device.**

Keywords—MOSFET aging, Temperature Dependence, Trap-density increase, bulk MOSFET, Double-Gate MOSFET

I. INTRODUCTION

Stress applied to devices during circuit operation induces a trap-density N_{trap} increase at the insulator/substrate interface, which is the origin of MOSFET aging [1]. Our investigation focuses on nMOSFET aging, where hot carriers are responsible for the N_{trap} increase. Particular focus is given on the temperature-dependent device aging, to determine whether the N_{trap} increases as the temperature increases. It has been shown that the trap-time constant is temperature dependent, reducing with increased temperature [2]. The emission-time constant shows the same characteristic. This is important for circuit simulation. However, investigations for aging of real device after stress duration with different temperatures have not been done yet. Our purpose here is to analyze the measured temperature dependence of aged *I-V* characteristics on the basis of the trap density. The temperature dependence of the trap density will be analyzed, to determine whether the temperature dependency can be written only by the temperature-dependent physical quantity of the thermal voltage. In this work aged *I-V* characteristics of a leading-edge bulk MOSFET are studied with use of the developed aging model, which considers the trap density explicitly within the Poisson equation. The investigation is further extended to a multi-gate technology to verify whether the obtained results are still valid for this advanced generation.

II. ANALISYS OF TEMPERATURE-DEPENDENT AGING

Fig. 1 shows measured I_{ds}-V_{gs} characteristics at low drain voltage (V_{ds}) after enhanced stress duration at different temperatures of 25, 85 and 125°C. A leading-edge 50nm CMOS technology is applied for the device fabrication. Figs. 1a and b show the transfer characteristics at room temperature in semi-log and linear scale, respectively. Enhanced stress conditions are also applied with different duration time at different temperatures. The device aging is clearly observed in the subthreshold region, while the device characteristics are mostly governed by the carrier scattering in the high field, induced by V_{gs} for the strong inversion condition. Additionally, it is seen that the aging is enhanced for elevated temperatures, as shown in Figs. 1c and d.

The measured I_{ds}-V_{gs} characteristics are studied with the compact model HiSIM, where the trap density is explicitly considered in the Poisson equation as [3, 4]

$$\nabla\phi^2 = -q/\varepsilon_S \cdot \left(p - n + N_D^+ - N_A^- - N_{trap}^-\right) \quad (1)$$

$$N_{trap} = N_0 \exp\left[\left(E_F - E_C\right)/E_S\right] \quad (2)$$

$$N_0 = g_C \cdot E_S \cdot kT/E_S \big/ \sin\left(kT/E_S\right) \quad (3)$$

$$E_F - E_C = -\left[qV_{ds} - q\phi_S + \left(E_C - E_V\right) - E_V - kT\ln\left(N_V/N_A\right)\right] \quad (4)$$

where only the acceptor-type trap N_{trap} is considered. Above equations are solved iteratively to obtain a consistent solution of the static potential distribution ϕ. N_{trap} includes the thermal energy and the bandgap, which induces a temperature dependence.

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The parameter extraction is performed with HiSIM including the N_{trap} increase due to the applied stress conditions [3]. The stress is modeled as a function of the integrated substrate current, reflecting the stress condition, during the stress duration. In the HiSIM model the temperature dependence is modeled by physical quantities, as listed in Table 1, which are identical with the 2D-device simulation treatment. All measured temperature dependences of the unstressed-device performances are well reproduced, as demonstrated in Fig. 2a for two V_{ds} values. It is further seen that good temperature-dependence reproduction in the subthreshold region is nearly exclusively due to the contributions from thermal voltage and band-gap, while the phonon scattering is responsible for data reproduction under the strong-inversion condition. As verified in Fig. 2 the aged measurements can also be reproduced with the same temperature dependence of the trap density, which is modeled only by the thermal-energy and band-gap differences. Fig. 3 compares the measured transfer characteristics after stress at high temperature for low applied V_{ds} to the model-calculation results. A good agreement for all aged I-V characteristics verifies that the temperature dependence of the trap density can be written only by the thermal energy and band-gap dependences as it has been expected. This simplifies the model development for circuit simulation as well as increases the reliability of the circuit simulation.

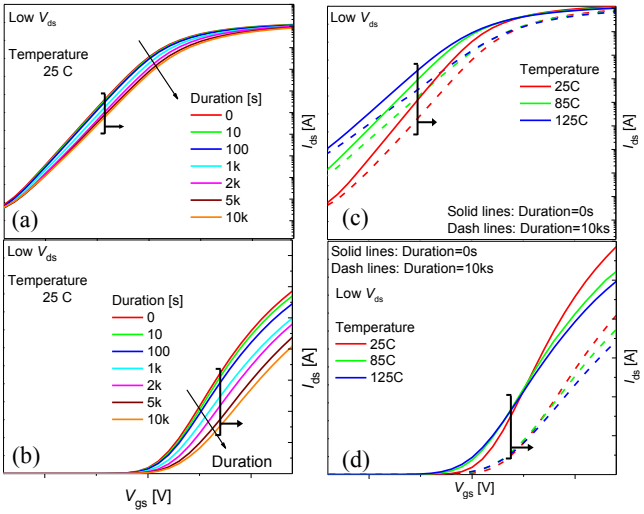


Fig. 1. Measured drain current (I_{ds}) characteristics of the studied device with aging are shown in (a) semilog and (b) linear scale at low V_{ds}. Aged and not aged I_{ds}-V_{gs} measurements for temperatures of 25, 85 and 125C are shown in (c) semilog and (d) linear scale at low V_{ds} .

TABLE I. TEMPERATURE DEPENDENT PHYSICAL QUANTITIES

Physical Quantity	**Value**[a]
Thermal voltage	$\beta^{-1}=kT/q$
Band-gap	$E_g = E_{g0} + \mathbf{BGTMP1} \cdot X1 + \mathbf{BGTMP2} \cdot X2$ $X1 = T - \mathrm{TNOM}\ ;\ X2 = T^2 - \mathrm{TNOM}^2$
Intrinsic Carrier concentration	$n_i = \sqrt{N_C \cdot N_V} \cdot \exp(-\beta E_g/2)$
Velocity saturation	$v_{sat} = \dfrac{\mathbf{VMAX}}{1.8 + 0.4X1 + 0.1X1^2 - \mathbf{VTMP}(1 - X1)}$
Phonon Mobility	$\mu_{ph} = \mu_{ph0} \cdot X1^{\mathbf{MUETMP}}$
Substrate current	$I_{sub} = I_{sub0} \cdot (1 + \mathbf{SUBTMP} \cdot X1)$

[a] TNOM is the nominal temperature, N_C and N_V are the densities of states in the conduction and valence band, respectively. E_{g0} is the band-gap value at 0K. μ_{ph0} and I_{sub0} are the phonon mobility and substrate current at nominal temperature, respectively. BGTMP1, BGTMP2, VMAX, VTMP, MUETMP and SUBTMP are model parameters

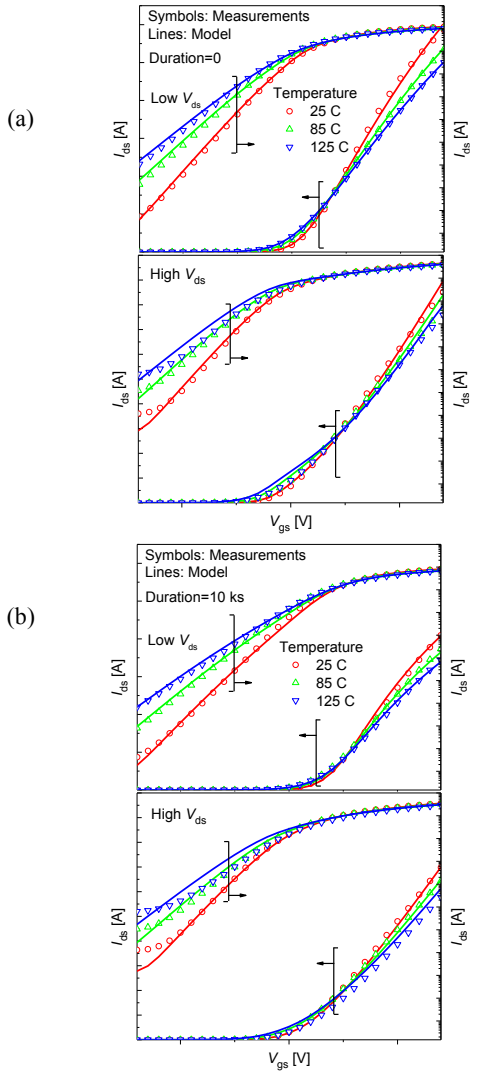


Fig. 2. Comparison of measurements and modeled results for different temperatures of (a) an unstressed device and of (b) a device with degradation time of 10ks at low and high V_{ds}.

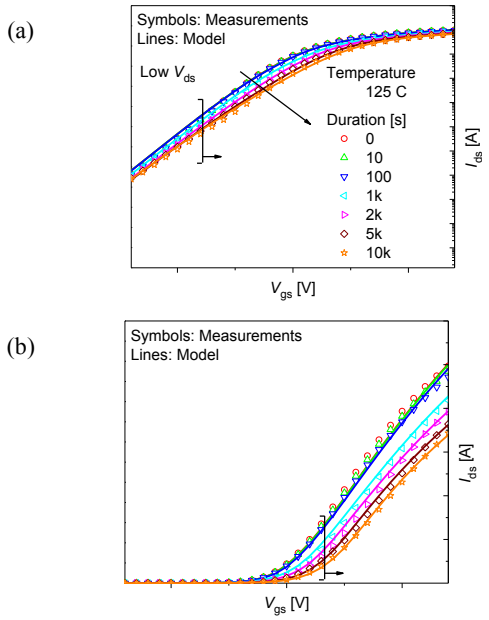


Fig. 3. Comparison of measurements and the best fit of modeled aging results for several degradation times at temperature of 125C for low V_{ds} in (a) semilog and (b) linear scale.

III. Temperature-Dependent Trap Density

The extracted trap-density increase with measured *I-V* characteristics is investigated in detail here. Fig. 4a shows extracted density of state (DoS) distributions within the band-gap for different stress durations under a constant stress bias at different temperatures. Here N_{trap} is the multiplication of the intercept with conduction-band edge E_C and the inverse of the gradient of the logarithmic DoS plot, as can be seen in Eq. 2 [5, 6]. The gradients of the DoS-curves in Fig. 4a also effectively determine the V_{gs} dependence of N_{trap}. It can be seen that the N_{trap} increase starts to saturate for long stress durations. In spite of the quite drastic DoS increase as a function of the stress magnitude, the stress-temperature dependency remains at a practically negligible level, as can be seen in zoomed Fig. 4b. This temperature dependence is caused by the thermal-voltage and band-gap changes in the extracted results for all stress conditions. The stress estimation, used for modeling the trap-density increase, is done with the substrate current, which is strongly dependent on the temperature. For the DoS extraction this dependency must be ignored to reproduce the measurements. The reason could be that the hot electrons suffer from the very high scattering probability as observed in the drain current. Thus not all of the hot carriers can contribute to the trapping but only lucky carriers. A trap/detrap-time-constant reduction could be also the reason. Anyway, our result concludes that the trapping probability does not increase, in spite of the hot carrier increase.

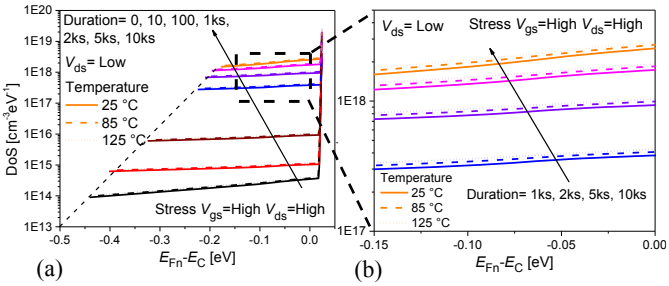


Fig. 4. (a) Density-of State (DoS) increase *vs.* energy difference between the Fermi level and the conduction band, $E_{Fn} - E_C$, for several degradation times and different temperatures at low V_{ds}. (b) Zoom of the selected upper-right range of Fig. 4a.

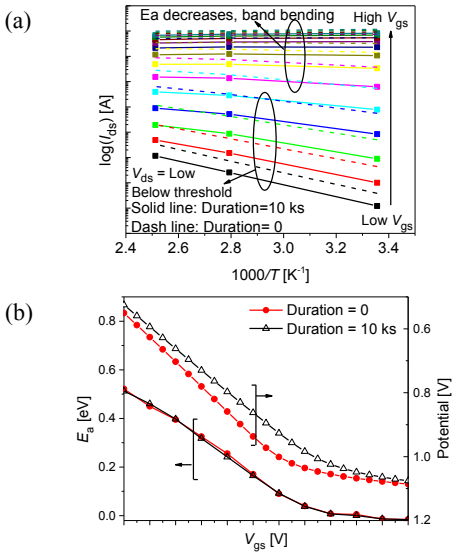


Fig. 5. (a) Temperature dependence of drain current with/without stress for a bulk device. (b) Activation energy as a function of V_{gs} for bulk device and source potential for degradation times of 0 and 10ks.

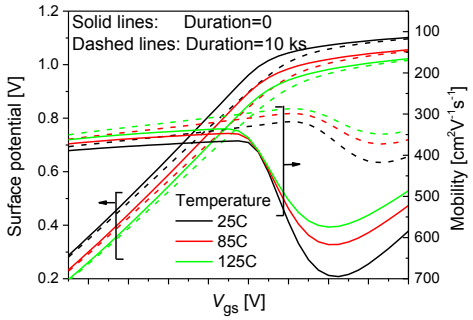


Fig. 6. Surface potential and mobility degradation for different temperatures and for non-aged and aged measurements of a bulk MOS device.

The temperature dependence of the measured drain current was investigated. Fig. 5a compares the Arrhenius plots of non-aged and aged measurements. Only results for the longest stress-duration time are depicted. Fig. 5b compares the extracted activation energies E_a as a function of V_{gs}, showing a reduction of E_a according to the V_{gs} increase. For comparison, the electrostatic surface potentials ϕ_s are depicted together. The drastic reduction of E_a in the subthreshold region is due to the temperature dependency of the carrier density, where the thermal voltage and the band-gap are the origins, since their values determine the charge densities within the Poisson equation, resulting in the temperature dependence of ϕ_s. Above the threshold voltage, E_a decreases smoothly to zero, referring negligible temperature dependence. The reason is that the potential starts to saturate, resulting also in a weaker temperature dependence. On the contrary the phonon scattering of carriers increases, which cause a mobility reduction as shown in Fig. 6. The comparison of activation energies with/without aging in Fig. 5b verifies that E_a is nearly independent of device aging, even though the surface potential characteristic is degraded by aging. Therefore, it can be concluded that the device features observed from the non-aged measurements are preserved in spite of the N_{trap} increase. This result coincides with that obtained by investigating the compact model HiSIM, namely the reduction of the temperature dependence to that induced by the thermal voltage and the band-gap.

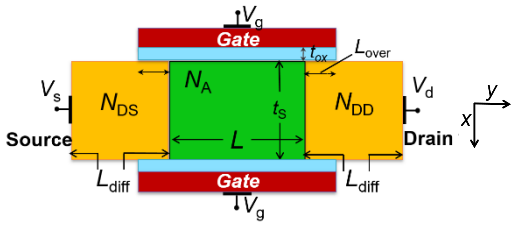
IV. Discussion

To confirm the proposed model for temperature dependence of the trap density, 2D-device simulation is investigated for a DG-MOSFET [7]. The studied structure is depicted in Fig. 7. The simulation includes the mobility degradation, the velocity saturation as well as the interface trap density [6]. The DoS distribution within the band-gap is ignored and treated as homogeneous (see Fig. 8) as can be observed in Fig. 4 after aging. The value of the interface state density D_{it} is varied to imitate the different stress conditions. As the compact model for the investigation HiSIM_MG is applied, where the only difference from HiSIM for bulk MOSFETs is that the Poisson equation has to consider the two gate controls. 2D-device simulation results of the I_{ds}-V_{gs} characteristics at low and high V_{ds} are depicted in Figs. 9a and b, respectively. Calculation results with HiSIM-MG are depicted together. These results confirm that the modeling of the trap density is still valid for such an advanced MOSFET generation, where the carriers are controlled by multiple fields within the device.

Fig. 10 shows the E_a characteristics as a function of V_{gs} for non-aged and aged cases with surface trap-densities of 5×10^{11} and 10^{12} cm^{-2}eV^{-1}, where D_{it} of 10^{11} cm^{-2}eV^{-1} is considered as the appropriate value for a fresh device. The same results as obtained for the measurements (see Fig. 5b) are obtained. This verifies again that the temperature-dependent trap density is correctly modeled only by the contributions from thermal energy and band-gap. Further, it confirms that the conventional temperature-dependent models are well applicable for aging investigations.

V. Conclusion

The temperature dependence of an aged device can be modeled simply with the temperature dependence of physical quantities as it is usually done. Even though the substrate current and stress-duration time are controlling the induced trap-density, the device characteristics after aging at higher temperature show only a very small temperature effect on the trap-density. The trap densities generated through stress at room temperature give enough accuracy in the calculation of the aged drain-current characteristics. Further the trap-density models for temperature dependence of unstressed devices are reliable for temperature-dependence simulations of the stressed devices. It is also observed that in bulk devices the temperature dependency of the N_{trap} increase is not detectable in the E_a characteristics. Therefore, device aging mainly originates from the aging of the electrostatic device parameters. The flexibility of the developed trap-density-based aging model has been corroborated by extending the model to multi-gate devices, such as double-gate MOSFETs.



$N_{DS}=10^{20}$ cm^{-3} $t_{ox}=1.5$ nm
$N_{DD}=10^{20}$ cm^{-3} $t_S=10$ nm
$N_A=10^{15}$ cm^{-3}

Fig. 7. Schematic of the studied double-gate MOS structure and the device parameters values.

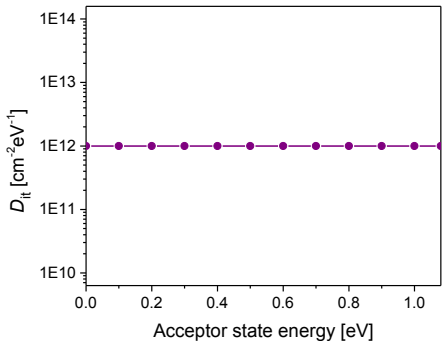


Fig. 8. Assumed homogeneous interface DoS distribution.

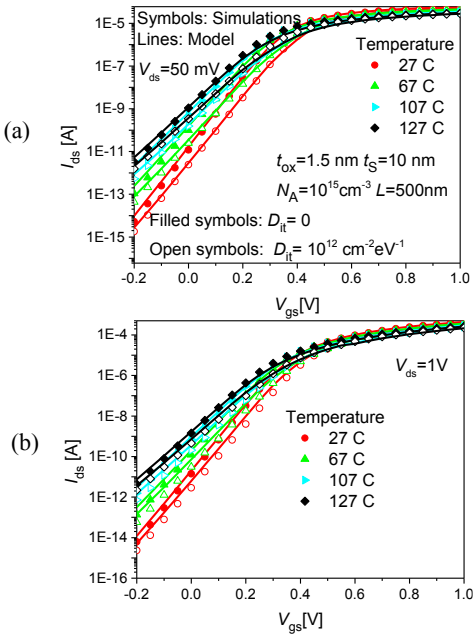


Fig. 9. Drain current characteristics for a DG-MOS considering the trap density distribution, $D_{tA}=10^{12}$cm^{-2}eV^{-1}, for different temperatures at (a) $V_{ds}=50$mV and (b) $V_{ds}=1$V.

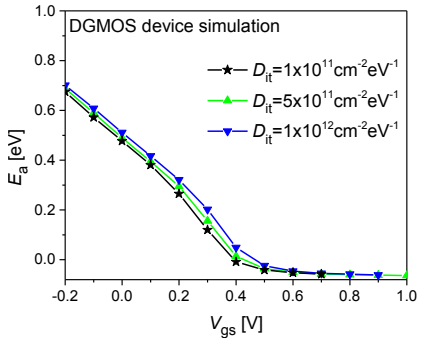


Fig. 10. Activation energy for different trap-density distributions as a function of V_{gs}.

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