From devices to circuits: modelling the performance of 5nm nanosheets

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***Abstract*—A simulation flow for design-technology co-optimisation using 5nm stacked nanowires is presented. The effect of variation in key process parameters on the behaviour of benchmark circuits is examined through the use of variability-aware compact models, accounting for both global and local variability.**

Keywords—DTCO, TCAD, variability, SPICE, compact models, circuits, nanowires

I. Introduction

Design-Technology Co-Optimisation (DTCO) has developed into a key methodology to reduce technology development costs and speed up time to market. Starting from technological specifications and customer requests, Technology Computer Aided Design (TCAD) is used to simulate the performance of transistors and interconnects. This is followed by compact model and resistor-capacitor (RC) extraction for SPICE simulation, and the assessment of key technology performance metrics [1].

Here we present a TCAD-to-SPICE simulation flow that demonstrates the evaluation of transistor performance using circuit-level metrics. The work presented here was done as part of the European research project SUPERAID7*.

II. TCAD Process and Device Simulation

The benchmark device used here is a 5nm stacked nanowire transistor. The fabrication of nanowire transistors has been demonstrated by CEA-Leti [2], and detailed information about their fabrication process was provided in the form of technical specifications as well as transmission electron micrographs (Fig. 1). Process simulation is used not only to generate the nominal dimensions, dopant and stress distribution of the transistor to be investigated, but also to predict the changes of these quantities in the case of systematic variations of the processes occurring. While Synopsys has a complete set of TCAD tools including lithography (Sentaurus Lithography) and topography (Sentaurus Topography), for the process flow simulation in the SUPERAID7 project Fraunhofer IISB used a combination of Sentaurus Process [3] and their in-house simulation tools ANETCH, BNDEDIT, DEP3D and Dr.LiTHO to produce the simulation structure shown in Fig. 2.

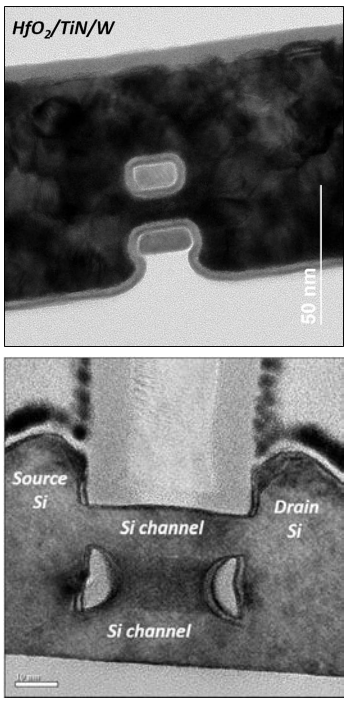

Fig. 1. Example of nanowire transistors fabricated by CEA-Leti and considered in this work: Cross-sectional TEM images of stacked nanowires (top), with SiN inner spacers (bottom).

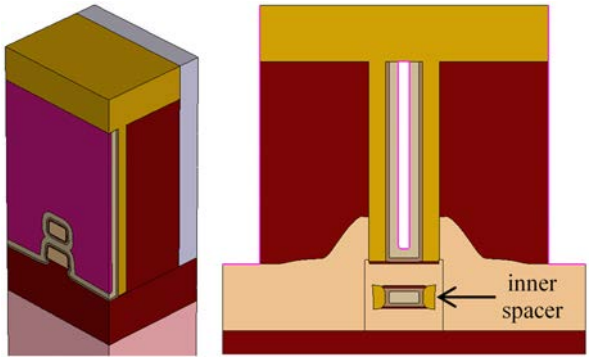

Fig. 2. Simulated nanowire transistor: (left) half of the structure cut across the nanowires, and (right) cross section along source-drain direction.

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Using simulations of transfer characteristics in Sentaurus Device [4], a sensitivity analysis of key process parameters was performed (Fig. 3) and three complementary parameters covering different processes (etching, deposition, and lithography) were chosen to form a design of experiment (DoE) matrix, where each parameter is varied by a +/- amount. The three process parameters chosen were the thickness of the deposited nitride layer (d_{SADP}) in the self-aligned double patterning process employed for the fin, the defocus of the gate lithography setup (F_{gate}) and the Germanium content of the sacrificial layer (x_{Ge}), which influences position and shape of the inner spacers. The nominal values and the size of variation applied to form the DoE are given in TABLE I. This is used to study the systematic global variability (GV) due to process variations.

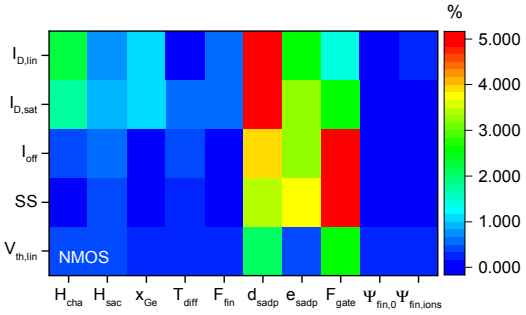

Fig. 3. Sensitivity of electrical FET properties (left axis) to variations in process parameters (bottom axis).

TABLE I. PROCESS PARAMETERS CHOSEN TO FORM THE DOE, NOMINAL VALUES AND THE MAGNITUDE OF THE VARIATIONS USED.

Process Parameter	Symbol	Nominal	Variation
SiGe mole fraction	x_{Ge}	0.3	± 0.03
Gate litho defocus	F_{gate}	0.0	± 0.04 µm
Fin SADP deposition factor	d_{sadp}	1.0	± 0.1

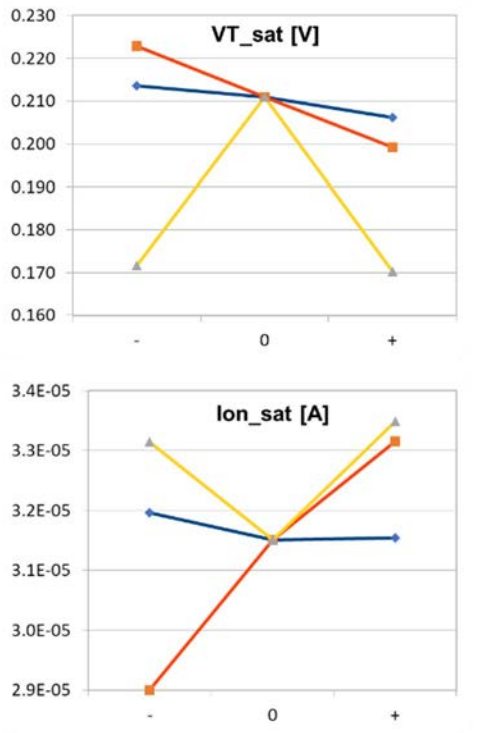

Fig. 4. Variation of key figures of merit with the -ve, nominal and +ve variation of each process parameter for the nMOS nanowire. Key: blue - x_{Ge}; orange - d_{SADP}; yellow - F_{gate}.

To capture the effects of the process variations across the DoE, Sentaurus Device simulations of the required I_D-V_D and I_D-V_G characteristics are run at each point in the DoE, which will be sufficient for the extraction of process-variability-aware compact models. Fig. 4 presents an analysis of the effects of varying each individual process parameter on key figures of merit (FoM). Each line has three data points with the centre point representing the nominal parameter value, while the left and right points respectively represent the negative (-ve) and positive (+ve) variation. Of note here is the non-monotonic response to variation in F_{gate}, which will need to be captured in the process-variability-aware compact model. F_{gate} has a large effect on Vt_{sat} and also impacts Ion_{sat}. The largest variation in Ion_{sat} comes from d_{SADP}.

To capture the statistical variability effects, the dedicated local variability (LV) simulator Garand VE [5] is used. For the 5nm technology being considered here, it is expected that metal gate granularity will no longer be a significant source of LV, as gate-last processing will lead to a mostly amorphous gate metal. Therefore, the sources of LV considered here are random discrete dopants (RDD) and line edge roughness (LER) in the gate edge. The dominant source of LV in these devices will be RDD and an example of RDD within the benchmark nanowire structure is shown in Fig. 5, with resultant I_D-V_G characteristics for the nominal DoE point shown in Fig. 6, for an ensemble of 500 devices.

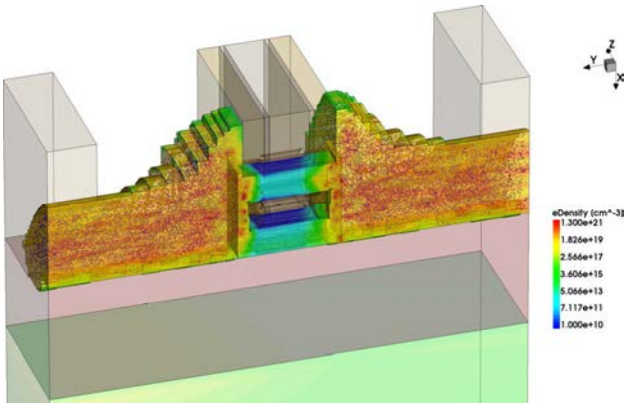

Fig. 5. Benchmark nanosheet device simulated in Synopsys Garand with random discrete dopants.

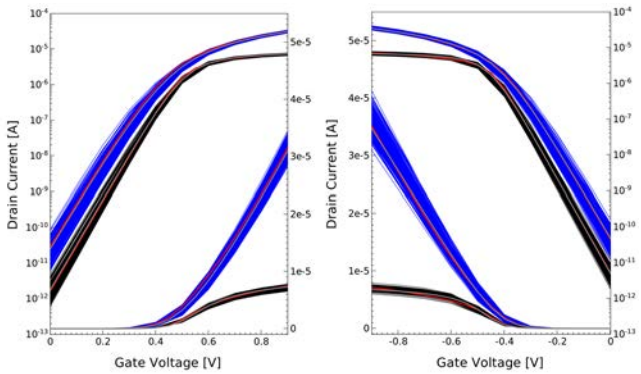

Fig. 6. I_D-V_G characteristics for the nMOS and pMOS devices at the nominal point in the DoE, with a statistical ensemble of 500 devices. Black: V_D=0.05V and blue: V_D=0.9V.

III. SPICE Model Extraction

The L-NSP model [6] is a surface-potential-based model dedicated to advanced 3D CMOS device architectures. The model was developed with special emphasis on supporting vertically stacked nanowire/nanosheet Gate-All-Around (GAA) CMOS technologies, and fits naturally with the stacked nanowire architecture that is investigated here.

L-NSP is constructed in a hierarchical way with two levels of parameter sets: a global-mode parameter set, and a local-mode parameter set. In the Synopsys TCAD-to-SPICE flow [7], instead of using the global mode to describe devices with different geometries, the Response Surface Model (RSM) approach is applied. RSM can not only capture the device geometry-dependent effects, but also the impact of non-geometry parameters, such as implantation energy, annealing condition, lithography defocus, etc., on device electrical characteristics. To use the RSM approach, only the local mode is required for SPICE modelling of individual devices.

The SPICE compact model extraction is divided into three stages: nominal device extraction stage (provides the base SPICE model for the target device at the nominal process design point), the response surface model extraction stage (provides SPICE models that cover device global process variation in the DoE space), and, finally, the statistical model extraction stage (provides SPICE models that cover device local statistical variability across the DoE).

To reduce the large number of statistical device simulations required, the LV simulations and statistical compact model extraction were not done at every DoE point. The benefit of the compact model approach adopted here is that the distributions and correlations of figures of merit due to LV are maintained across the DoE, even at points for which they were not extracted. This is demonstrated in Fig. 7, which compares the correlations of key FoM generated by TCAD simulations (black) and coming from the compact model interpolated by the RSM (red) at a point in the DoE at which the TCAD local variability simulations were not included in the RSM.

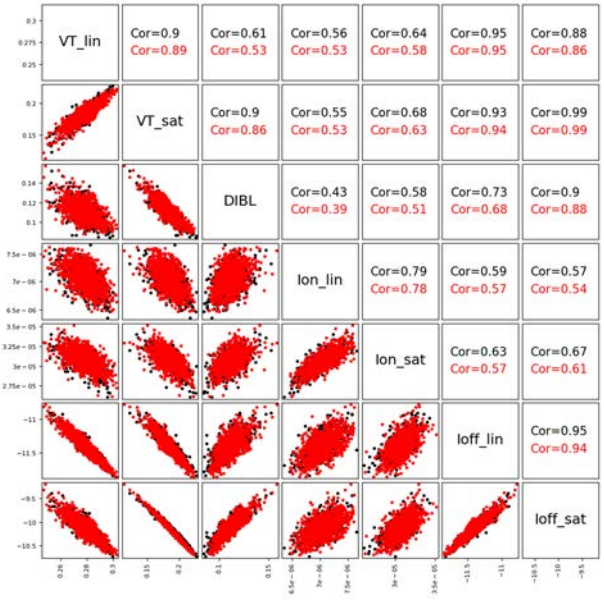

Fig. 7. Statistical compact model fitting results for nMOS nanowire devices (Black: TCAD results; red: compact model results) at x_{Ge}=0.3, d_{SADP} =0.9 and F_{gate} = -0.04 µm.

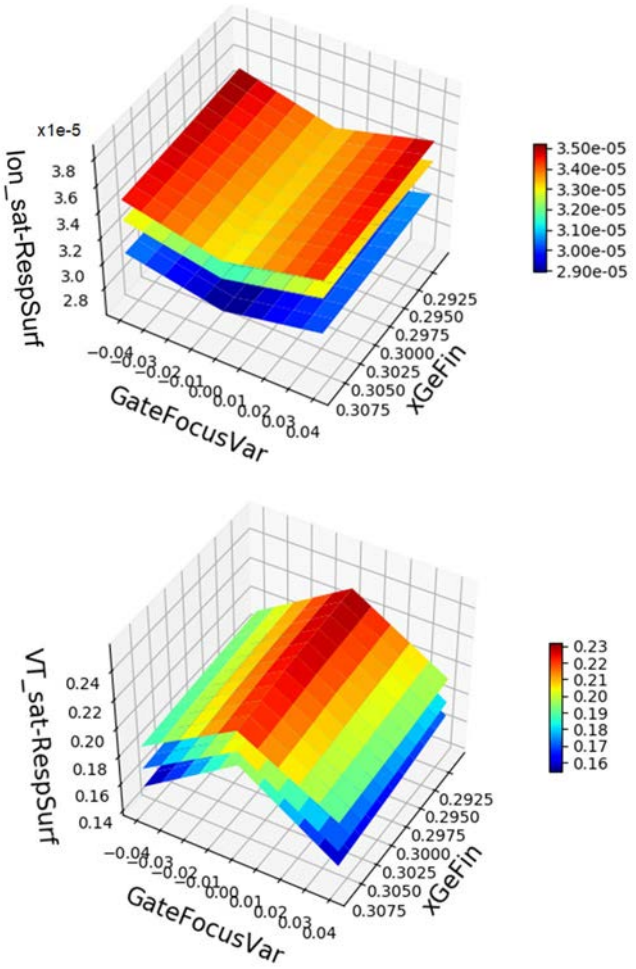

Fig. 8. Response surface compact model, regenerated by RandomSpice, covering DoE of nMOS nanowire devices. Different surfaces correspond to the three different DoE values of d_{sadp}.

An unlimited number of compact models can be generated for any point in the DoE following the extracted response surface (Fig. 8), allowing large-scale statistical circuit simulations. Note that the observed non-monotonic dependence on F_{gate} is captured in the compact model.

When generating random instances of devices within the DoE we will assume a Gaussian variation of the three process parameters about the nominal value. In the case of F_{gate}, the "V"-shaped response observed in Fig. 4, when applied to a Gaussian distribution, will lead to distinctly skewed FoM. The highest Vt_{sat} occurs at the nominal gate focus factor (peak of the Gaussian distribution), therefore there will be a large number of devices with close-to-maximum Vt_{sat}. At the same time, the minimum Vt_{sat} occurs at both +ve and -ve tails of the distribution in gate focus factor and therefore has significantly lower probability of occurring. Conversely, the Ion_{sat} distribution will be oppositely skewed.

IV. Circuit Simulation

The circuit used as a demonstrator is an AND-OR-Inverter (AOI), with a realistic 5nm backend structure produced in Process Explorer [8] (Fig. 9), based on an AOI221 standard cell layout in GDSII format. Once a 3D structure has been generated using process emulation, this can be used to extract a netlist of the RC equivalent parasitic elements for the BEOL, which in combination with front-end compact models can be used to construct a complete SPICE netlist for circuit

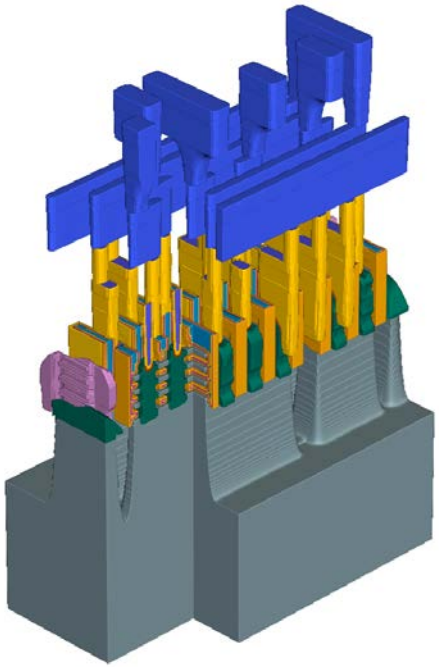

Fig. 9. 3D emulated process structure of an AOI221 standard cell for the 5nm technological node.

simulation of the AOI standard cell. The equivalent RC netlist for the interconnects is extracted using Raphael [9].

We have performed large-scale Monte Carlo circuit simulation to investigate the effects of GV and LV on delay times for different state transitions. For example, in Fig. 10 we see that transition *b2f_2_xr* (delay from input *b2* falling to output *x* rising) is usually the critical delay path, but due to a combination of global and local variability it is possible to have a circuit in which *a1f_2_xr* becomes the longer delay. As a result, it is critical to consider the combined impact of GV and LV when developing cell characterisation flows which feed into place and route, and static timing analysis (STA) for advanced technologies.

We have also studied the performance of ring oscillators (ROs) by wiring the AOI to mimic digital logic delay chains. The leakage and frequency variations are dominated by GV, and we can isolate the effects of the individual process parameters (Fig. 11). As shown, d_{SADP} variation mainly impacts the RO frequency, while the variation of F_{gate} mainly impacts on the RO leakage. x_{Ge} variation has a small impact on RO performance, however, it contributes to the decorrelation between frequency and leakage.

V. Conclusions

We have presented a fully integrated process-to-circuit simulation flow. This can be used to identify the relative impact of both global and local variations, and can help to direct process improvement efforts to the aspects of variation where the biggest gains in circuit performance can be achieved, thus closing the feedback loop on design-technology co-optimisation.

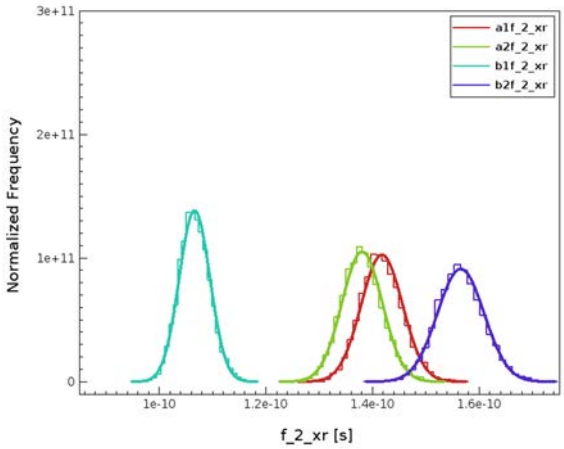

Fig. 10. Signal timing histograms with fitted Gaussian distributions for AOI propagation delays in the presence of combined GV and LV.

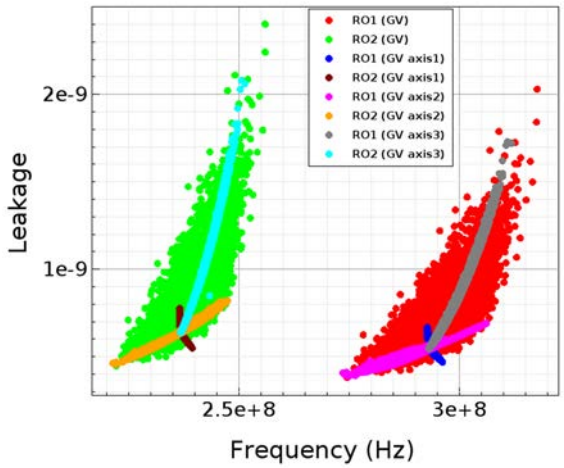

Fig. 11. Variations introduced by different process parameters for the leakage of two extreme case ROs (axis1: x_{Ge}; axis2: d_{sadp}; axis3: F_{gate}).

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