Single Event Transient Compact Model for FDSOI MOSFETs Taking Bipolar Amplification and Circuit Level Arbitrary Generation Into Account

Neil Rostand
DPHY
ONERA
Toulouse, France
neil.rostand@onera.fr

Sébastien Martinie
DCOS
CEA-LETI
Grenoble, France
sebastien.martinie@cea.fr

Joris Lacord
DCOS
CEA-LETI
Grenoble, France
joris.lacord@cea.fr

Olivier Rozeau
DCOS
CEA-LETI
Grenoble, France
olivier.rozeau@cea.fr

Thierry Poiroux
DCOS
CEA-LETI
Grenoble, France
thierry.poiroux@cea.fr

Guillaume Hubert
DPHY
ONERA
Toulouse, France
guillaume.hubert@onera.fr

***Abstract*— Single Event Transients (SET) are ionizing particles induced current pulses which are able to generate soft errors in CMOS circuits. In Silicon-on-Insulator (SOI) technologies, bipolar amplification phenomena is more significant due to presence of the Burried Oxide (BOX), which is detrimental to soft errors sensitivity. State of the art FDSOI SET models account for bipolar amplification through a dynamic pre-factor. This approach is mainly empirical and not compact. In this work, we propose a SET compact model for FDSOI MOSFETs including a physical modeling of bipolar amplification. Results are validated through TCAD simulations. A circuit level approach is proposed considering arbitrary generation within functional SRAM cell. This approach allows more realistic Single Event Upset (SEU) prediction and we show how circuit level generation can influence SEU prediction.**

***Keywords*— SET, Bipolar Amplification, SOI MOSFET, Compact Model, SPICE, TCAD.**

I. INTRODUCTION

Soft errors in circuits are generally due to parasitic current induced by ionizing particles within MOSFETs, called Single Event Transients (SETs) [1]. In recent technologies based on SOI technology, bipolar amplification phenomena is more significant due the presence of the BOX and increase circuit sensitivity to single events [2-7]. It consists in parasitic source – drain current induced by storage of generated holes (in NMOS) or electrons (in PMOS) in the Silicon film. Another issue is the morphology of the particle induced charge deposit at the circuit level which matters for high level of integration as its spatial extension can overlap with many transistors volumes. Both circuit level charge deposit and bipolar amplification have to be taken into account in SET models in order to perform reliable soft errors risk assessment.

In the literature, the approach to model bipolar amplification in SOI technologies relies on consideration of equivalent access resistance to determine triggering of bipolar amplification. Classical SET current model (i.e without bipolar amplification; called 1st discharge in [2]) is then multiplied by an empirical pre-factor [8]. This approach is not suitable for compact modeling (or SPICE modeling) point of view [9].

In this paper, we propose a compact model of SET taking both bipolar amplification and circuit level arbitrary charge deposit into account suitable for Fully Depleted SOI (FDSOI) structures (exposed for NMOSFETs). In Section. II, we evidence bipolar amplification through TCAD simulations of FDSOI MOSFET. In Section. III, we develop our bipolar amplification model and the Verilog-A implementation method. In Section. IV, we show the resulting SET compact model considering, 1st discharge, bipolar amplification, and circuit level arbitrary charge deposit. The relevance of accounting for circuit level charge deposit is highlighted through SPICE simulations of Single Event Upsets (SEUs).

II. EVIDENCE OF BIPOLAR AMPLIFICATION

In this section, bipolar amplification is evidenced performing transient TCAD simulations [10] of a 2D FDSOI NMOSFET ($L_{ch} = 0.1\mu m$, $T_{si} = 10nm$, $V_{ds} = 1$, $V_{gs} = 0V$) with heavy ion strike considering simulation setup explained in [1]. After particle strikes the transistor, generated holes remain in the body (due to SOI structure) as illustrated in Fig. 1.a. This involves barrier lowering (see Fig.1.b) which allows electrons to flow from source to drain if $V_{ds}>0$, this extra current is the bipolar amplification. As illustrated in Fig. 1.c, after prompt 1st discharges, we see these pulses exhibit relaxation tails which decay very slowly involving an higher collected charge at the drain $Q(t) = \int I_d dt$ than deposited charge Q_{dep} which is the main feature of bipolar amplification. Fig 1.d illustrates the hole and electron quantity in the body (respectively denoted P and N) for different LET versus time, and highlights that holes are stored inside the body after a short time interval corresponding to quick decay of P (for high Linear Energy Transfer LET). We can actually show that this decay is due to quick recombination in source area. We also see electrons are injected in the body (still N remains lower than P) in order to contribute to bipolar amplification current.

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III. MODELIING OF BIPOLAR AMPLIFICATION

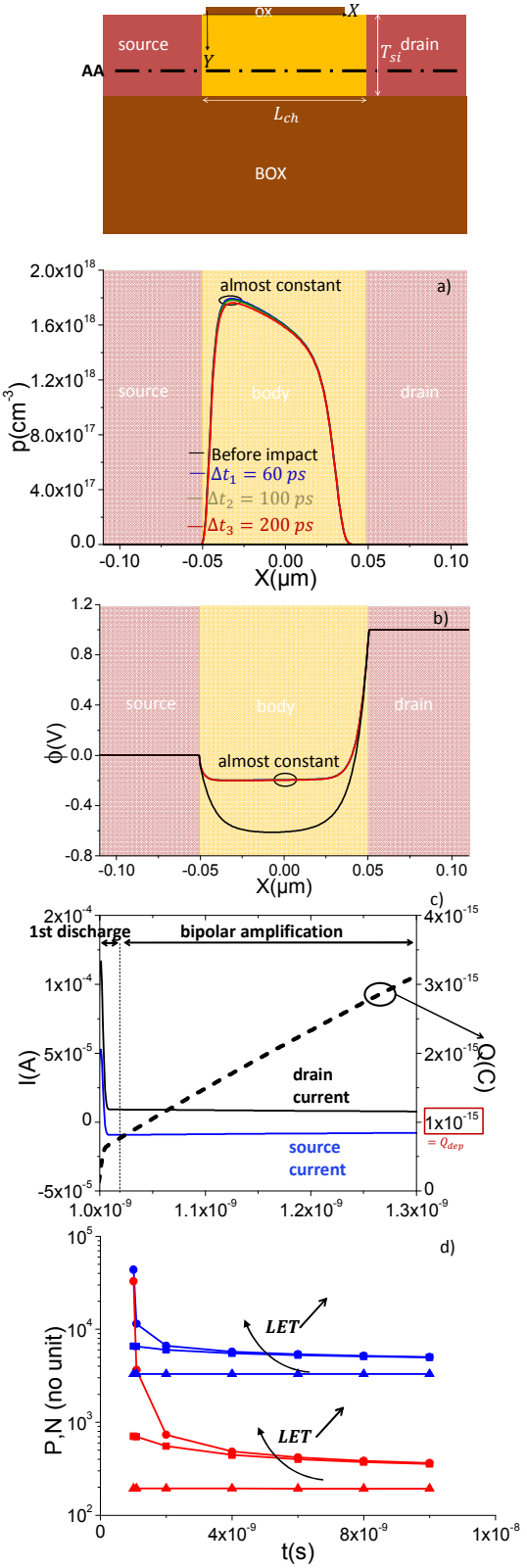

Fig. 1: TCAD evidence of bipolar amplification for *LET=0.1 pC/µm* . a,b): plots of hole density p and of the electrical potential ϕ in AA cutline for different times after particle impact *Δt*. c): SET pulses at drain (black full line) and source (blue full line) electrodes and collected charge at the drain electrode (black dash line). d): quantity of holes (blue) and of electrons (red) relative to time after particle impact in the body. Circle, square, and triangle symbols correspond respectively to *LET={1,0.1,0.05 } pC/µm.*

A. Explicit bipolar amplification current expression

In this part, we consider the particle generated $P_{dep} = LET.T_{si}/q$ electron/hole pairs in the body during impact at time t_i. We assume electron current density $\boldsymbol{J_n}$ is conservative within the body, as evidenced by TCAD ($\boldsymbol{\nabla.J_n} \approx 0$). In a 1D problem along X, it means $\boldsymbol{J_n}$ is uniform. Integrating $\boldsymbol{J_n}$ in drift-diffusion formalism along $\boldsymbol{X}$, we obtained:

$$j_n = -q.\frac{\mu_n}{L_{ch}}.\int_0^{L_{ch}} n.\frac{\partial \phi_n}{\partial x}.dx \qquad (1)$$

In (1), ϕ_n is the electron quasi-Fermi potential, μ_n the electron mobility in the body and n the electron density. To capture V_{ds} dependence, we consider simplified case of linear ϕ_n often called "long channel approximation". We can then derive (2), corresponding to source to drain bipolar amplification current:

$$I_{ba}(t) = \frac{-q.\mu_n}{L_{ch}^2}.N(t).V_{ds} \qquad (2)$$

At this point we introduce the electroneutrality factor defined by $X(t) = N(t)/P(t)$. As the relation between time and P is a bijection, we can redefine X so that it is $P(t)$ dependant. Then:

$$I_{ba}(P(t)) = \frac{-q.\mu_n}{L_{ch}^2}.\mathrm{X}\big(P(t)\big).P(t).V_{ds} \qquad (3)$$

An empirical function is chosen for the electroneutrality factor $\mathrm{X}\big(P(t)\big)$ (which is actually *LET* dependant). We now need to determine $P(t)$.

B. Non-linear differential equation for $P(t)$

Fig.2 shows the hole quasi-Fermi potential ϕ_p in X direction for different times after particle impact. We clearly see that ϕ_p is almost uniform in the body. Writing $d\phi_p/dx = 0$ in the body, we obtain the 1st order partial differential equation:

$$\frac{\partial \Delta p}{\partial X} = -\frac{\partial \phi}{\partial X}.\frac{1}{V_t}.\Delta p \qquad (4)$$

In (4), Δp is the excess hole density (generated by the particle), ϕ the electrical potential, and V_t the thermic voltage. Considering Δp property $\int_0^{L_{ch}} \Delta p.dX.W.T_{si} = P(t)$ (W being the body width), the solution of this equation can be written as follow:

$$\Delta p(X,t) = \frac{P(t)}{W.T_{si}.I_\phi(t)}.e^{\frac{\phi(X,t)}{V_t}} \qquad (5)$$

Where $I_\phi(t) = \int_0^{L_{ch}} e^{-\frac{\phi(X,t)}{V_t}}.dX$. The next step is to express the hole conservation law in the body, considering zero hole current at the source – body and body – drain junctions. However, surface recombination currents at these jonctions have to be taken into account because of high doping in source/drain areas. Note that no volume recombination occurs in the body for this time scale due to very low doping level $N_a = 10^{15} cm^{-3}$. Denoting V_{rec} for the recombination speed at the PN junctions, the resulting conservation law can be written as follow:

$$\frac{dP}{dt} = -\frac{1}{\mathrm{T}(P)}.P \qquad (6.a)$$

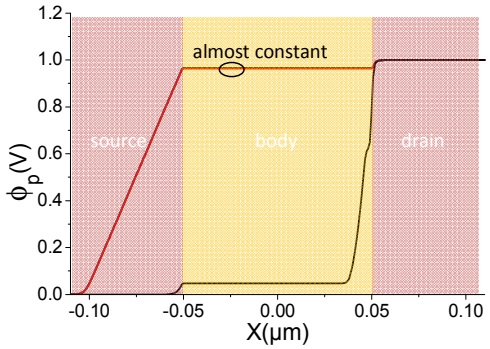

Fig. 2: plot of hole quasi Fermi potential ϕ_p in AA cutline for different times after particle impact Δt.

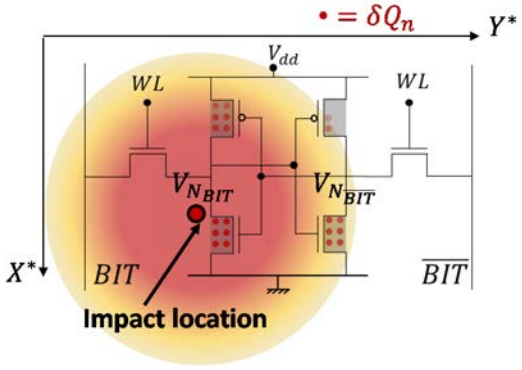

Fig. 3: 6T-SRAM cell submitted to particle strike. Illustration of discretization of circuit level charge deposit morphology induced by the particle in vertical incidence (orthogonal to the SRAM cell plane).

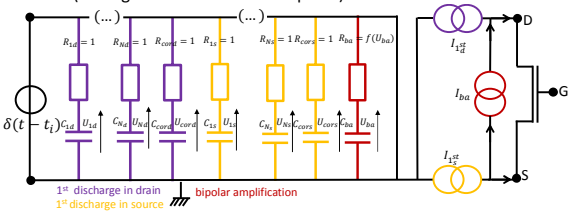

Fig. 4: equivalent electrical circuit of SET model in case of FDSOI. Modified RC circuit related to bipolar amplification completes initial 1st discharge RC circuits, see [1,9].

$$\mathrm{T}(P) = \frac{I_\phi(P)}{V_{rec}\left(e^{-\frac{V_s}{Vt}} + e^{-\frac{V_d}{Vt}}\right)} \qquad (6.b)$$

As the time constant (6.b) is not analytical, we prefer extract a simpler expression from TCAD, plotting the quantity $-P^{-1}.dP/dt = \tau(P)^{-1}$. We obtain the following function:

$$T_{ex}(P) = \tau_r.\left(1 + \left(\frac{P_c}{P}\right)^{\gamma}\right), \forall P > 0, \gamma > 0, P_c > 0 \qquad (7)$$

In (7), τ_r is the recombination time in source/drain while γ and P_c are parameters depending on geometry parameters (in particular L_{ch}, T_{si} and W) but this dependence has not been modeled. The set of implicit equations represented by (6.a) and (7) can be solved by the SPICE simulator, assigning P/P_{dep} to the voltage drop U_{ba} of a capacitance being part of a modified RC circuit, where R value depends on U_{ba}, this circuit being submitted to 1V voltage pulse at impact time of the particle. This equivalent circuit is implemented in Verilog-A.

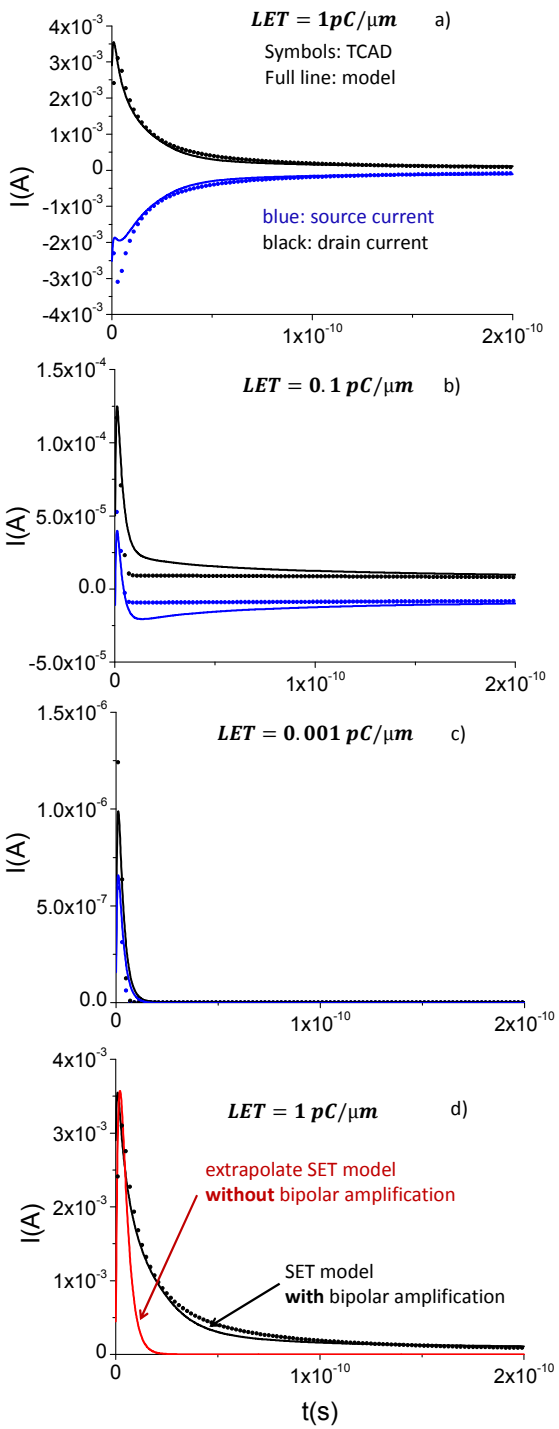

Fig. 5: a-c): comparison between TCAD and proposed SET model at source and drain electrodes for different LET values. Such a good agreement is obtained setting model parameters to consistent values: $D = 2.7.10^{-4} m^2.s^{-1}, v_X = 4000\ m.s^{-1}, D_n = 2.25.10^{-4}\ m^2.s^{-1}, P_c = 3.10^3 C, \gamma = 3$. d): comparison between SET model with and without bipolar amplification and TCAD pulse at drain electrode after adjustment of model parameters for $LET = 1\ pC/\mu m$: we cannot describe the tail of the pulse.

IV. SET COMPACT MODEL FOR CIRCUIT LEVEL ARBITRARY CHARGE DEPOSIT: SEU PREDICTION IN SRAMS CELLS

As bipolar amplification occurs after 1st discharge, we can assume that 1st discharge and bipolar amplification are independent. For 1st discharge modeling, we improved

former work [1,9] assuming the particle induced many punctual charge deposits δQ_i at different locations of the circuit (made of many transistors) with coordinate X_i^* along X^*, see Fig.3. We also consider uniform drift velocity v_X in source – drain direction in the body of each transistor. For one given transistor of the circuit, the resulting 1st discharge model at the drain for example is then:

$$I_{1^{st}}(t) = \sum_{k=1}^{\infty} G_k . e^{-\frac{t-t_i}{\tau_k}} . H(t-t_i) \quad (8.a)$$

$$G_k = -q . D_n . T_{si} . W . \frac{\partial A_k}{\partial X}(L_{ch}) \quad (8.b)$$

$$A_k = \frac{2.\left(\sum_{i\in body} \delta Q_i . \sin\left(\frac{k.\pi}{L_{ch}} . X_i\right) . e^{\frac{v_X (X-X_i)}{2.D}}\right) . \sin\left(\frac{k.\pi}{L_{ch}} . X\right)}{W . T_{si} . L_{ch} . q} \quad (8.c)$$

$$\tau_k = \left(\frac{\pi^2 . k^2 . D}{L_{ch}^2} + \frac{v_X^2}{4.D}\right)^{-1} \quad (8.d)$$

In (8.a-d), H is the Heaviside function, D_n the electron diffusivity in the body, $X_i = X_i^* - X_s^*$ (X_s^* being the source – body junction along X^*), $X = X^* - X_s^*$, and D is the ambipolar diffusivity.

Resulting SET model at the drain of one given transistor is then the sum of $I_{1^{st}}$ and I_{ba}. Similar model can be obtained for the source SET current. The corresponding equivalent electrical circuit is shown in Fig. 4. Note that at circuit level, the number of deposited holes in the body are expressed as $P_{dep} = \sum_{i\in body} \delta Q_i / q$. SET Model has been validated through extraction of source and drain TCAD pulses for one generation point in the middle of the channel. We obtain good agreement between TCAD and model, after realistic calibration of 1st discharge parameters D, D_n, v_X and bipolar amplification parameters τ_r, P_c, γ, as shown in Fig.5.a-c. Fig.5.d evidences the relevance of the bipolar amplification modeling work, comparing model with and without bipolar amplification.

We then apply the proposed SET model to SEU prediction performing transient SPICE simulations of standard 14nm FDSOI SRAM [11]. In Fig.6.a, we consider 2 different cases of charge deposit at $t = 0$: case 1 corresponds to deposit localized in non-sensitive PMOS for the considered initial bit state and case 2 to more realistic charge sharing with sensitive NMOS latch. We see that circuit level generation can influence SEU prediction as shown in Fig.6.b as a slight charge generation in sensitive NMOS latch can overcome large generation in non-sensitive PMOS (the latter actually reinforcing the initial state) and trigger the bit state flipping.

V. CONCLUSION

In this paper, we proposed a compact model of SET taking bipolar amplification and circuit level arbitrary charge deposit into account. Such a model is dedicated to FDSOI structures (FDSOI MOSFET, FinFET …) and is suitable for performing realistic soft error risk assessment. TCAD simulations supported model development. More extensive work will be dedicated to improve predictability of the model focusing on electroneutrality function and description of the triggering of bipolar amplification around impact time.

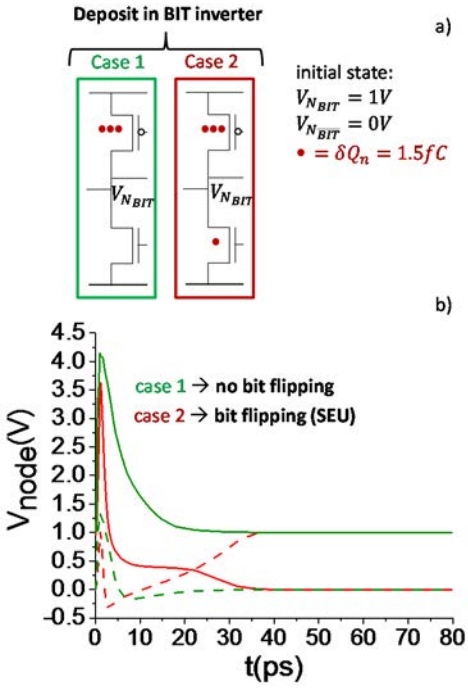

Fig. 6:a): illustration of 2 different cases of particle induced charge deposit at initial time within the BIT inverter b): dynamics of V_{BIT} and $V_{\overline{BIT}}$ after particle strike for these cases: SEU is able to occur even if most of the charge is deposited in non-sensitive PMOS because of some charge deposited in sensitive NMOS Latch.

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