Quantum Mechanical Simulations of the Impact of Surface Roughness on Nanowire TFET performance

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***Abstract*—In this work, the impact of the surface roughness (SR) on the variability in p-type InAs nanowire Tunnel FET (TFET) has been investigated. Using the Non-Equilibrium Green's Function (NEGF) module implemented in the University of Glasgow quantum transport simulation tool, called NESS, we have simulated a statistical ensemble of 200 TFETs with unique SR profiles. The SR in each device is defined by the characteristic values of the SR root mean square amplitude (RMS) and correlation length. Our results show that the larger the RMS, the stronger the variability. We find that the SR-induced variability is reduced in InAs-Si heterostructure TFETs when comparing with their homogenous InAs counterpart. The impacts of both metal grain granularity and random discrete dopants on InAs TFETs are also studied. Our finding suggests that SR is the weakest source of statistical variability.**

Keywords—surface roughness (SR), variability, tunnel field-effect transistor, quantum simulation.

I. INTRODUCTION

With the continuous scaling of the MOSFETs, the power consumption has become a critical concern since the subthreshold swing (SS) in MOSFETs is limited to 60mV/decade at room temperature. Based on band-to-band tunneling (BTBT) the tunneling FET (TFET) is a promising candidate allowing to achieve SS<60mV/decade and thus offering reduction of leakage or supply voltage at constant drive current [1].

Although TFETs have been widely studied experimentally and through simulation in order to optimize performance [2]-[4], the variability induced by the surface roughness (SR) is still not very well investigated [5], [6]. Considering that the SR has a strong impact on MOSFETs performance [7], it is crucial to investigate its impact on TFETs. F. Conzatti *et al.* [5] reported simulation of statistical ensemble with 50 SR realizations in n-type TFET in comparison with MOSFETs. H. Carrillo-Nuñez *et al.* [6] studied the impact of SR in p-type TFET by carrying out atomistic simulations of only few devices. Therefore, there is a need of thorough investigation of the SR in TFETs on a proper statistical scale.

In this work, the variability induced by SR is investigated in ensembles 200 p-type InAs nanowire TFETs by using the quantum transport solver module in NESS [8]. The dependence of the variations on the values of the root mean square (RMS) amplitude has been studied. We also report that InAs-Si heterojunction not only can improve the current but also can alleviate the variability caused by SR. Physical insight into the influence of SR is also provided. Besides, a comparison between the variability induced by SR, random discrete dopants (RDD), and metal grain granularity (MGG) is given.

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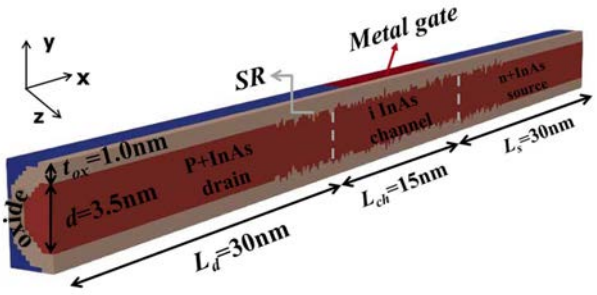

Fig. 1. 3D view of the p-type InAs nanowire TFET with SR. For all devices, the diameter of nanowire is d= 3.5nm, and the channel length is L_{ch} = 15nm. The SR is between the oxide and InAs semiconductor, covering the whole channel and 10nm source and drain regions. The left 20nm source/drain without SR is for better convergence. The source-drain voltage is fixed at $V_{ds} = -0.5$V.

II. SIMULATION METHODOLOGY

Fig. 1 shows the sketch of a p-type InAs nanowire TFET with SR. The nanowire diameter is $d = 3.5$nm, the gate length is $L_{ch} = 15$nm, and the oxide thickness is $t_{ox} = 1$nm with dielectric constant $\varepsilon_{\mathrm{ox}} = 9.0$. The doping level in the n^+-source and p^+-drain is $N_S = N_D = 5 \times 10^{19}\mathrm{cm}^{-3}$, and the channel is left intrinsic. The SR at the interface between InAs and gate oxide is introduced by means of an autocorrelation function $\mathrm{C}(x) = \Delta_m^2 \exp(-\sqrt{2}x/L_m)$, which is characterized by the RMS Δ_m and correlation length (CL) L_m parameters [9]. The SR region covers the whole channel and 10nm source and 10nm drain regions. The smooth part in source/drain region is required for numerical stability. The source-to-drain voltage is fixed at $V_{ds} = -0.5\mathrm{V}$, and all simulations are performed at room temperature ($\mathrm{T} = 300\mathrm{K}$).

The Flietner model [10], [11], combined with the non-equilibrium Green's function (NEGF) within an effective mass approximation, is used to calculate the BTBT current. The accuracy of this approach, implemented in NESS, has been validated by comparison with atomistic simulation results showing a very good agreement [11], [12]. The BTBT

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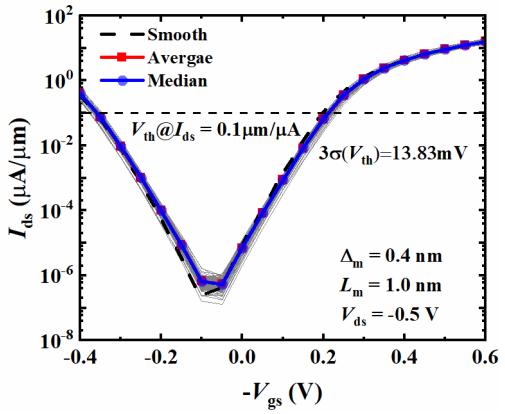

Fig. 2. $I_{ds} - V_{gs}$ characteristics of an ensemble of 200 p-type InAs nanowire TFETs with SR (gray curves). $\Delta_m = 0.40$nm, and $L_m = 1$nm. The threshold voltage is defined as the V_{gs} yielding $I_{ds} = 0.1$μA/μm, and the off-current is $I_{off} = 10$pA/μm at $V_{gs} = 0$V. The current is normalized by πd. The ambipolar current is also plotted.

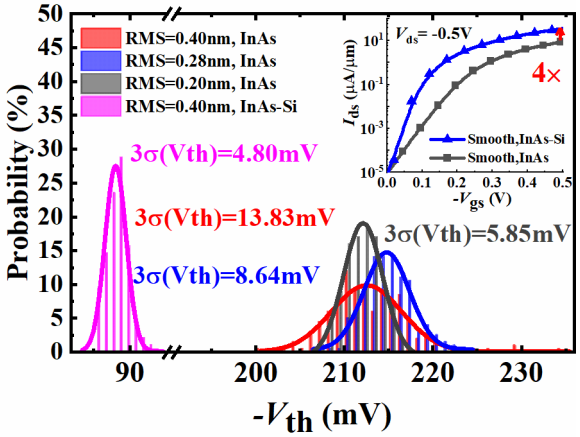

Fig. 3. The distribution of V_{th} with 0.20, 0.28 and 0.40nm RMS amplitude of SR variation of an ensemble of 200 InAs and InAs-Si TFETs. The inset shows the $I_{ds} - V_{gs}$ characteristic of the smooth InAs and InAs-Si TFETs. The off-current at $V_{gs} = 0$V is defined as 10pA/um. In InAs-Si TFET, Si (InAs) is used as the channel/drain (source) material. With the increase of RMS, the variability induced by SR increases. The InAs-Si heterostructure not only can improve the current but also can alleviate the variation caused by SR. $L_m = 1$nm in all devices.

model is detailly explained in [11]. The inclusion of the electron-phonon coupling would improve the accuracy of our results. However, it has been reported phonon scattering to only have a small influence on the OFF-state in TFETs [6]. The inclusion of phonon scattering is also very computational intense, particularly, when considering a large number of samples. The latter would not significantly change the conclusions of this study and thus phonon scattering is neglected in this work.

III. Results and Discussions

Fig. 2 shows the $I_{ds} - V_{gs}$ characteristics of an ensemble of 200 nanowire TFETs with random SR configurations determined by $\Delta_m = 0.40$nm and $L_m = 1$nm. The smooth, average, and median curves are also presented. The off-current of smooth case is $I_{off} = 10$pA/μm at $V_{gs} = 0$V, and the threshold voltage (V_{th}) is defined as the V_{gs} yielding $I_{ds} = 0.1$μA/μm. It can be seen that the ambipolar current can also be predicted by NESS. In this case, the standard deviation of threshold voltage is $3\sigma(V_{th}) = 13.83$mV. I_{off} of the ensemble ranges from 1.92×10^{-6}μA/μm to 1.25×10^{-5}μA/μm, and the on-current (I_{on}) defined at $V_{gs} = 0.5$V varies from 7.56μA/μm to 11.34μA/μm, indicating a smaller variability than I_{off}. The smaller variability in I_{on} than I_{off}, also found in MOSFETs [9], is attributed to the smaller SS in on-state.

In Fig. 3, the threshold voltage probability distribution (PD) is plotted for different values of RMS, i.e. 0.20, 0.28, and 0.40nm. It can be found that the variability increases with the increase of RMS, which is in agreement with [13]. The PD of the V_{th} in case of the InAs(source)-Si(channel) heterojunction nanowire TFET is also shown in Fig. 3. In the latter, the doping levels in the source and drain are 5×10^{19}cm^{-3} and 2×10^{20}cm^{-3}, respectively. The $3\sigma(V_{th})$ with $\Delta_m = 0.40$nm in the InAs-Si TFET is reduced by 17.95%, 44.44%, and 65.29% when comparing with that in InAs TFETs with $\Delta_m = 0.20$nm, 0.28nm, and 0.40nm. The inset in Fig. 3 compares the $I_{ds} - V_{gs}$ characteristics of the smooth InAs and InAs-Si TFETs under the same $I_{off} = 10$pA/μm. The InAs-Si TFET provides an on-current four times higher than the InAs TFET. Therefore, the heterojunction not only can improve the current but also can reduce the SR-induced variability. In order to gain a physical insight into our findings, the current spectra of both TFETs with the SR are shown in Fig. 4. The regions from left to right are drain, channel, and source regions, respectively. The red lines denote the highest valence and the lowest conduction subbands. Observe the fluctuations in the subbands due to the SR influence on the confinement. Fluctuations in the valence subband in the InAs TFET are more pronounced in comparison to InAs-Si

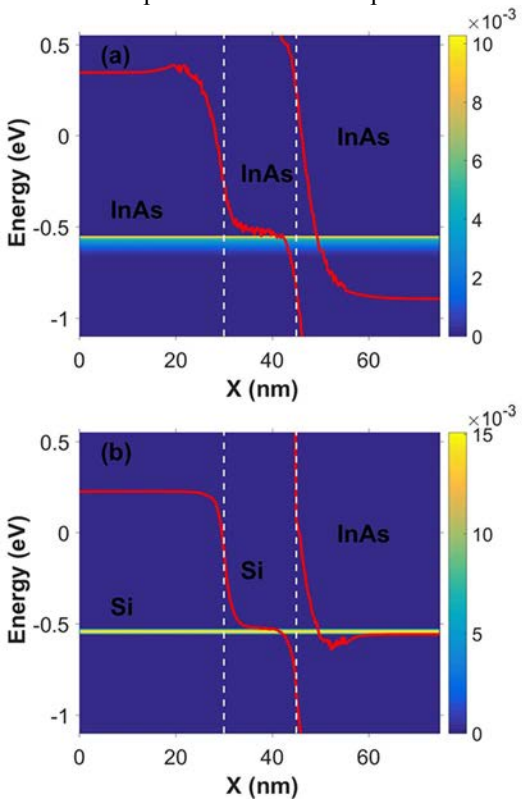

Fig. 4. The current spectra of the (a) InAs TFET and (b) InAs-Si TFET at the maximum V_{th} with 0.40nm RMS amplitude of SR variation. $L_m = 1$nm. The unit is μA/eV. The red lines denote the highest valence and the lowest conduction subbands. Due to the fluctuation in thickness from SR, the subbands are not smooth anymore which results to the variation of performance. Compared with the case in InAs-Si TFET, the fluctuation of the valence subband in InAs TFET is much stronger.

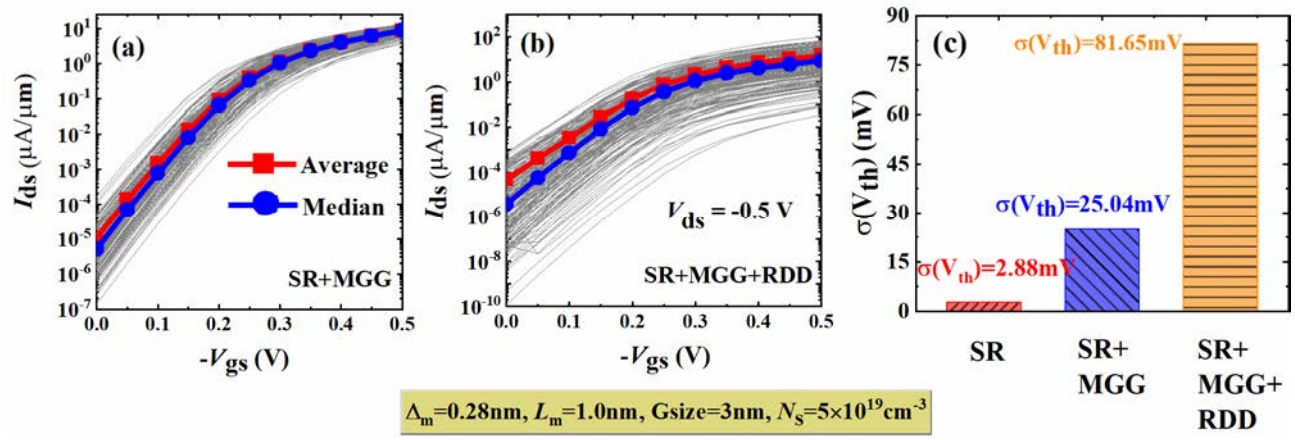

Fig. 5. The variability of V_{th} induced by SR compared to other major sources of variability (MGG and RDD) at $V_{ds} = -0.5$V of an ensemble of 200 InAs TFETs. MGG is generated from the realistic Voronoi pattern with average grain size (Gsize) of 3.0nm. RDD is considered in the source and drain regions, and covers 10nm length in each region as SR does. The number of dopants in RDD working regions obeys the Poisson distribution. For SR, $\Delta_m = 0.28$nm and $L_m = 1$nm. Compared with the influence from MGG and RDD, SR shows the least impact on the variability of the p-type InAs TFET.

transistors, resulting from the stronger quantum confinement effect in InAs channel due to its lighter hole effective mass than Si material. As a result, the SR-induced variability is more pronounced in InAs TFETs.

Except SR, there are still other source of variabilities, such as MGG, RDD, and trap-assisted tunneling (TAT). The latter strongly affects the subthreshold region by increasing the off-state BTBT current. TAT is not considered in this work since its impact is already well known [14]-[16]. We rather focus on the MGG- and RDD-induced variability. The MGG is generated by using the realistic Voronoi pattern [9], [17]. Here, we have considered a TiN metal gate which has two possible grain orientations (<200> and <111>) with a work function difference of 0.2 eV [18]. The occurrence probabilities of each orientation are 60% and 40%, respectively. The default average grain size of the metal gate is Gsize = 3nm. In case of RDD, the number of dopants in each of the TFETs is randomly chosen from a Poisson distribution, placing them by means of a probability rejection technique. The mean is determined by the doping concentration multiplied by the volume of the RDD region [9]. In InAs TFETs, the RDD regions cover 10 nm length in the source and drain, i.e. the same SR regions. For numerical purposes, uniform doping is adopted at the endings of source and drain regions to guarantee the numerical convergence.

Fig. 5 compares the impact of the different aforementioned variability sources, including SR, on the characteristics of TFETs. Compared with SR (Fig. 2), MGG has stronger influence on the $I_{ds} - V_{gs}$ characteristics, as observed in Fig. 5(a). When considering MGG, I_{off} ranges from 1.35×10^{-7}μA/μm to 1.64×10^{-4}μA/μm, larger than 3 orders of magnitude. I_{on} ranges from 3.84μA/μm to 13.54μA/μm, and its variation is still much weaker than I_{off} case. However, we find that RDD-induced variability is the dominant source of variability. This is shown in Fig. 5(b) where one can observe that the on-current now spreads over 4 orders of magnitude. The same effect is found for the off-current which spreads over 7 orders of magnitude. This strong impact is attributed to the position and number of the dopants that directly affect the electrical field across the tunnel junction [12], [19]. The impact on the V_{th} variation is summarized in Fig. 5(c). It is observed that the $\sigma(V_{th})$ in the overall combined case is nearly 30× larger than that in SR case.

IV. Conclusion

The impact of the SR on p-type InAs nanowire TFET is analyzed through quantum transport simulations of ensembles of 200 samples. The statistical analysis shows that the increase of RMS enhances the SR induced variability. Heterojunction TFETs, such as InAs-Si TFETs, not only can improve the performance of TFET but also could effectively reduce the influence of SR, due to the heavier hole effective mass in the Si channel and thus the weaker quantum confinement effect. It was also found that SR is the weakest source of variability in TFETs when compared to other variability sources such as MGG and RDD. Whereas, the RDD-induced variability is found to be the strongest.

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