# Optimization of select gate transistor in advanced 3D NAND memory cell

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*Abstract*—**There are several device challenges unique to the select gate transistor in 3D NAND memory cell. It requires low leakage current to prevent read and program disturb problem and it needs to provide enough current during read and erase operation. In this paper, we examined the design optimization of select gate transistor with respect to various device elements including work-function, S/D overlap, and trap density. Finally, we reviewed the path to reduce the channel length of the select gate transistor in conjunction with the role of dummy cells.**

*Keywords—3D NAND memory, program/erase operation, program disturb, self-boosting effect*

## I. Introduction

Demand for aggressive bit density scaling of 3D NAND memory device is driving more cells per string as well as more string per block. These multi layers of materials such as oxide and polysilicon introduce manufacturing complexity in various NAND process steps including memory hole, stair step, and slit etch process. It is desirable, therefore, to reduce the layer thickness while increasing the number of memory cells per string. In addition, the number of dummy cells and gate length of select gate device at the end of memory string play a big role on overall stack thickness. In this paper we studied the role of select gate and dummy cells on memory operation including program disturb and cell operation speed.

## II. Process Simulation

In this paper, BICS type 3D NAND memory device [1] was examined. The process flow of memory array was simulated as shown in Fig. 1. In this task, special 3D process simulation was used in order to accommodate challenges unique to 3D NAND process flow simulation; process simulation must encompass memory array, interface region and peripheral circuits. As the number of stacks is increased, cell array to circuit interface structure become larger and more complex. From the 3D simulator perspective of view this is a daunting task: simulator need to use fine grid space for memory array simulation e.g. nm resolution, yet it needs to cover 10x10um area. Usually, simulating such a large area with fine resolution hamper the overall performance. In order to overcome this problem, we used Cell-mode 3D simulation. It is a geometry tetrahedral based mesh structure with polygonal algorithm for etch and deposition process. This mode automatically adjust the grid space without presetting of the resolution. Fig. 2 shows the close-up image of memory cell constructed by conventional and Cell-mode. It is apparent that the core cell structure simulated by Cell-mode show superior quality. It is noted that the Cell-mode is capable of performing conventional 3-D process simulations such as implantation and diffusion.

Note that the NAND cell is comprised of polysilicon core with P+ doped poly-Si gate material. The bottom of the memory cell is connected to NWell through Bottom Select Gate (BSG) and top of the memory cell is connected to Bit-line through Top Select Gate (TSG) device.
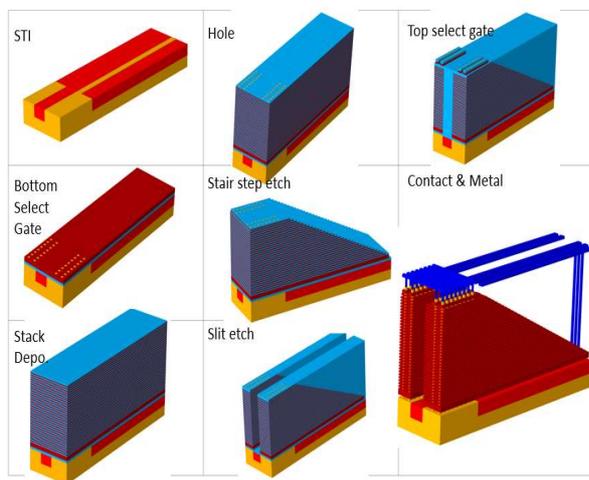


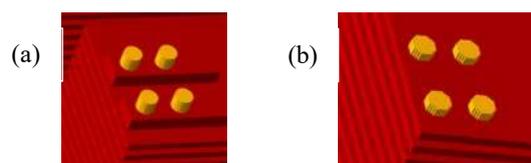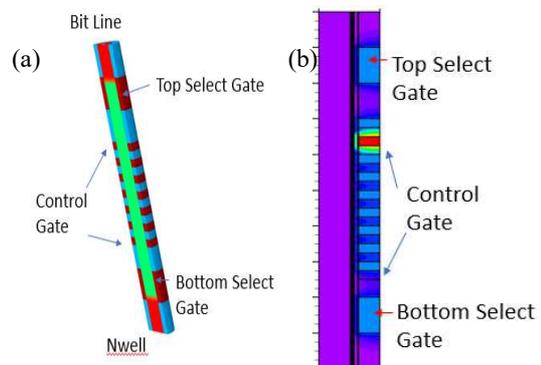Fig. 1. Process flow of BICS type 3D NAND memory.



Fig. 2. Close-up image of memory cell region simulated by two different mode in 3D process simulation. (a) Cell-Mode, (b) Process-Mode with 5nm resolution.



Fig. 3. Structure used in device simulation (a) 3D image (b) 2D cut image of potential after programing of one cell.
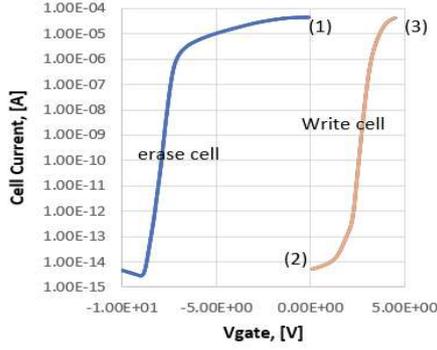
Fig. 4. Cell current with control gate bias for (a) erase cell and (b) programed cell

## III. DEVICE SIMULATION

### A. Erase/Program/Read simulation

Basic cell operation, program/erase/read, simulation is conducted. The bias condition of cell operation used in this simulation is described in Table 1.

TABLE I.       CELL OPERATION CONDITION

|  | Read | Program | Erase |
|---|---|---|---|
| Word Line (select) | 0 | 10 | 0 |
| Word Line (unselect) | 4.5 | 3 | 0 |
| TSG (select) | 4.5 | 3 | Floating |
| TSG (unselect) | 4.5 | 0 | Floating |
| BSG transistor | 4.5 | 0 | Floating |
| Bit Line (select) | 1 | 0 | Floating |
| Bit Line (unselect) | 0 | 3 | Floating |
| Nwell | 0 | 0 | 20 |

For the cell operation simulation, we examined one string of memory structure which is consisted of 7 storage cells and Bottom and Top select transistor as shown in Fig. 3(a). Fig. 4 shows the Bit Line current with respect to the gate voltage of selected cell after (a) erase and (b) write operation, which correspond to Fig. 3(b). For read operation, all unselected cells are biased to 4.5V and TSG/BSG is turned ON. Good erase operation is demonstrated and achieved Bit Line current level of 50uA at Vgate=0V (1). For the simulation of write operation, we first erase entire cells and immediately write one cell. Good blocking state is obtained as the Bit line current of string is less than 1e-12A at Vgate=0V (2). It is also noted that we achieved good pass current level of 40uA at gate bias of 4.5V (3), high enough to establish basic NAND operation.
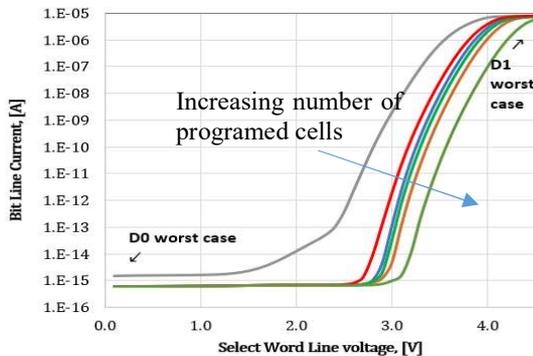


Fig. 5. Bit line current with respect to control gate voltage of single cell, with different number of programmed cells.
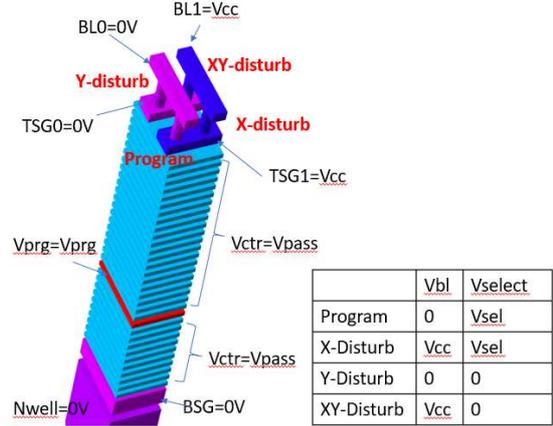


Fig. 6. Bias condition for programming operation used in 3D device simulation for 32-layer NAND device.

| | Vbl | Vselect |
|---|---|---|
| Program | 0 | Vsel |
| X-Disturb | Vcc | Vsel |
| Y-Disturb | 0 | 0 |
| XY-Disturb | Vcc | 0 |

So far we demonstrated one pattern of erase/program operation consisting of block erase and single cell program and read. It is important to test the worst case or pathological case. Data1 worst case is to read the erased cell when all other cells in the string were programed. Data0 worst case is to access the programed cell when all other cells are in the erase state. Fig. 5 is the read current for both data1 and data0 in various data patterns. For D1/D0 read, the current level is decreased/increased as the number of program cell is increased. Good ON and OFF ratio is achieved considering all data patterns. The worst case of D1/D0 simulation is used in
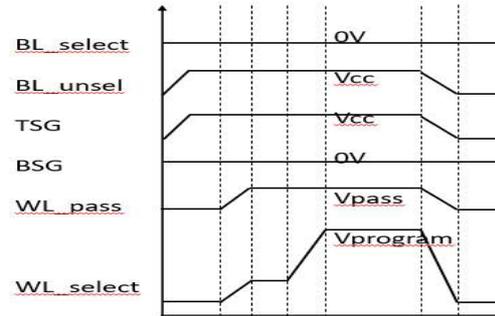


Fig. 7. Timing diagram of program operation

all subsequent simulations shown this paper.

### B. Program disturb simulation

The basic cell configuration of 3D NAND memory is that Bit Line is connected to each string and Word Line of each cell is connected at a common point in the block. This shared word line topology creates efficient block erase scheme but generate program disturb problem. Fig. 6 illustrate how programing of one selected cell produces various bias conditions on unselected cell. In order to prevent unwanted programing on unselected cell, all bias conditions applied to unselected cell must fit the condition of minimum electric field between body and control gate. TCAD device simulation of program operation was investigated capturing all four cells.
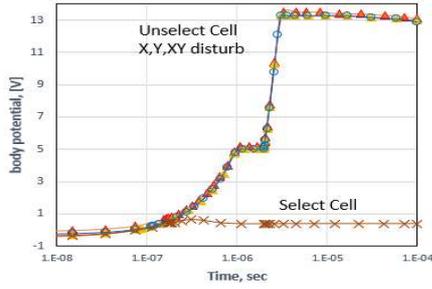
Fig. 8. Time dependent body potential from four cells defined in Fig. 6 with Lg of select gate transistor of 150nm.

This method enables to monitor program cell and all three disturb cells (X, Y, XY) at the same time. The timing diagram used on the program operation is shown in Fig. 7 as in [2].

We monitored the potential at the center of the cell during the program operation, Fig. 8. The body potential of select cell maintains ground and this ground potential is supplied by Bit Line through TSG device, which is in ON state. In the case of unselected cell, there is no path to make cell body ground since either both side of select transistor is OFF (Y, XY-disturb) or Bit Line is not grounded (X-disturb). Therefore the body potential level shoots up at the rising edge of the gate bias: self-boosting effect. The boosted potential will gradually drop and eventually reset to ground by leakage current of two select transistors. In order to avoid program disturb, this boosted body bias need to stay in high level during the program operation. One of the example of demonstrating poor self-boosting effect is when the TSG channel length is small (Fig. 9), which degrade the leakage control. In this case, boosted potential at the body drop fast creating higher e-field between body to control gate causing unwanted programing for the unselected cell. Note that the bias condition for Y-disturb is the worst among three disturb modes: the Vgs(gate to source voltage difference) level is zero, which is less favorable compare to other disturb modes, in which the Vgs level become negative [3,4].

Memory cell disturb behavior was examined in respond to various device parameters of select gate transistor (Fig. 10). In this study, we introduced the "critical potential", body potential at fixed time (10us), as a measure for disturb behavior. Effects of various transistor parameters on disturb margin are investigated, which includes (a) Work Function, (b) Source/Drain overlap, (c) interface charge density, and (d) bulk trap density. It is apparent that the ability to control
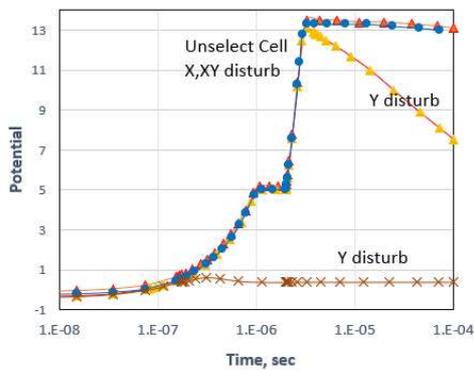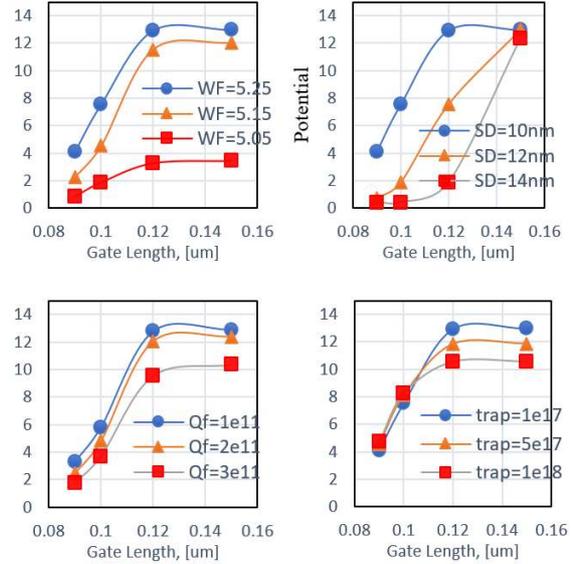


Fig. 10. Critical potential in various device parameters. (a) Workfunction (b) S/D overlap (c) Interface charge (d) Trap density

leakage current, either by increasing Vth (WF, Qf) or improving short channel control (Lg, S/D overlap) is the primary way to prevent the program disturb.

C. *Effect of traps*

Effect of bulk traps on disturb behavior is investigated Fig. 10(d). The long channel device containing high defect density exhibit poorer disturb margin. Interestingly this trend reversed for the short channel device: higher traps device produces better disturb margin. To understand this behavior, we investigated select gate transistor focusing on trap effects. Fig. 11 depicts the Id_Vg curve of select transistor with various trap densities showing traps pushing Vth higher. We believe this to be due to the extra charges coming from traps and contribute to the charge balance. The Poisson's equation in cylindrical coordinates become [5],

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\Psi(r)\right) = \frac{q}{\varepsilon_{si}}(N_a + N_T\,\Psi(r))$$

In our simulation traps are assumed to be of acceptor type, i.e., positively charged when occupied and neutral when not occupied. This equation implies that traps ($N_T$) are contributing to effective charge like dopant and subsequently
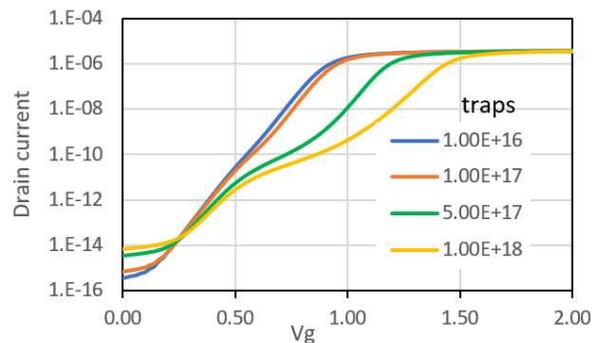


Fig. 9. Time dependent body potential from four cells with Lg of select gate transistor of 100nm.



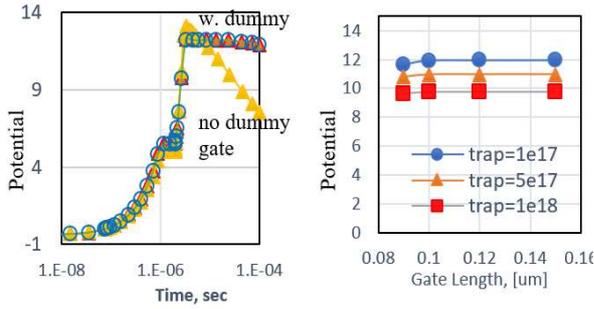Fig. 11. Id_Vg curve of select gate transistor with various trap concentrations.

Fig. 12. Time dependent body potential with (a) with/w.o. dummy (b) critical potential in various Lg and traps with dummy cell.

modulating Vth level. It is also observed that the off-state leakage current is increased with traps. Unlike workfunction effect where higher Vth provides lower leakage floor. Effect of traps is different; it increases the threshold voltage and leakage current at the same time. When the channel length is long, the leakage current is the main contributor of the disturb problem whereas for the short channel device, higher Vth attributed by high trap density plays a bigger role.

### D. Impact of dummy cell

It is common practice to place dummy cells right next to both select gate transistors to alleviate any edge cell adverse effect. We investigated the role of dummy cell on disturb behavior. Fig. 12(a) shows the Y-disturb potential plot with/without dummy devices. The presence of dummy cell improves self-boosting effect significantly. Fig. 12(b) is the same plot of Fig. 10(d) except that it contains dummy cell. The disturb margin is improved with dummy cell across all gate lengths.

Fig. 13(a) shows the conduction band energy diagram at the center of the cell. When there is no dummy, the energy barrier was lowered at the select gate device causing in the injection of electrons into the cell body, which reduces the boosted potential. Fig. 13(b) illustrate the 3D image of potential at programed cell showing reduction of potential at the center of the cell, where the influence of control gate is minimal.

### E. Impact of GIDL on erase operation

For erase operation, it requires high positive bias at the core of the cell, which produces high electric field between
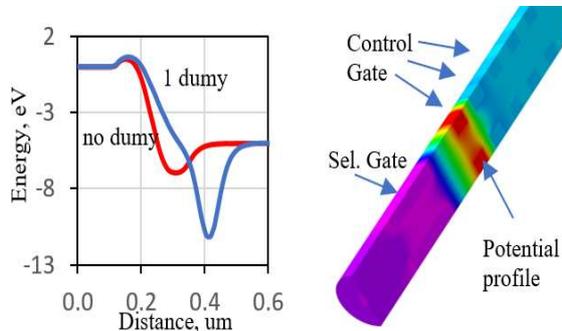


Fig. 13. (a) Conduction band diagram of the device with and w.o. dummy cell. (b) Potential distribution profile at programing operation.
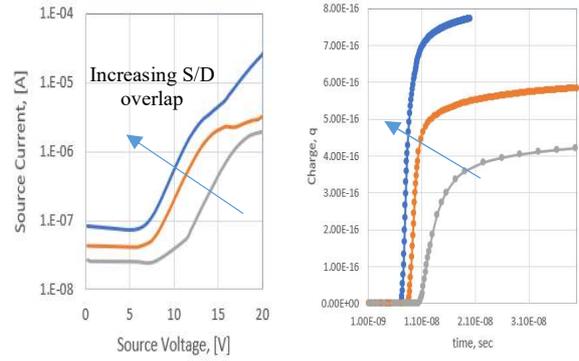


Fig. 14. (a) Source voltage-current curve at various s/d overlap. (b) Charge storage level during erase operation, with various s/d overlap. (S/D overlap: 60,80,100nm)

cell body to control gate enabling charge storage. This body bias is supplied from Nwell in the form of block erase scheme. Since the junction is revers biased, it takes time to raise the body potential. The conventional reverse junction leakage current is too small to raise the potential in time. Therefore, it requires GIDL current [6].

The GIDL current effect on erase operation is investigated. Fig. 14(a) shows the simulation result of source current for the device with various S/D junction overlap. The results show that current level is increased with larger junction overlap due to higher GIDL current. The rate of charge storage in the cell, which tracks the speed of the erase operation, is improved with increasing S/D overlap, Fig. 14(b). It is noted that larger junction overlap is adverse effect on disturb problem as observed previously in Fig.10 (b). Adding that the dopant diffusion in poly-Si material is highly variable, it is proper to have the channel length of the BST longer.

## IV. CONCLUSION

We investigated the device characteristics of select gate transistor on 3D NAND structure. We found that there is a room to shrink the channel length of the Top select gate device providing that there is a dummy cell. We project that Bottom Select Gate device has a limit to shrink the channel length considering program disturb and erase speed.

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