3D TCAD Model for Poly-Si Channel Current and Variability in Vertical NAND Flash Memory

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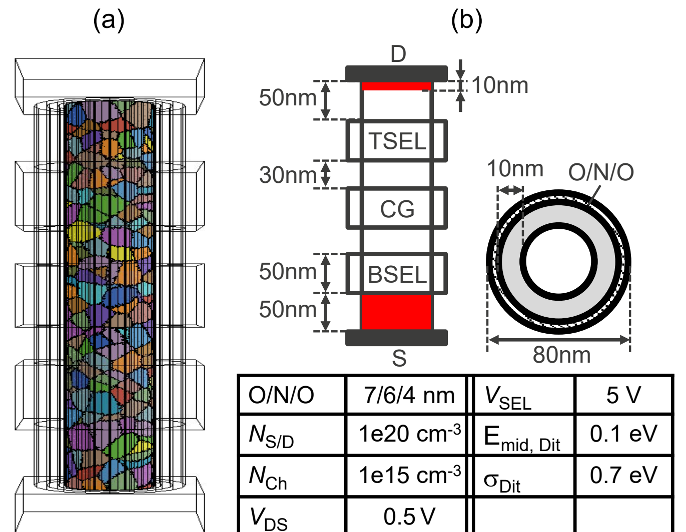
***Abstract*—The polycrystalline nature of state-of-the-art 3D NAND flash channels complicates on-current and variability modeling. We have therefore developed a 3D TCAD model that captures percolating current behavior and the resulting variability, and implemented it into the Global TCAD Solutions software package. In our simulation flow, we model the channel transport through the randomly generated grain structure with thermionic emission modulated by discrete traps at the grain boundaries, combined with a crystal orientation dependent mobility model inside the grains. We show that this approach can reproduce experimentally observed on-current temperature dependence and variability and use it to investigate the influence of defect density levels and average grain size.**

I. Introduction

Flash memory scaling has turned vertical, with devices stacked onto each other in strings with a cylindrical channel geometry to enhance bit density and improve memory operation [1]. In such a structure, the channel is created through crystallization of as-deposited amorphous silicon. Numerous grains with different crystal orientations are thereby formed, as the crystallization initiates at various random nucleation sites throughout the structure. The current conduction through such a polycrystalline channel leads to particular experimental observations that require a different modeling approach from the monocrystalline case to explain. First, the cell on-current (I_{ON}) is strongly reduced, as it is hampered by the increased scattering in the grain boundary regions that results from the change in crystal orientation [2]. Second, unwanted threshold voltage fluctuations are observed due to the trapping of charge carriers in the highly defective regions at the grain boundaries and at the oxide interfaces [3]. Third, inter-device variability in I_{ON} is significantly increased because of the random nature of the grain structure and the location of the defects. The degree of variability is strongly determined by the percolating nature of the current flow, which results from an interplay between the grain and defect configurations [4]. And finally, a positive temperature dependence of the current is typically observed, which is a sign of conduction by thermionic emission [5], [6].

To gain understanding of these intricate experimental observations, we present a 3D TCAD model implemented in the Global TCAD Solutions (GTS) package. We first detail the model and then show its use in reproducing I_{ON} temperature (T) dependence and variability of experimental macaroni channel NAND devices.



O/N/O	7/6/4 nm	V_{SEL}	5 V
$N_{\mathrm{S/D}}$	1e20 cm^{-3}	$E_{\mathrm{mid,\,Dit}}$	0.1 eV
N_{Ch}	1e15 cm^{-3}	σ_{Dit}	0.7 eV
V_{DS}	0.5 V		

Fig. 1: Investigated macaroni channel 3D NAND device structure. (a) Grain structure in the channel for average L_{grain} of 12 nm. The gates and other layers have been rendered transparent. (b) Configuration details and parameters. The red areas indicate the doping extensions at source and drain. V_{SEL} is applied at both BSEL and TSEL and is chosen large enough to ensure the SEL transistors are in the linear regime.

II. Models and simulation flow

The first step in the simulation flow is the definition of the device structure, followed by the Voronoi-based growth of grains in the channel region from randomly placed nucleation sites (see Fig. 1) [7]. The number of sites is determined by the specified average grain size (L_{grain}). Besides a random location and shape, each grain is also assigned a random crystal orientation. Where the grains meet, grain boundaries are defined as 2D interfaces to prevent a mesh dependence that occurs for boundaries with a finite volume.

At the grain boundaries, we model two main physical effects, based on previous ab-initio research [2]: discrete trapping and carrier velocity reduction. For the former, acceptor-type discrete traps are placed randomly at the boundary mesh points. The traps interact with the charge carriers through a Shockley-Read-Hall (SRH) process, which governs their occu-

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pancy. Once charged, they form local potential barriers that are key to reproducing the experimental temperature behavior. The random nature of these local trap potentials also renders the channel current non-uniform, with the charge carriers flowing in percolation paths. The amount of traps that are placed is determined by the specified trap density ($N_{\mathrm{t,GB}}$), which serves as a calibration parameter. The traps are also placed at the channel-oxide interfaces ($N_{\mathrm{t,ox}}$). The second effect that is modeled at the grain boundaries, carrier velocity reduction, results from increased carrier scattering due to the breaking of crystal periodicity in the grain boundary and is captured with a thermionic emission model. The current through a boundary between two grains (labeled with subscripts 1 and 2) is expressed as [8]:

$$J_{\mathrm{n1}} = J_{\mathrm{n2}} = q\left(v_{\mathrm{b}} n_2 - v_{\mathrm{b}} n_1 \exp\left(-\frac{\Delta \mathrm{E_b}}{\mathrm{k_B T}}\right)\right) \quad (1)$$

with q the elementary charge, v_{b} the barrier velocity, n the electron density, ΔE_{b} the uniform energy barrier height, k_{B} the Boltzmann constant and T the temperature. v_{b} acts as a collection velocity of carriers from one grain to the other [9]:

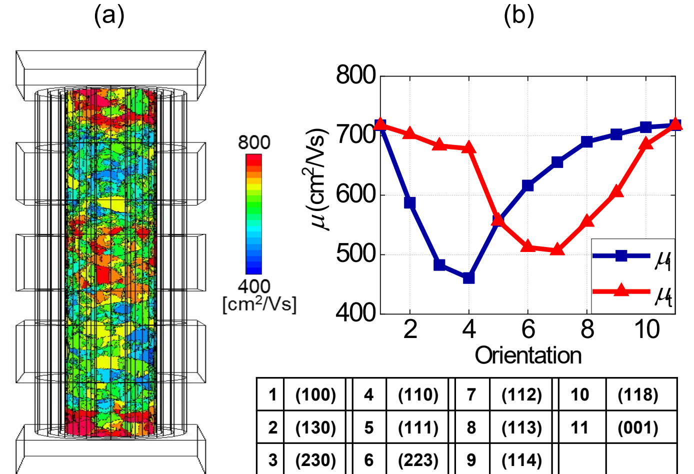
$$v_{\mathrm{b}} = \alpha v_{\mathrm{th}} = \alpha \sqrt{\frac{2 k_{\mathrm{B}} T}{\pi m^*}} \quad (2)$$

with v_{th} the thermal velocity, m^* the electron effective mass and α the scattering factor. Through α, v_{b} can be reduced to represent increased scattering.

Inside the grains, carrier transport is governed by standard drift-diffusion continuity equations, but with a crystal orientation dependent mobility. The random orientation means the oxide interfaces and the local electric field break the band structure symmetry differently in each grain [10]. We therefore extract the mobility at each mesh point from a table, based on the local crystal orientation relative to the nearest oxide interface (see Fig. 2). This table is calculated separately on a 2D slice of the device. On the slice, an effective mass Poisson-Schrödinger system is solved self-consistently, after which the obtained carrier subband wave functions and energy levels are fed into a Kubo-Greenwood based formula [11]. Combined with relaxation times from various scattering mechanisms (listed in Fig. 2), this module calculates a mobility value. A table of such mobilities is constructed by repeating this procedure for a representative sample of crystal orientations and for each V_{CG}. Fig. 3 shows the full simulation flow.

III. Simulation Results and Calibration

We first confirm in Fig. 4 that the implemented model qualitatively reproduces the expected T dependence of I_{ON} for a single device (see details in Fig. 1(b)) with varying L_{grain} and $N_{\mathrm{t,GB}}$. The spread with T in I_{ON} indeed increases and becomes more positive for smaller grains and larger $N_{\mathrm{t,GB}}$, while I_{ON} itself decreases. This is a result of the increased presence of trap-induced energy barriers in the current paths, which hinder carrier transport and require thermal energy to overcome. The uniform barrier height at the grain boundaries



1	(100)	4	(110)	7	(112)	10	(118)
2	(130)	5	(111)	8	(113)	11	(001)
3	(230)	6	(223)	9	(114)		

Fig. 2: (a) Calculated intrinsic non-uniform mobility in the macaroni channel and (b) longitudinal (μ_{l}) and transversal (μ_{t}) mobility variation with the surface orientations listed in the table. Considered scattering mechanisms are optical and acoustic phonon scattering, inter-valley and surface roughness scattering [11]. V_{CG} is 1 V. Other configuration details are listed in Fig. 1.

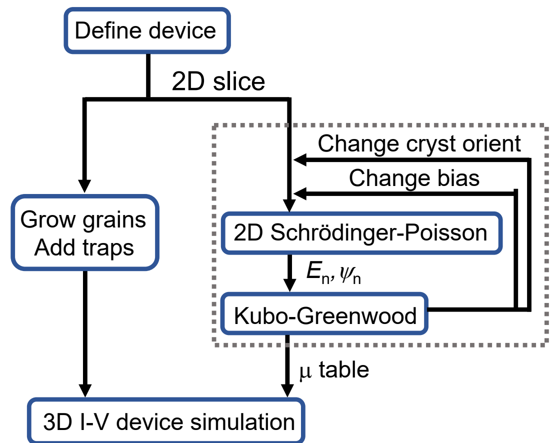


Fig. 3: Flowchart of the simulation procedure implemented in the GTS software package. E_{n} and ψ_{n} are energy eigenvalues and state wave functions respectively, obtained from the converged self-consistent Schrödinger-Poisson loop.

ΔE_{b} is set to zero, which means the presence of traps alone suffices to explain the positive T dependence.

We see the same trends in the I_{ON} distributions in Fig. 5. Here, $N_{\mathrm{t,ox}}$ and $N_{\mathrm{t,GB}}$ are varied independently for 10 random seeds of the trap and grain configurations. The average L_{grain} is assumed to be close to the channel thickness and is therefore fixed at 12 nm [4]. Both increasing oxide and grain boundary trap density are shown to invert the T dependence from negative to increasingly positive, while I_{ON} is decreased. At the same time, the distributions grow wider, pointing to stronger inter-device variability due to enhanced current percolation. Increasing $N_{\mathrm{t,GB}}$ has a stronger effect than $N_{\mathrm{t,ox}}$: as the grain

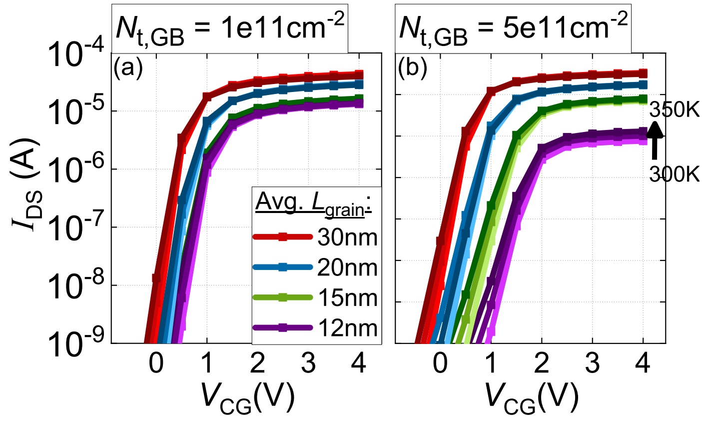


Fig. 4: Simulated transfer characteristics for a single macaroni device for varying grain size and temperature (300K, 325K, 350K) and two values for $N_{t,GB}$. $N_{t,ox}$ is fixed at 1e12 cm^{-2}. Other configuration details are listed in Fig. 1(b).

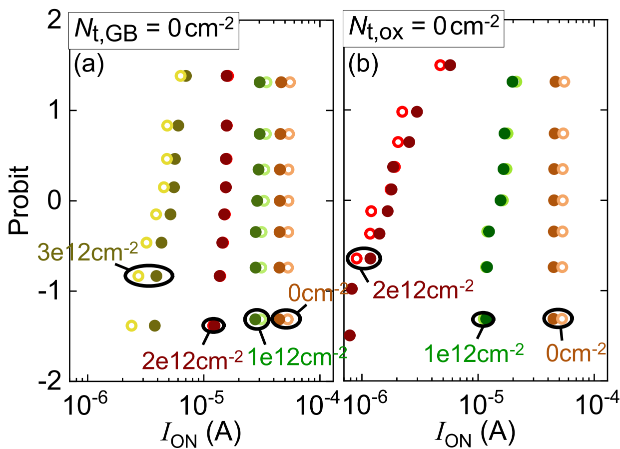


Fig. 5: Simulated I_{ON} distributions for random grain and trap configurations, extracted at V_{CG}=V_T + 2 V with V_T at I_{OFF}=1e-9 A/μm, for varying (a) $N_{t,ox}$ and (b) $N_{t,GB}$. Average L_{grain} is 12 nm. Open symbols correspond to a temperature of 300 K, closed to 350 K. Other configuration details are listed in Fig. 1(b).

boundaries run through the full thickness of the channel, traps at those boundaries are located more directly in the current path of the charge carriers.

Finally, we calibrate the model to experimental I_{ON} distributions in Fig. 6. The measured devices are three-gate test vehicles fabricated on a 300 mm platform with a process flow inspired by Bit-Cost Scalable technology [12], [13]. The target dimensions and doping levels are the same as those listed for the simulated configurations in Fig. 1(b). After processing, the experimental devices have been treated with a high pressure hydrogen anneal, which is known to improve performance in terms of I_{ON} and STS by curing defects [14]. Again, we assume that the grain size (L_{grain}) is of the same order as the channel thickness (12 nm). Fig. 6 shows a good agreement between experimental and simulated

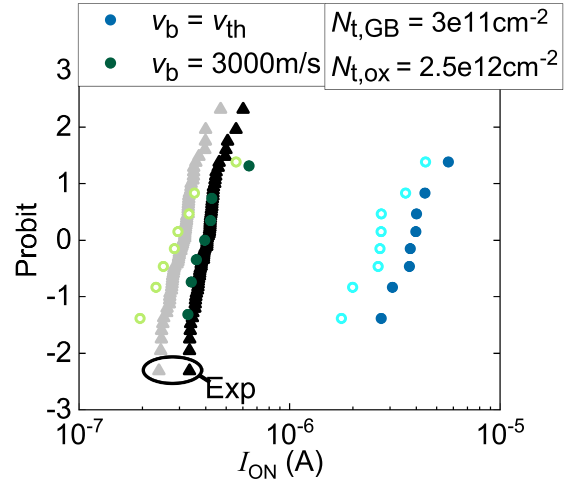


Fig. 6: Calibration of simulated I_{ON} distributions and temperature dependence to experimental results. Average L_{grain} is 12 nm. Open symbols correspond to a temperature of 300 K, closed to 350 K. Other configuration details are listed in Fig. 1(b).

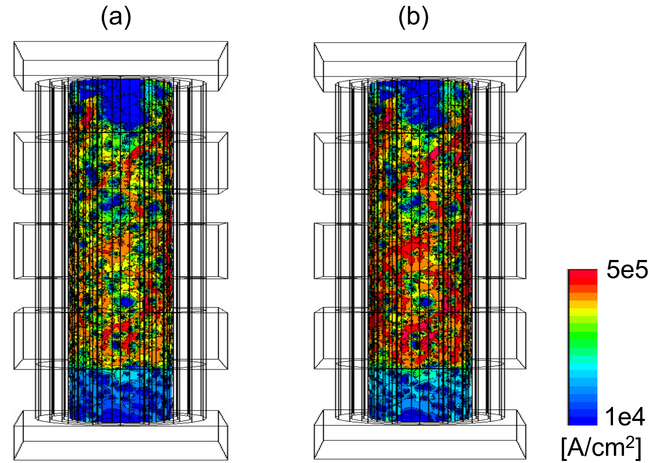


Fig. 7: Electron current density in the channel for a T of (a) 300 K and (b) 350 K. V_{CG} is 4 V. Average L_{grain} is 12 nm. $N_{t,ox}$ and $N_{t,GB}$ have the calibrated values of 2.5e12 cm^{-2} and 3e11 cm^{-2}, respectively. Other configuration details are listed in Fig. 1.

distributions. The temperature dependence and distribution spread is matched by adjusting $N_{t,ox}$ and $N_{t,GB}$, while the I_{ON} magnitude is captured by lowering the scattering factor α in Eq.(1). Fig. 7 illustrates the current density for one of these simulated configurations at the measurement temperatures: the current percolation caused by the grain boundaries and traps is clearly visible. As the temperature is increased, the percolation paths grow wider and the flow of current increases as a result of enhanced thermionic emission.

IV. Conclusion

We reported on a polycrystalline channel current model and simulation flow for 3D NAND flash strings that has been implemented in the GTS TCAD package. This model captures the particular conduction in a random grain structure with discrete traps and a reduced carrier velocity at grain boundaries, combined with an orientation dependent intra-grain mobility. With this approach, we showed that an increased grain boundary trap density and a decreased grain size both not only deteriorate I_{ON}, but also render the I_{ON} temperature dependence more positive. Looking at statistical distributions, we showed a larger effect of grain boundary traps on the distribution spread than oxide interface traps. Finally, we reproduced experimental temperature behavior and statistical distribution of I_{ON} through a calibration of trap densities and carrier velocity at the grain boundaries. For future research, the presented simulation flow can be a valuable tool in the investigation of current conduction mechanisms and variability in scaled 3D NAND devices.

Acknowledgments

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