Numerical simulations of nanosecond laser annealing of Si nanoparticles for plasmonic structures

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***Abstract*—This paper reports numerical simulations of nanosecond laser thermal annealing of plasmonic structures based on Si-nanoparticles embedded in a SiO_2 matrix. From these simulations, we extracted guidelines for the structure design to be adopted. This study also investigates the expected laser annealing process window and the influence of nanoparticles coverage.**

Keywords—Laser annealing, Si nanoparticles, melt, plasmonic nanostructures.

I. Introduction

Noble metal nanoparticles exhibiting localized surface plasmon resonance (LSPR) show remarkable light scattering and absorption properties. The LSPR frequency is slightly tunable by the nanostructure size, geometry and local medium but is mainly controlled by the free electron density. Thus, a key advantage of using semiconductor nanoparticles for plasmonic structures is that their free carrier concentrations can be tuned by doping. Among plasmonic materials, heavily doped semiconductors such as Si Nanoparticles (Si-NPs) receive much attention thanks to their potential use in the infrared spectral range [1]. They find their application in the domains of biosensing, subwavelength microscopy or photovoltaics [2]. However, due to self-purification, doping Si-NPs is a challenge [3-5]. Doping levels and activation ratios become concepts to be reviewed. There are several different techniques compatible with CMOS technology to fabricate size controlled Si-NPs (2-10 nm) with narrow size distribution. A first one is leveraging Plasma Immersion Implantation (PIII) which allows the control of density and position of Si-NPs by tuning the plasma and the implantations conditions (energy and dose) [6]. The advantage of this technique is that it provides high throughput capabilities in the low energy regime and is well adapted for high dose implant applications. A second one uses the SiO/SiO_2 layer structure deposited by e-beam evaporation [7]. In that case, the doped Si-NPs embedded in a SiO_2 matrix are achieved thanks to the subsequent high temperature phase separation. Dopant introduction is made during the Si-rich layer deposition. This method is interesting for the formation of multilayers of small (2-5 nm) size controlled Si-NPs. For both processes, a subsequent high temperature annealing for dopant activation is mandatory. In this context, Ultra Violet Nanosecond Laser Annealing (UV-NLA) is a promising choice to achieve efficient dopant activation at the nanoscale. This technique allows working in near out-of-equilibrium conditions (nanosecond timescale at peak temperature near melting point) and fosters electrical dopant activation above the solid solubility limit [8]. This work presents preliminary simulation results carried out to optimize UV-NLA parameters. The aim of this study is to determine the UV-NLA energy density necessary to reach the Si-NPs melting point without melting the substrate which may generate detrimental surface roughness. We will also be able to determine the most favorable SiO_2 buffer layer thickness.

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II. Si-NPs modeling

The expected experimental structure is illustrated in Figure 1. In our 2D simulations, the model consists in a single layer of undoped Si-NPs with a quasi-spherical shape (3-7 nm diameter), embedded in a SiO_2 matrix below a 2 nm thin SiO_2 surface layer. Both cases amorphous and crystalline NPs must be considered, in particular for Si-NPs that will be synthesized by PIII process because initially crystalline NPs could be amorphised by further dopant ion implantation. Figure 1 illustrates the cross-section view of the corresponding test structure, used for 2D simulations, with 5 nm diameter Si-NPs with 5 nm spacing. These dimensions correspond to those given in [7]. The structure lays on a SiO_2 buffer layer (thickness varying from 10 to 50 nm) on top of a Si substrate. Based on this view, the ratio between the surface occupied by the NPs and the section area of the whole "SiO_2 embedded matrix" defines the coverage level of Si-NPs. In this example, the calculated coverage is about 33.7 % which can be related to a Si-NPs density of $1.7.10^{12}$ cm^{-2}. This value is in the same order of magnitude as in [7]. The first step was to consider extreme cases: maximum coverage (100 %) with a full sheet Si layer (amorphous and crystalline) and minimum coverage (0 %) by only keeping the SiO_2 matrix thickness. The resulting simplified structures can be investigated by 1D simulations (cf. Figure 2).

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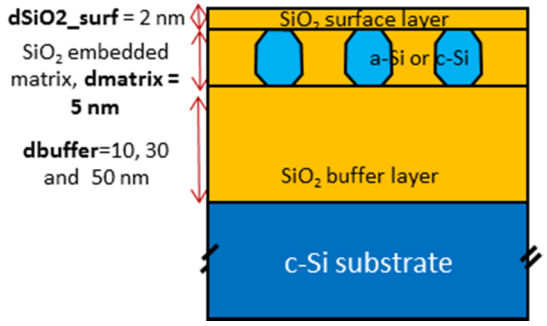

Fig. 1: Si-NPs modeling for 2D numerical UV-NLA simulations. 3 Si-NPs of 5 nm diameter spaced of 5nm, the coverage level is 33.7 %. This corresponds to a Si-NPs density of $1.7.10^{12}$ cm^{-2}.

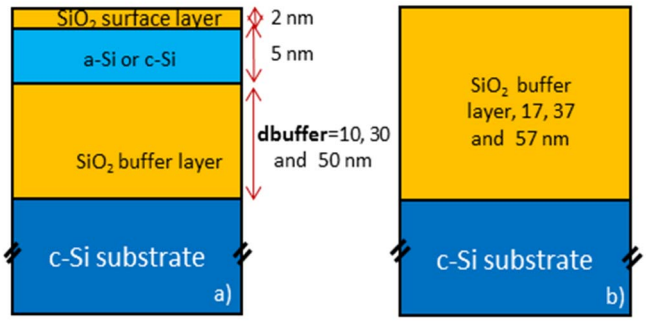

Fig. 2: Modeling of extreme coverage levels of Si : a) 100 % and b) 0 % for 1D UV-NLA simulations. In the case a), Si-NPs are replaced by a blanket Si layer. In the case b), only the SiO_2 matrix remains

III. Numerical Simulations

A. One dimensional simulations (1D)

Numerical simulations were performed using LIAB simulation software described in [9]. This tool solves self-consistently the heat equation coupled to the time harmonic solution of Maxwell equation (UV laser light coupling), including temperature dependency of materials parameters and phase change (here using an enthalpy-based approach). The laser annealing system for our future experiments being the SCREEN LT-3100 platform, we used the corresponding laser pulse with 160 ns duration and a 308 nm wavelength. In a first approach, 1D numerical simulations were carried out with the simplified theoretical structures shown in Figure 2. All simulation conditions are summarized in table I.

N°	5 nm Si layer	SiO_2 buffer thickness (nm)
1	a-Si	10
2	a-Si	30
3	a-Si	50
4	c-Si	10
5	c-Si	30
6	c-Si	50
7	_	17
8	_	37
9	_	57

Table I: Framework of 1D numerical simulations performed in this work in order to delimit the UV-NLA energy densities and avoid the substrate melt. In grey simulations are performed with a full sheet Si layer and no Si layer for the others. In this case, the Si layer is replaced by SiO_2 in order to preserve the same structure thickness which is important for laser heating.

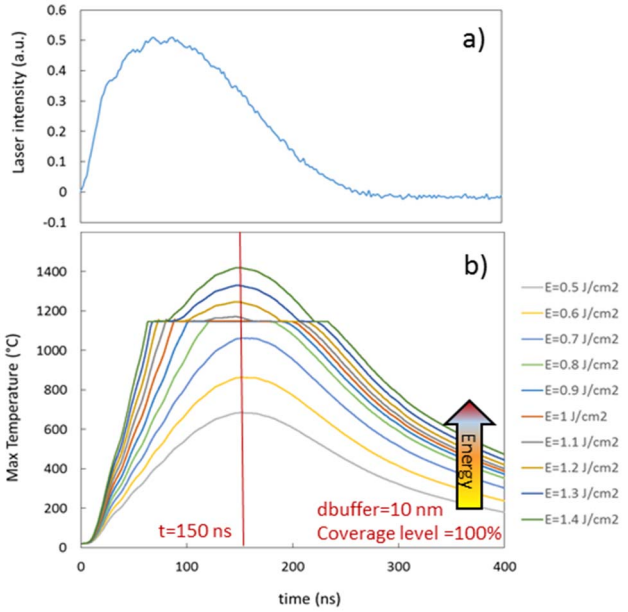

Fig. 3: a) : laser pulse profile used for 1D numerical simulations. b) : max temperature into the a-Si layer versus time and laser energy (J/cm²). The thickness of SiO_2 buffer layer dbuffer=10 nm. The maximum temperature is reached at 150 ns.

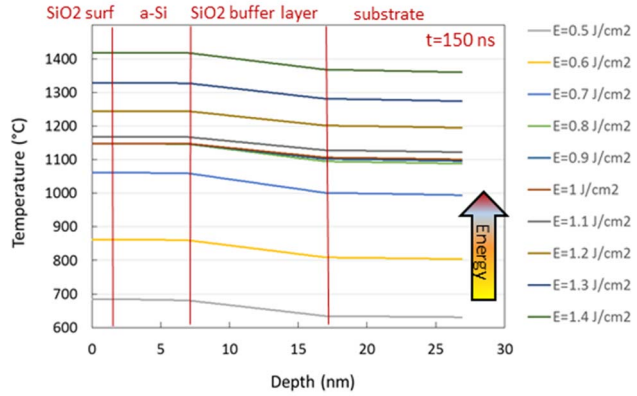

Fig. 4: 1D numerical simulations. Temperature as a function of depth in the structure a) of Fig.2 and laser energy density at t=150 ns and dbuffer=10 nm for a a-Si layer. This graph provides information on the temperature in both in the a-Si layer and substrate.

These simulations take also into account the initial phase of the Si film (crystal or amorphous) as well as temperature and phase dependent optical and physical material parameters at the given wavelength. The temperature in the top Si layer as a function of time is plotted in Figure 3. The temperature goes up as the energy density increases until reaching a plateau. This one corresponds to the beginning of the a-Si layer melt. The plateau becomes larger when the energy rises until the totality of the a-Si layer is melted. Afterwards, the temperature still increases in the Si layer. This graph allows the identification of the energy density corresponding to the Si layer melt onset and its full melt. Then, when the maximum temperature is reached in the Si layer (t=150 ns), we can also access to the spatial temperature depth profile shown in Figure 4. Thus, we can determine the temperature both in the top Si layer and the Si substrate.

Figure 5 shows the predictions for different buffer layer thicknesses: 10, 30 and 50 nm and in both cases of amorphous (full lines) and crystalline Si layer (dotted lines). Laser energy densities shown in the graph are related to the beginning of the

melt in the top Si layer. Note that these energy densities decrease as the buffer oxide becomes thicker. Indeed, in that case, the heat is less well evacuated by the substrate due to increased thermal insulation from the buffer layer. The temperature shift between c-Si and a-Si based structures is attributed to the melting temperature difference: Tm(a-Si) =1147°C and Tm(c-Si) =1414°C [10]. Melting Si-NPs without melting the Si substrate already appears much easier for a-Si than for c-Si-NPs. Besides, Figure 6 shows the critical energy densities leading to the melt of the a-Si layer (full lines) or the substrate (dotted lines). The energy densities allowing the Si layer melt and keeping the substrate below 1414°C, constitute the process window (PW). At first, the choice of a thick buffer layer seems to be relevant to keep a sufficient temperature difference between the top Si layer and the substrate. However, in the case of thicker SiO_2 buffer layer, the temperature increases severely near the surface structure and can reach the melt temperature of the SiO_2 matrix (1713°C). Again, this is due to the high thermal insulation from the presence of thick buffer layer as we saw above.

The conclusion is that it is preferable to work with a buffer layer with a maximum thickness of 30 nm. PWs determined with this 1D approach are summarized in table II for a-Si and c-Si layers. We also give schematic cross sections to illustrate physical phase in the multilayer structures. The energy densities shown in red represent the limitation due to the matrix melt and not the substrate melt.

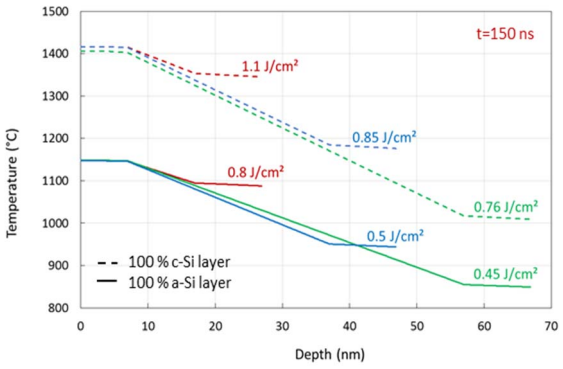

Fig. 5: 1D numerical simulations. Temperature as a function of depth at t=150 ns for dbuffer= 10 (red), 30 (blue) and 50 nm (green). The indicated energy densities correspond to ones necessary to reach Si-NPs melt.

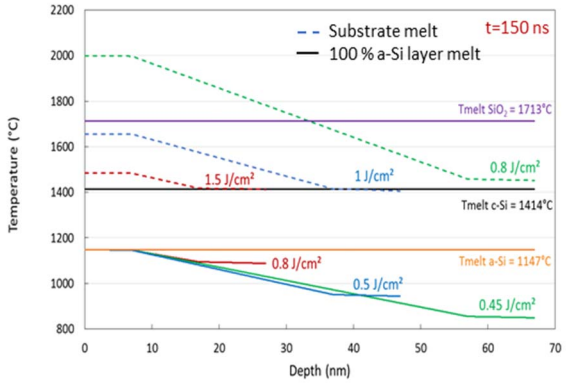

Fig. 6: 1D numerical simulations. Temperature as a function of depth at t=150 ns when dbuffer=10 (red),30 (blue) and 50 nm (green) and for an amorphous 100 % a-Si layer as an example (full lines). Dotted lines show the temperature and energy densities corresponding to the substrate melt. Here, it is obvious that using a thick buffer layer (>30 nm) leads to a poor heat diffusion and to a severe temperature increase at the surface.

phase: solid / liquid	a-Silayer (100%)		c-Silayer (100%)		SiO2 (0%)
Buffer thickness (nm)	E(a-Si NPs melt) J/cm²	E(substrate melt) J/cm²	E(c-Si NPs melt) J/cm²	E(substrate melt) J/cm²	E(substrate melt) J/cm²
10nm (17nm for 0% Si layer)	0.80	1.50	1.10	1.40	1.30
30nm (37nm for 0% Si layer)	0.50	1.00	0.80	1.10	1.00
50nm (57nm for 0% Si layer)	0.45	0.70 Limited by SiO2 melt (1713°C)	0.76	0.85 Limited by SiO2 melt (1713°C)	1.00

Table II: Summary of 1D numerical simulations performed in this work. Schematic cross sections indicate crystalline phase of the top Si layer: solid in red and liquid in blue. Energy densities (J/cm²) defined a PW which also takes into account the SiO_2 melting point when the buffer layer is too thick.

B. Two dimensional simulations (2D)

2D simulations complete this work by using the model described in Figure 1. For various SiO_2 buffer thicknesses, Figure 7(a) shows the onset of the Si-NPs phase change during the laser annealing with the corresponding energy densities. Figure 7(b) illustrates the onset of the substrate melt. Molten areas are indicated in blue whereas solid ones are in red. The predicted PW (0.90 - 1.20 J/cm^2) for this NPs coverage (33.7 %) is narrower than the one found for a 100 % coverage (0.80 - 1.50 J/cm^2). The limitation due to the heat confinement at the surface for buffer layer thicknesses beyond 30 nm is observed in the case of 50 nm where the whole "SiO_2 embedded matrix" becomes liquid as the same time as the substrate.

Figure 8 gives the simulated PW thanks to simulations performed with various 5 nm diameter a-Si and c-Si-NPs coverage levels, indicated in the insert part and for a 10 nm thick SiO_2 buffer layer. As the number of Si-NPs increases, the energy necessary to melt the nanoparticles and the substrate decreases. The SiO_2 matrix is transparent to the UV-NLA but the more silicon in the matrix the more energy radiation is absorbed in the matter.

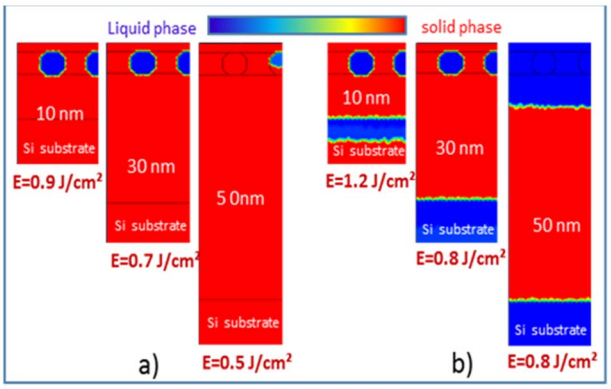

Fig. 7: 2D simulation of laser annealing for three 5 nm diameter aSi-NPs, 5 nm spaced (coverage level of 33.7 %); melting areas at the onset of a-Si NPs melt (a) and substrate melt (b) and corresponding laser energy densities. In the case of a 50 nm thick SiO_2 buffer layer, the substrate melt is accompanied by the matrix one.

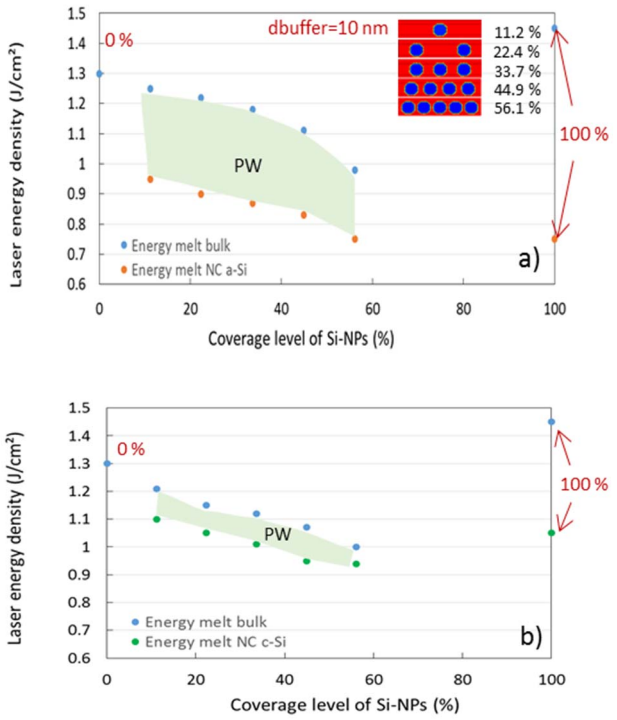

Fig. 8: Process window defined with various coverage levels of aSi-NPs (a) and cSi-NPs (b).

This absorption fosters the temperature elevation in the Si-NPs. However, we can observe that in the case of a full Si layer instead of NPs (case of 100% of Si), the energy density to melt the substrate is higher compared to the other coverage levels. We can explain this by a change in optical characteristics namely the reflectivity of the structure. To verify this point, we have plotted in Figure 9 the evolution of the reflection coefficient at 308 nm as a function of the coverage levels.

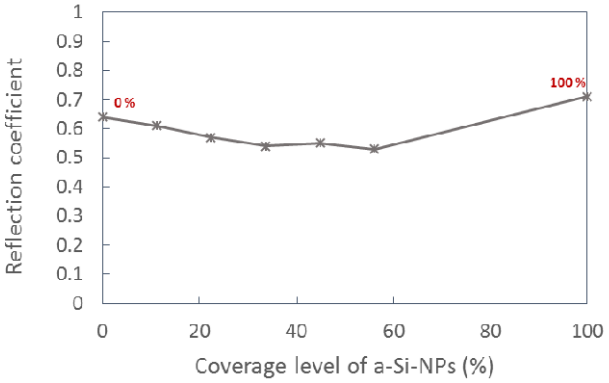

Fig.9: Reflection coefficient as a function of coverage levels of Si in the SiO_2 matrix. Extreme cases 0% and 100% also appear in the graph to compare

This coefficient is given for a laser beam with an energy density level below the melting threshold.

IV. Conclusion

In order to prepare experimental nanosecond laser annealing of plasmonic structures based on Si-NPs embedded in a SiO_2 matrix, we performed 1D and 2D numerical simulations taking into account electromagnetic and thermal aspects of such a process. These simulations provide guidelines on the design of the structures to be annealed and on the expected process windows. Such process windows depend at first order on the phase of the Si-NPs just before laser annealing (crystalline or amorphous), then on the oxide thickness between the Si-NPs and the Si substrate, and finally on the Si-NPs surface coverage. Amorphous Si-NPs lead to a wider process window compared to their crystalline counterparts thanks to the much lower melting point of a-Si. Si-NPs located 2 nm below the surface should preferably be separated from the Si substrate by a buffer SiO_2 layer thinner than 30 nm in order to reach Si-NPs melting point (for optimal dopant activation) before that of the Si substrate or the top oxide layer.

References

[1] D. Rowe, J.S. Jeong, K.A Mkhoyan and U.R. Kortshagen, "Phosphorus-doped silicon nanocrystals exhibiting mid-infrared localized surface plasmon resonance", Nano Letters, vol. 13 (3), pp.1317-1322, 2013.
[2] H. Atwater and A. Polman, "Plasmonics for improved photovoltaic devices", Nature materials vol.: 9 (3), pp. 205-213, 2010.
[3] S. Ossicini et al., "Simultaneously B- and P-doped silicon nanoclusters: formation energies and electronic properties", Applied Physics Letters, vol. 87 (17), 173120, 2005.
[4] M. Peregro, C. Bonafos and M. Fanciulli, "Phosphorus doping of ultra-small silicon nanocrystals", Nanotechnology, vol. 21 (2), pp. 1-6, 2010.
[5] S. Gutsch *et al*, "Electronic properties of phosphorus doped silicon nanocrystals embedded in SiO2", Applied Physics Letters, vol. 106 (11), 113103, 2015.
[6] C. Bonafos *et al*, "Controlled fabrication of Si nanocrystal delta-layers in thin SiO2 layers by plasma immersion ion implantation for nonvolatile memories", Applied Physics Letters, vol. 103 (25), 253118, 2013.
[7] H. Rinnert, O. Jambois, and M. Vergnat, "Photoluminescence properties of size-controlled silicon nanocrystals at low temperatures", Journal of Applied Physics, vol.106 (2), 023501, 2009.
[8] K. Huet, F.Mazzamuto, T.Tabata, I. Toqué-Tresonne, and Y. Mori, "Doping of semiconductor devices by laser thermal annealing", Materials Science in Semiconductor Processing, vol. 62, pp.92-102, 2017.
[9] S.F. Lombardo *et al*, "Theoretical study of the laser annealing process in FINFET structures", Applied Surface Science vol. 467-468, pp. 666-672, 2019.
[10] A. La Magna, P. Alippi, V. Privitera, G.Fortunato, M. Camalleri, B. Svensson, "A phase-field approach to the simulation of the excimer laser annealing process in Si", Journal of Applied Physics, vol.95 (9), pp.4806-4814, 2004