Trap Dynamics based 3D Kinetic Monte Carlo Simulation for Reliability Evaluation of UTBB MOSFETs

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***Abstract*—Trap dynamics based 3D Kinetic Monte Carlo (KMC) simulator is developed to offer physical insights into the electrical characteristics degradation and quantitative reliability evaluation for advanced MOSFETs. The physics-based 3D KMC simulation enables to reproduce the evolution of stress-induced charge distribution in the multi-layer dielectrics and identify the trap impact on the degradation of device performance. Simulation results of UTBB FDSOI MOSFETs reveal that assumption of the uniform charge distribution in the dielectrics induced by stress underestimates the statistical degradation and variability. It also shows that the higher intrinsic trap density of back-gate oxide leads to the larger degradation and its variability, especially for the increased back-gate bias case.**

Keywords—trap dynamics, kinetic Monte Carlo, UTBB, performance degradation, variability

I. Introduction

Trap induced time-dependent variability and reliability have emerged as one of the major challenging issues for advanced technology [1-3]. The trap dynamics during operation, including charging and discharging as well as the interactions with the ions or other traps, have a crucial impact on the device performance and reliability [4-5]. Therefore, the comprehensive physics-based simulation is highly desired for the understanding of trap behaviors and reliability identification.

In this work, the multiple trap-related physics processes in the multi-layer gate stacks are simulated by 3D Kinetic Monte Carlo (KMC) method, which is capable of reproducing the stress-dependent charge distribution and evaluating the degradation of the electrical characteristics for reliability optimization. Ultra-Thin Body and Box (UTBB) FDSOI device delivers superior benefits in the fields of mobile and IoT application [6-8]. The UTBB device reliability associated with the unique back gate modulation is investigated by the developed simulator. The impacts of back-oxide traps as well as remote Coulomb scattering (RCS) on the reliability degradation during different back-gate biases are clarified.

II. Simulation Method

The underlying stochastic trap behaviors during stress are responsible for the time-dependent variability and degradation [9-10]. Therefore, the 3D KMC method is employed to address the complex physical processes. The fully-coupled trap behaviors in the multi-layer gate stacks implemented in the 3D KMC simulator are depicted in Fig. 1. The processes can be categorized as the charging/discharging of intrinsic/newly-generated traps, trap generation and recombination with neighbor ions, as well as the interactions with other traps [11]. The modeling equations for corresponding trap behaviors sketched in Fig. 1 are listed as follows.

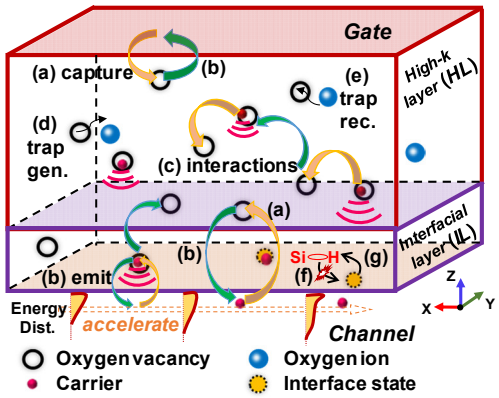

Fig. 1. Schematics of trap behaviors (a)-(g) in the gate dielectrics and the corresponding modeling equations: Eqs. (1)-(12) [9]. The mobility degradation due to remote Coulomb scattering (RCS) is described with Eqs. (13)-(15) [15].

Process (a)/(b) denotes the charge trapping/de-trapping from channel and gate as expressed in Eqs. (1)-(2).

$$P_{c,cg} = \delta_{c,cg} v_n n_{c,g} \exp(-\frac{u_c - \lambda(F/F_0)^\rho}{k_B T}) \quad (1)$$

$$P_{e,eg} = \delta_{e,eg} v_n N_{c,g} \exp(-\frac{u_e + \lambda(F/F_0)^\rho}{k_B T}) \quad (2)$$

where v_n is thermal velocity, $\delta_{c,cg}/\delta_{e,eg}$ is capture/emission coefficient, λ and ρ are enhancement factors of the electric field, $u_{c,e}$ are zero-field thermal barriers.

Process (c) represents the charge exchange between traps as described in Eq. (3).

$$P_{ij} = T_{ij} f_c \exp(-\frac{\varepsilon_{ij}}{k_B T}) \quad (3)$$

where T_{ij} is tunneling coefficient, ε_{ij} is the thermal barrier from the ith trap to jth trap.

Process (d)/(e) shows the generation/recombination of bulk traps, whose probability can be written as Eqs. (4)-(5).

$$P_g = f_g \exp(-\frac{E_a - \gamma F}{k_B T}) \quad (4)$$

$$P_r = f_r \exp(-\frac{E_r}{k_B T}) \quad (5)$$

where $f_{g,r}$ are lattice vibration frequencies, γ is bond polarization factor, $E_{a,r}$ are the zero-field activation energies of trap generation and recombination, respectively.

Process (f)/(g) illustrates the generation/recombination of interface states, which follows the truncated harmonic oscillator model as expressed in Eqs. (6)-(12). The bond breakage of Si-H bonds is contributed to the competitive

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mechanisms of antibonding (AB) and multi-vibrational excitation (MVE) [12-13].

$$P_{AB,n} = \int f(E)g(E)\sigma_0(E - E_b + E_i)^p v(E)dE \quad (6)$$

$$P_{MVE} = \int f(E)g(E)\sigma_0(E - \hbar\omega)v(E)dE \quad (7)$$

$$P_u = P_{MVE} + f_e \exp(-\frac{\hbar\omega}{k_B T}) \quad (8)$$

$$P_d = P_{MVE} + f_e \quad (9)$$

$$P_{ig,n} = P_{AB,n} + f_e \exp(-\frac{E_b - E_i}{k_B T}) \quad (10)$$

$$P_{ig} = \frac{1}{k}\sum_n P_{ig,n}(\frac{P_u}{P_d})^n,\ k = \sum_n (\frac{P_u}{P_d})^n \quad (11)$$

$$P_{ir} = f_e \exp(-\frac{E_{ir}}{k_B T}) \quad (12)$$

where $E_{b,ir}$ are the dissociation and passivation energies of Si-H bond, respectively.

The detailed flowchart of trap dynamics simulation is illustrated in Fig. 2. The model parameters related to material properties containing band-breakage energy and thermal barriers for state transition (i.e. empty↔occupied) have been validated in [9]. The 3D electrostatics distributions obtained from device simulator are used for computing the event probabilities according to the above equations. The trap and charge distributions are updated along with the simulation time.

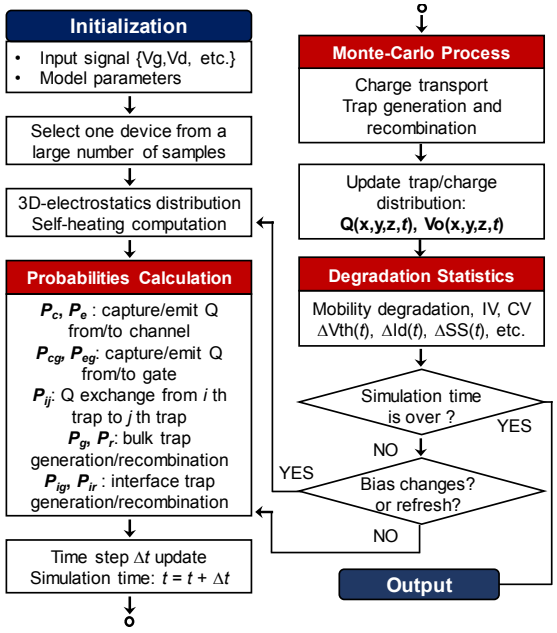

Fig. 2. The flowchart of 3D KMC implement of trap dynamics simulation for reliability evaluation.

The developed 3D KMC simulator incorporating the commercial TCAD tool e.g. Sentaurus [14] allows to evaluate the mobility degradation considering the effect of RCS [15] with the following equations (13)-(15), thereby the holistic time-dependent degradation of electrical characteristics can be acquired according to the time evolution of charge distribution. The variability is based on the statistical simulations of a large ensemble of devices which are unique in the trap configurations (e.g. initial locations, energy levels and thermal barriers).

$$\frac{1}{\mu} = \frac{1}{\mu_{other}} + \frac{D_{rcs} D_{rcs\_HL}}{\Delta\mu_{rcs}} \quad (13)$$

$$\Delta\mu_{rcs} = \mu_{rcs} f(N_{A,D}, T, g_{screening}) / f(F_\perp) \quad (14)$$

$$f(F_\perp) = 1 - \exp(-\xi F_\perp / N_{dep}) \quad (15)$$

Here, the enhanced Lombardi model is applied to account for the mobility degradation due to RCS effect, where μ_{other} is the mobility contributions from other degradations. $F_\perp$ is the transverse field, D_{rcs}, D_{rcs_HL} are damping factors and g_{screen} is screening factor.

III. Results and Discussion

The schematic of UTBB FDSOI device and the corresponding spatial distributions of traps in the front-gate stacks and back-oxide layer (Box) are illustrated in Fig. 3.

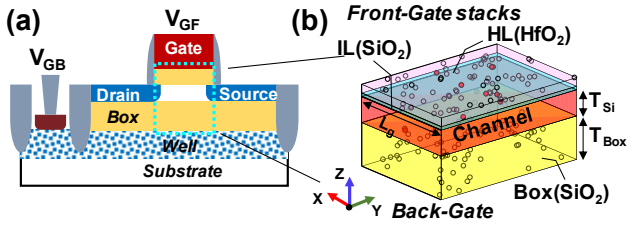

Fig. 3. (a) Schematic of the UTBB FDSOI device. (b) The traps (black circles) and charges (red circles) in the multi-layer gate stacks and back-oxide layer (Box).

The time evolutions of charge number (#) and distribution in the device during the typical BTI stress and recovery phases are shown in Fig. 4(a) and Fig.4 (b), respectively. It indicates that charges in the interfacial layer (IL) and Box are trapped/de-trapped in a short time due to the relatively small capture/emission time constants, which is mainly attributed to the traps with the shallow energy level. The charges in the high-k layer (HL) turn into the dominant role with increased time due to the high trap density in the HL and show the non-uniform distribution across the gate stacks owing to the differences of the trap locations and electrostatics.

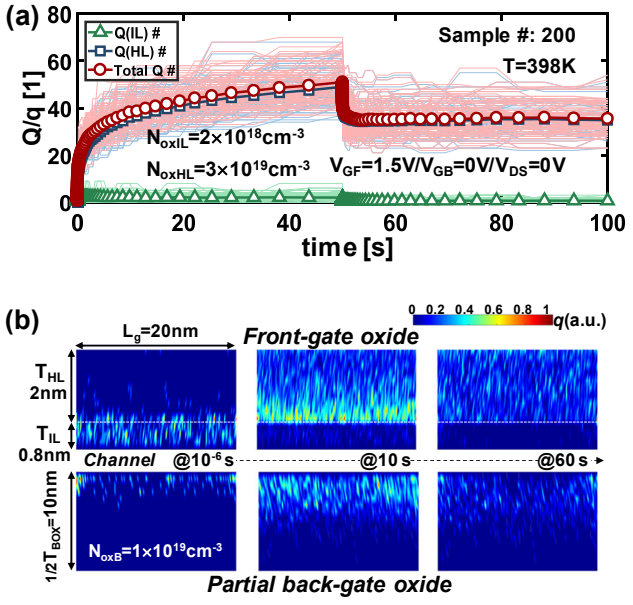

Fig. 4. Time evolutions collected from 200 samples: (a) charge # in IL and HL of the UTBB nFETs subjected to PBTI stress. (b) charge distributions in the front-gate oxide and the partial region of Box.

Fig. 5 shows the degradation difference between the assumed uniform charge distribution and simulated charge distributions. To make a fair comparison, the average charged

traps number is the same for the two cases. It can be noted that the assumption of uniform charge distribution during stress underestimates ΔVth and ΔSS as well as the variabilities. The more serious Vth and SS degradation can be attributed to the fact that most of the charges generated by PBTI stress are trapped near the channel compared to the case of uniform charge distribution. To investigate the role of back-gate oxide in the reliability of the UTBB device, the statistical simulations of PBTI induced parameter degradation with and without the impact of back-gate oxide traps are compared. The results in Fig. 6 show that the degradation and variability increase with the consideration of trapped charges in the back-gate oxide. It can be seen from Fig. 7 that charged traps in the front-gate and back-gate oxides would induce the potential variations at both front- and back channel surfaces, thus deteriorating the electrical characteristics.

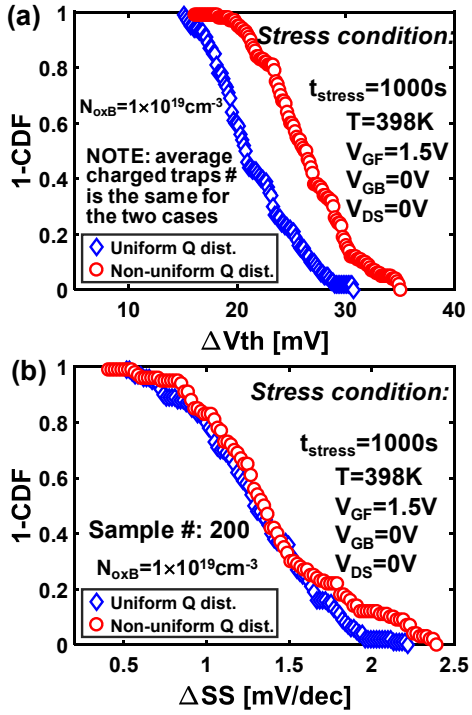

Fig. 5. Comparison of statistical (a) Vth and (b) SS degradations induced by the assumed uniform and simulated non-uniform charge distributions in the dielectrics.

To distinguish the degradation contribution by the traps located in the back-gate oxide, the energy band diagram with the illustration of trap distribution is shown in Fig. 8. The distributions of deep and shallow trap levels in HfO_2 and SiO_2 are taken into account [16]. The active regions in Fig. 8 denote that traps in the Box respond to back-gate bias, indicating the major contribution of shallow energy traps in the Box to the degradation of FDSOI nFET with p-Well during back-biasing.

The impact of different intrinsic trap densities in the Box on trapped charge # during stress is investigated. It can be found from Fig. 9 that the higher intrinsic trap density in the Box leads to more trapped charges and number variation during BTI stress, especially for the case of large back-gate bias. Therefore, improving the quality of back-gate oxide not only reduces the degradation but also mitigates its variability. Current degradation can be also acquired with the developed simulator. More Id degradation in the device with higher trap density in the Box can be observed from Fig. 10 when the back gate bias is enlarged. Moreover, it can be noted that ~1.4% Id after 1000s stress is contributed by RCS under the case of V_{GB} = 3V and N_{oxB}=1×10^{19}cm^{-3}.

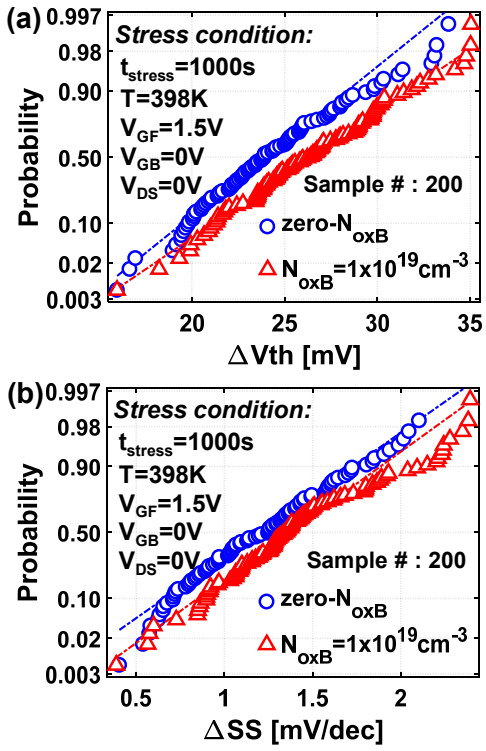

Fig. 6. Comparison of statistical (a) Vth and (b) SS degradation with/without the consideration of back-oxide traps.

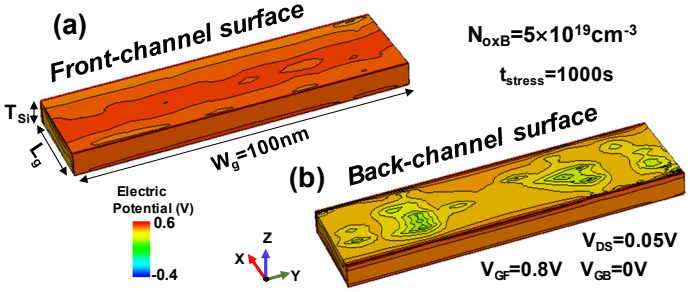

Fig. 7. Charged traps in the dielectrics induce the variations of the electric potential at the (a) front- and (b) back- channel surfaces, respectively.

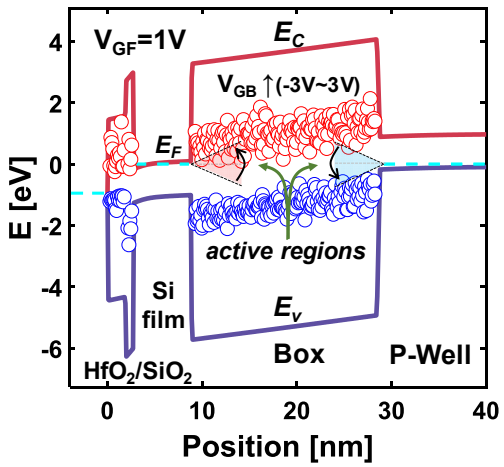

Fig. 8. Traps in the Box of the FDSOI nFET respond to the back-biasing from the energy band diagram perspective.

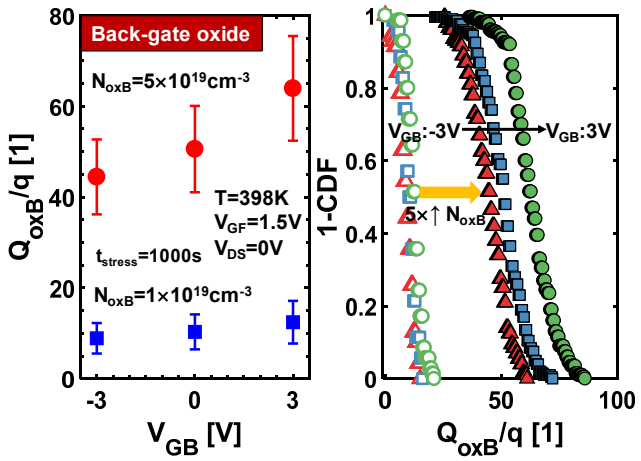

Fig. 9. (a) Charge statistics of the device with different intrinsic trap densities in the Box. (b) Complementary cumulative distribution plots.

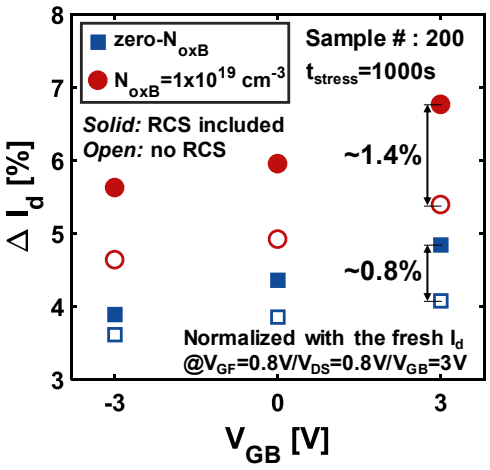

Fig. 10. The effects of RCS on statistical average ΔId of the device with/without traps in the Box during varying back-gate biases.

IV. Conclusion

The 3D KMC simulation approach of trap dynamics in the dielectrics is proposed to track time-dependent charge distribution and degradation. With the proposed method, simulation results show that the assumption of the uniform charge distribution in the dielectrics induced by stress underestimates the statistical degradation and variability. Moreover, the larger initial back-oxide trap density in the UTBB FDSOI brings more serious degradation and variability as the back-gate bias increases.

Acknowledgment

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