Accurate and Efficient Dynamic Simulations of Ferroelectric Based Electron Devices

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I. Introduction

In recent years electron devices based on ferroelectric materials have attracted a lot of interest well beyond FeRAM memories. Negative capacitance transistors (NC-FETs) have been investigated as steep slope transistors [1], [2], and Ferroelectric FETs (Fe-FETs) are under intense scrutiny also as synaptic devices for neuromorphc computing, where the minor loops in ferroelectrics can allow to achieve multiple values of conductance in read mode [3], [4], [5]. Furthermore, the persistence of ferroelectricity in ultra-thin ferroelectric layers paved the way to ferroelectric tunnelling junctions [6], where a polarization dependent tunneling current can be exploited to realize high impedance memristors, amenable for ultra power-efficient and thus massive parallel computation.

In all the above devices the dynamics of ferroelectric domains must be solved self-consistently with the device electrostatics. Furthermore, in MOS transistors having a semiconductor channel, the semiconductor introduces a strong non linearity in the electrostatics, and consequently in the dynamic equations describing the ferroelectric device evolution. The defects at the interfaces also play an intriguing role in ferroelectric FETs [7], in contrast to the well established and detrimental effects in conventional FETs [8]. Moreover, the presence of different trap levels imply a large range of charging and discharging time constants, possibly very different compared to the ferroelectric time constants.

In this paper we compare different numerical integration methods to achieve an accurate and effective simulation of NC-FETs, where the dynamics is governed by possibly very different time constants for either the ferroelectric or interface traps.

II. Model description and numerical algorithms

In the multi-domain, time-dependent Landau-Khalatnikov Equations (LKE) the description of ferroelectric domains requires the numerical solution of a set of differential equations for the polarization P_i of the i-th domain that read [9], [2]

$$\rho\frac{dP_i}{dt} = -(a_iP_i + b_iP_i^3 + c_iP_i^5) + \frac{V_{fe,i}}{T_{Fe}} + k\sum_j(P_j - P_i) \quad (1)$$

where ρ is a resistivity associated to domain switching, k is a coupling factor between nearest neighbor domains and $V_{fe,i}$ is the ferroelectric voltage drop for the i-the domain. The ferroelectric parameters were calibrated by comparing to experiments in [10], and the resulting set is [2] a=-9.5$\times10^8$ m/F, b=2.01$\times10^{10}$ m^5/F/C^2, c=5.11$\times10^{10}$ m^9/F/C^4.When the ferroelectric is operated at small P (e.g. in NC-FETs), the linear term in Eq. (1) is dominant and a time constant τ_{Fe}=$\rho/|a|$ is readily identified, which is a property of the ferroelectric material.

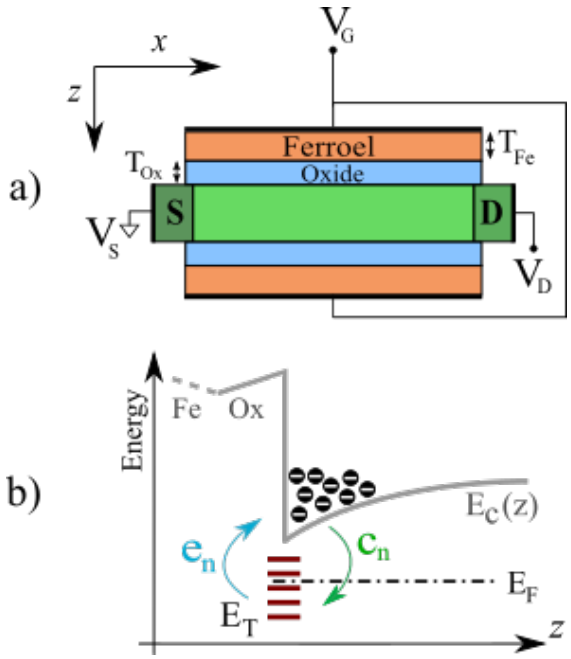

Fig. 1: a) Sketch of the double-gate ferroelectric NC-FET used in our simulations. b) Representation of the capture, c_n, and emission, e_n, processes for electrons at the semiconductor-oxide interface. E_T denotes the energy of an individual trap, E_C is the conduction band and E_F is the local Fermi-level.

Our analysis will be focused on an n-type, double-gate ultra-thin body (DG-UTB), nanoscale NC-FET (see Fig.1(a)), and a single domain analysis is used because the channel length is comparable to the size of ferroelectric domains [11]. Current is calculated with a simple ballistic top-of-the-barrier (ToB) model [12], [13], where electrons at the ToB with positive and negative velocity are taken to be in equilibrium with respectively the source, $E_{f,S}$, and drain Fermi level $E_{f,D}$=(E_{fS}-qV_{DS}) [12].

Quantization in the semiconductor is described with a 1D, parabolic effective mass Schrödinger solver, with valley multiplicities, and effective masses corresponding to a [100] silicon interface [14]. The link between the semiconductor and dielectrics is given by continuity conditions for the electric displacement at the interfaces; more modelling details may be found in [15].

We included in our analysis acceptor-type traps in the upper half of the silicon energy gap (see Fig. 1(b)), which exchange electrons with the conduction band with an emission, e_n, and

978-1-7281-0940-4/19/$31.00

capture rate c_n. The continuity equation for the carrier density n_T in traps with energy E_T can be written as [16]

$$\rho \frac{\partial n_T}{\partial t} = c_n \left(N_T - n_T\right) - e_n n_T \tag{2}$$

where N_T is the trap density at energy E_T, and

$$e_n = \sigma\, v_{th}\, N_C \exp[(E_T - E_C)/(K_B T)] \tag{3a}$$
$$c_n = \sigma\, v_{th}\, N_C \exp[(E_f - E_C)/(K_B T)] \tag{3b}$$

with E_C and E_f being the conduction band edge and local Fermi level, and σ, v_{th}, N_C denoting respectively the trap cross-section, thermal velocity and conduction band effective density of states. For any trap energy E_T, we solve Eq. (2) self-consistently with the ferroelectric dynamics governed by Eq. (1), in fact the charge in the traps Q_{it}=$-q\sum_{E_T} n_T(E_T)$ influences the overall electrostatics in the gate stack and thus across the ferroelectric.

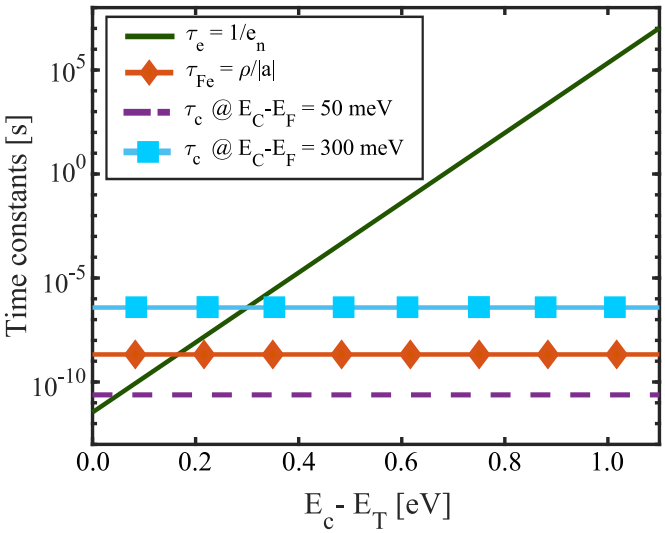

Fig. 2: Estimated time constants for the ferroelectric dynamic τ_{Fe}=$\rho/|a|$, and for the emission, τ_e=$1/e_n$, and capture process, τ_c=$1/c_n$, at the silicon oxide interface. In this work we use σ=10^{-15}cm^2, v_{th}=$2.3 \cdot 10^7$ cm/s, N_C=$3.2 \cdot 10^{19}$ cm^{-3}, which are the values experimentally extracted values for a Si-SiO$_2$ interface [17]. Moreover, for the ferroelectric we calibrated the model against data for large area metal-ferroelectric-metal structures [10][15].

Fig. 2 shows the time constant of the ferroelectric, whose parameters were extracted in [15] by comparison to experiments in [10]. Fig. 2 further compares those time constants to those of the interface traps, that depend on the external bias through the alignment between E_C and E_f. The figure confirms that a wide range of time constants are present in the problem at study. In other words the problem is numerically extremely stiff. In the numerical simulation community it is well known that, for such a problem, using standard explicit integrators would force very small time steps in order to avoid numerical instability. Fortunately an efficient implementation, not requiring small time steps and guaranteeing numerical stability, can still be obtained by employing implicit time domain integrators [18], [19], such as the trapezoidal method.

III. Results and Discussion

Our results were obtained for an n-type, DG-UTB NC-FET illustrated in Fig.1(a), having a 7 nm silicon film thickness, and a ferroelectric and interfacial SiO2 layer of respectively T_{Fe}=20nm

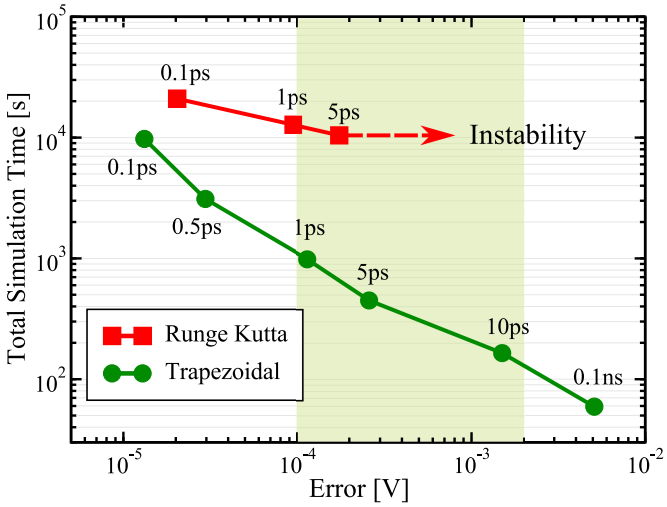

Fig. 3: Total simulation time (for one period of the input signal and for f=5MHz) versus maximum surface-potential error (i.e. potential at the silicon-SiO$_2$ interface) for an explicit Runge Kutta and the implicit trapezoidal methods. The shaded area indicates the typical range of acceptable maximum errors for the surface potential, namely between 10^{-4} and 2×10^{-3}V at room temperature. Note that the largest time step before the explicit method becomes unstable corresponds to a very small 0.15mV error.

and T_{ox}=0.5nm. An energetically uniform distribution of acceptor traps is assumed in the upper half of the energy-gap, with a concentration D_{it}=10^{13} cm^{-2}eV^{-1}.

In Fig.3 we compare the performance of an explicit integrator (Runge Kutta) with an implicit integrator (Trapezoidal). The figure shows that the total simulation time decreases in both methods for increasing values of the error, computed as the infinity norm of the semiconductor surface potential φ at different time-steps δ_t:

$$Error = ||\varphi_{\delta_t} - \varphi_{10fs}||_\infty := max\left(|\phi_{\delta_t} - \phi_{10fst}|\right) \tag{4}$$

where the potential calculated for δ_t=10fs was used used as the reference. However Fig.3 also shows that the explicit integrator becomes unstable for time steps larger than those needed to produce an error of 0.2mV. In other words, the explicit method is forced to continue using very small time steps and producing a small error even when larger errors would be acceptable. On the other hand the implicit integrator does not have stability problems, not even when using larger time steps when targeting larger values of the error in exchange for faster simulation times. For instance, if an error of 1mV is considered acceptable by the user, the implicit integrator could solve the problem in just 3 minutes while the explicit integrator would still be forced to require more than 4 hours to solve the problem to avoid numerical instability.

Fig.4 reports the simulated I_{DS}-V_G curves for two frequencies of the triangular gate voltage waveform. A few periods of the V_G input waveform were simulated and we verified that the I_{DS} becomes periodic after the first two or three periods, so that the I_{DS}-V_G curve plot can be obtained by taking the corresponding I_{DS} and V_G values in the last period of the V_G waveform. The results obtained with explicit and implicit methods are compared at two time steps, demonstrating a remarkable speed-up of the

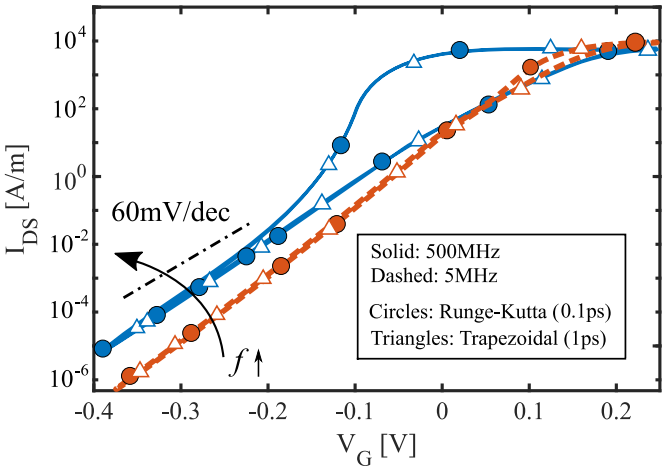

Fig. 4: Comparison of I_{DS}-V_G characteristics at different frequencies and for two integration methods . The curves are obtained with a uniform trap density D_{it}=10^{13}cm$^{-2}/eV$, the LKE coefficients reported in fig.2 and for a ρ=0.5Ωm. The curves obtained with the different integration methods are almost indistinguishable, but the speedups are consistent with the ones reported in Fig.3.

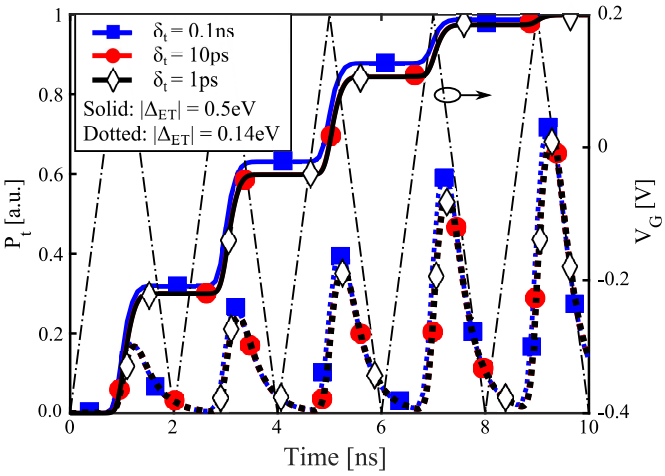

Fig. 5: Occupation probability P_t=n_t/N_t for two trap levels (in midgap position and closer to the conduction band) corresponding to the f=500MHz curve in Fig.4 and for three integration time-steps δ_t; the V_G input waveform is also shown (right y axis).Δ_{ET}=E_C-E_T is the distance between the energy level of the trap and the conduction band at the semiconductor-dielectric interface.

simulation time, enabled by a drastic reduction of the time step for a given accuracy. From a device perspective, Fig.4 also confirms how the presence of acceptor type interface traps can help reduce the subthreshold swing below 60mV/dec in NC-FETs (in contrast to the well-known detrimental effect it has in conventional MOSFETs), essentially because the traps improve the capacitance matching between the ferroelectric and the SiO_2-semiconductor stack [15]. However such a benefit tends to vanish at higher frequencies because the occupation of the traps cannot follow the gate voltage waveform, so that the subthreshold steepness of the I_{DS}-V_G curve degrades and the amplitude of the hysteresis enlarges by increasing the frequency.

To highlight the sensitivity of simulation outcomes to integration-step variations, in Fig.5 we have reported the occupation probabilities P_t for two energy levels E_T at three different time-step δ_t values, only for the trapezoidal integrator. At the frequency of 500MHz the deepest trap, placed 500meV below the conduction band, is not responding to the input waveform V_G, meaning that the emission mechanism is not fast enough to discharge the level E_T: this is again consistent with the behavior of the I_{DS}-V_G characteristics reported in Fig.4 of reference [15]. Fig.5 also shows that for δ_t smaller than 10ps the curves for different δ_t values are essentially overlapping, whereas for δ_t=0.1ns the difference in the P_t waveforms is sizeable. Still these differences are small and cannot result in an appreciable difference, for example, in the I_{DS}-V_G characteristic of the transistor, such as the curves reported in Fig.4. This is also confirmed by the analysis in Fig.6, where we have reported the relative error for the on- and off-state I_{DS}. As it can be seen for δ_t<0.1 ns the I_{DS} difference with respect to the reference value (i.e. the current calculated for δ_t=10fs) is smaller than 1%, which is sufficiently small for most TCAD applications.

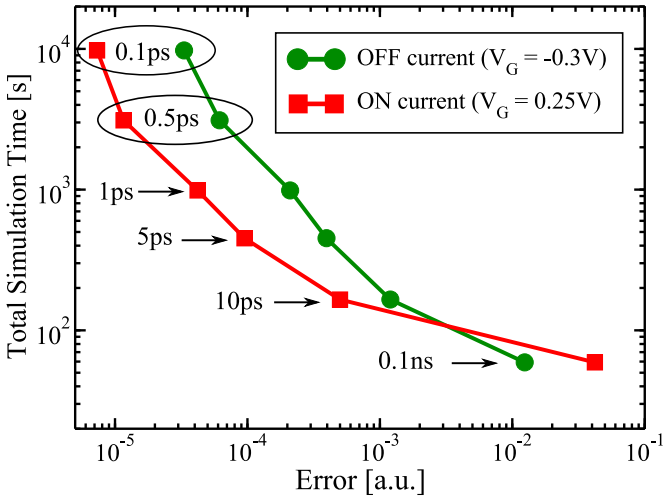

Fig. 6: Total simulation time (for one period of the input signal and for f=5MHz) versus the relative error on the current I_{DS} for the implicit integrator; the reference used to calculate the error is the simulated current at $delta_t$=10fs. We here label as on- and off-state current the I_{DS} at respectively V_G=0.25 V and V_G=−0.3 V (see also the I_{DS} versus V_G characteristics in Fig.4.

IV. Conclusions

In summary, in this work we systematically demonstrated the advantages of an implicit trapezoidal integrator with respect to a explicit Runge-Kutta method for the simulation of NC-FETs having a wide range of time constants set either by the ferroelectric or by the interface traps dynamics. Advantages are observed in terms of robustness of convergence and in terms of simulation time at fixed accuracy. Our results are expected to be useful in the development of robust TCAD tools for ferroelectric based devices, that are important for the design and optimization of ferroelectric FETs and ferroelectric tunnelling junctions. The growing interest for negative capacitance, steep slope FETs and ferroelectric based synaptic devices for neuromorphc computing will make the modeling and simulation of ferroelectric devices a topic of increasing technological relevance in the near future.

V. Acknowledgments

The project has received financial support from the MIT International Science and Technology Initiatives (MISTI) Global Seed Funds, within the MIT-FVG Project (University of Udine, Trieste and SISSA).

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